Rataclock test

Håkan J, apr 2017

Sending module

Reference oscillator

Counter
= time reference

OSC
100 MHz

FPGA

buf

counter

%1024==0?

DCM/PLL

Logic

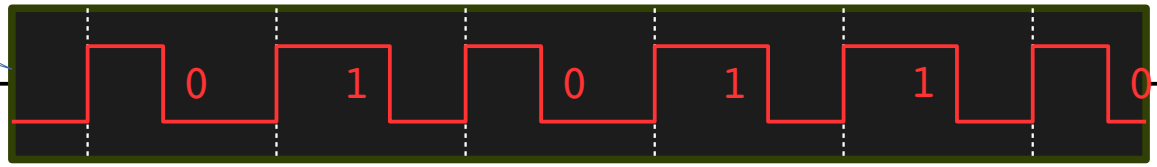
clock+time
sender

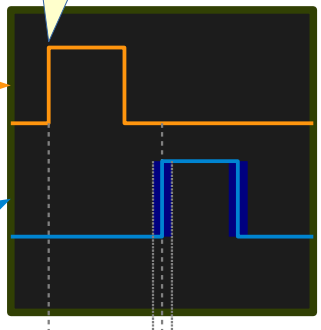
PLL = phase-locked loop
DCM = digital clock manager
(DCM is for ”PLL” in virtex4)

Test:

Ask both modules to
emit pulses at
same counter values

Serial signal,
with clock
(freq+phase)
and time labels





Init / monitor
counter.

Same
frequency
as reference,
and
phase-stable.

OSC
100 MHz

not used

FPGA

Logic

decoder

FF

buf

counter

%1024==0?

DCM/PLL

Δt: cable/routing delay
(constant;
does not matter)

σt: jitter
(= resolution)

Sending module mark

Receiving module mark

Δt between marks – σt ~ 100 ps

Concept A, option 1b