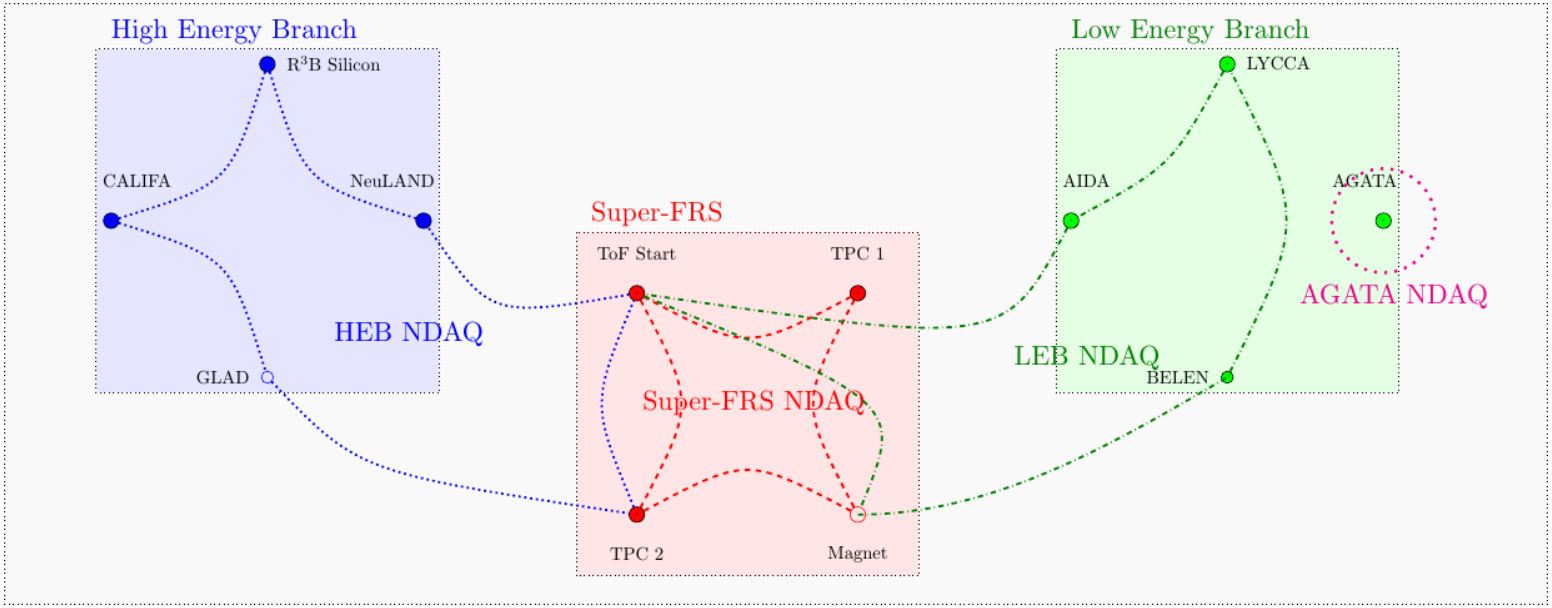
Trigger/Timing Distribution | DAQs Coupling Concept



In lieu of an NDAQ TDR talk

Håkan T. Johansson, Chalmers, Göteborg

Lichtenberghaus, Darmstadt, May 2015

SEP - Signal exchange points

- Flexible trigger, (spanning entire NuSTAR / SFRS complex):
  - 'Any' detector → 'any' detector (optical)
  - Easy topology changes
- The above with:
  - A few dedicated / specialised modules (& TRLO II)
  - Part of the fixed NDAQ installations:
    - Signal exchange points along beam-lines
    - Each detector connected to the close-by SEP
- Flexible time distribution:
  - TOF (few ps)
  - Time-stamping (few ns)
- Use accelerator timing (BuTiS / White Rabbit) (and locally serial TS)

NuSTAR signal exchange points

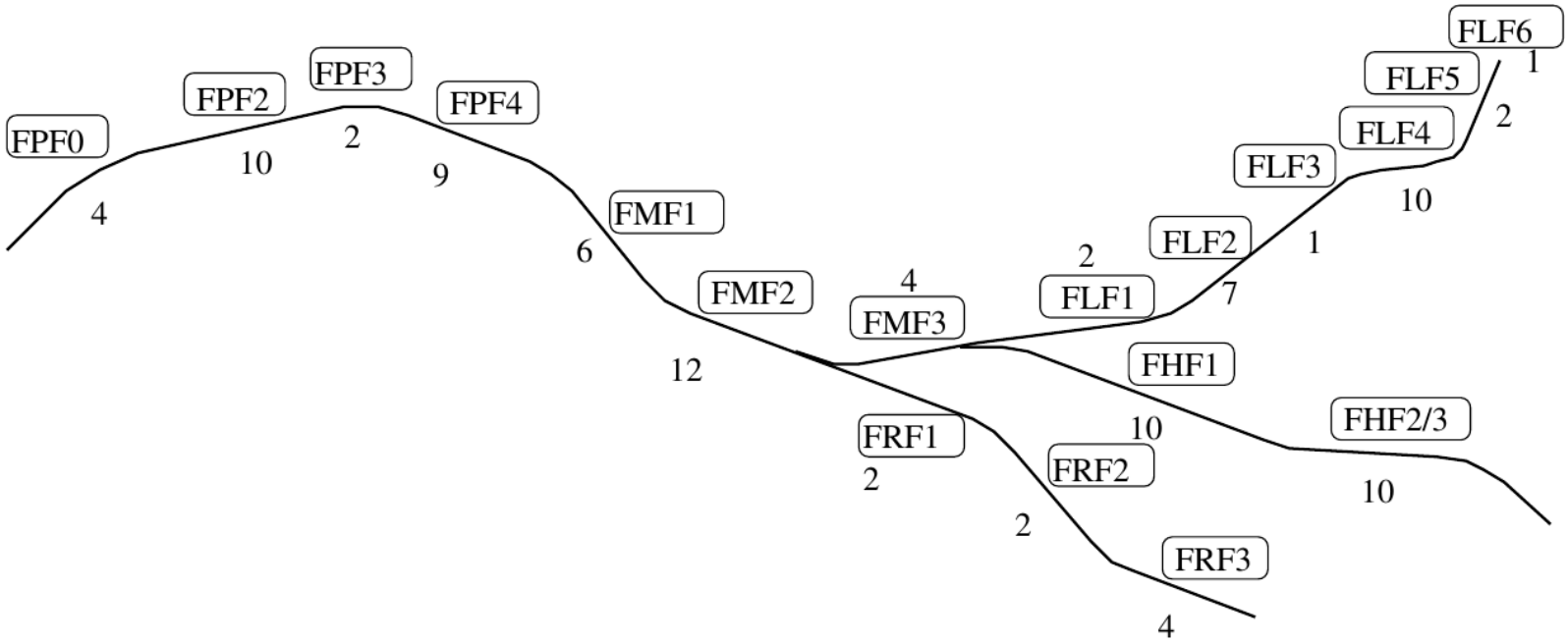


Figure 17: Schematic overview of the NUSTAR experiments and Super-FRS focal planes and local detector counts. The counts include both common Super-FRS infrastructure and experiment-specific detectors. The following notation is used: FPF refers to focal planes of the Super-FRS pre-separator, FMF indicates focal planes of the main Super-FRS, FLF refers to the low-energy branch (i.e. HISPEC, DESPEC, MATS and LaSpec), FHF to the high- energy branch (i.e. R^3B) and FRF indicates the ring branch.

CPU + FPGA

Before continuing:
2 slides with
mini SBCs

CPU + FPGA on same chip
- CPU boots,
- then programs FPGA!

CPU+FPGA

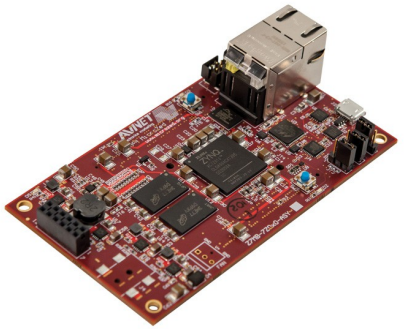
As daughterboard, with:
- RAM
- Network
- I/O

→ Full-featured mini-computer, running Linux.

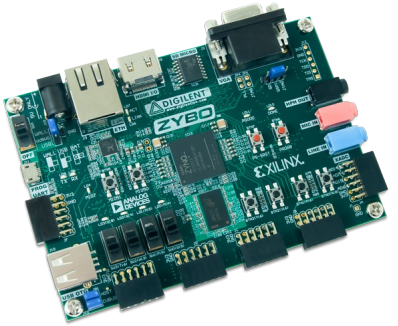
Off-the-shelf examples:

Enclustra MARS-ZX3

ZedBoard.org MicroZED

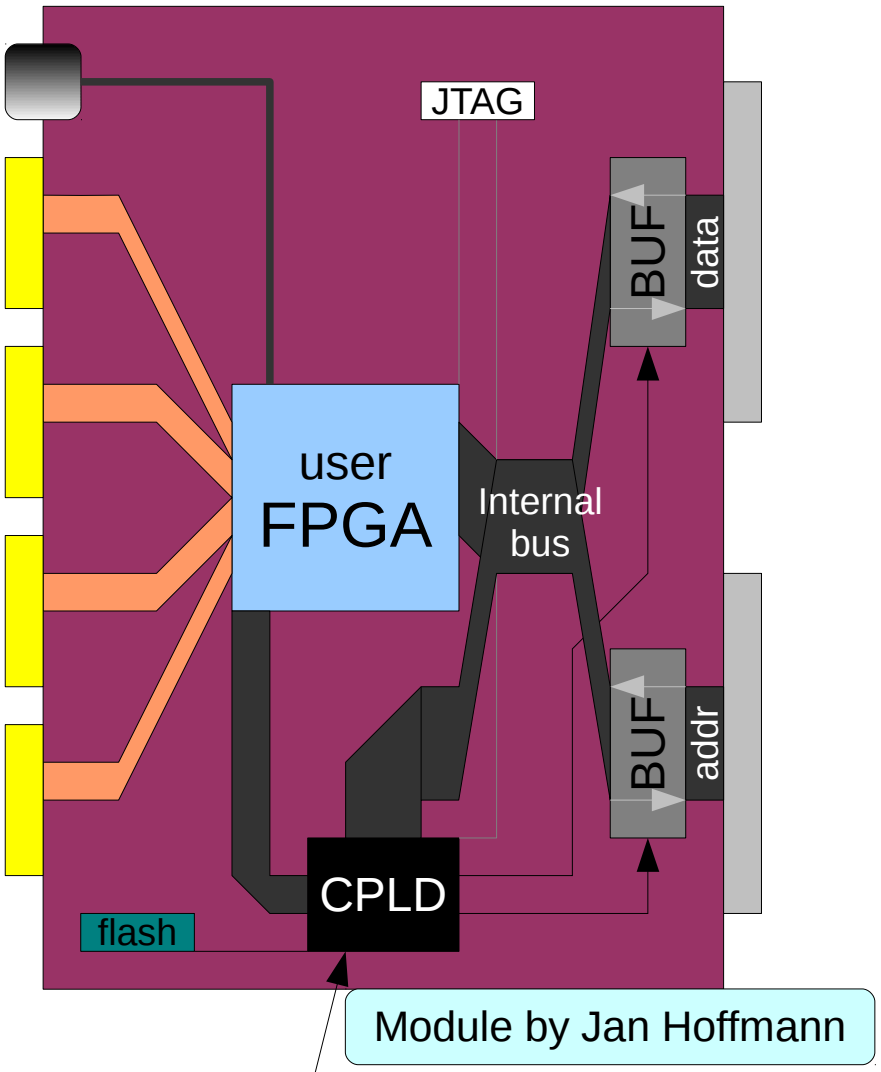


Digilent ZYBO



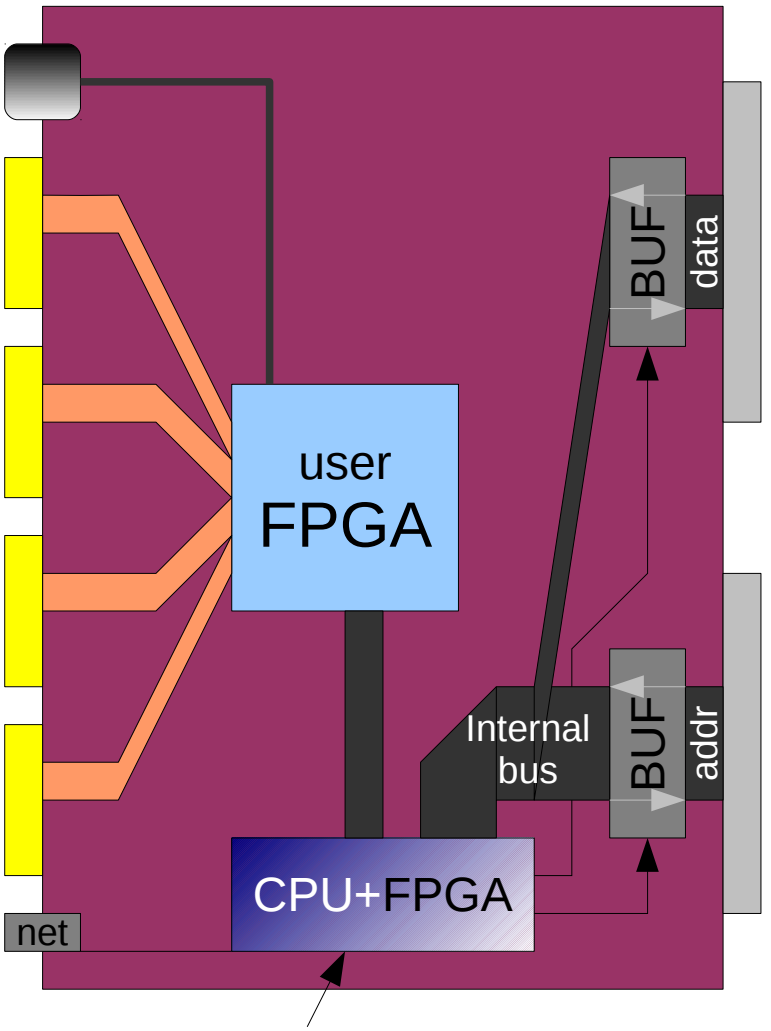
Netbooted VULOM-X

Current (VULOM4)



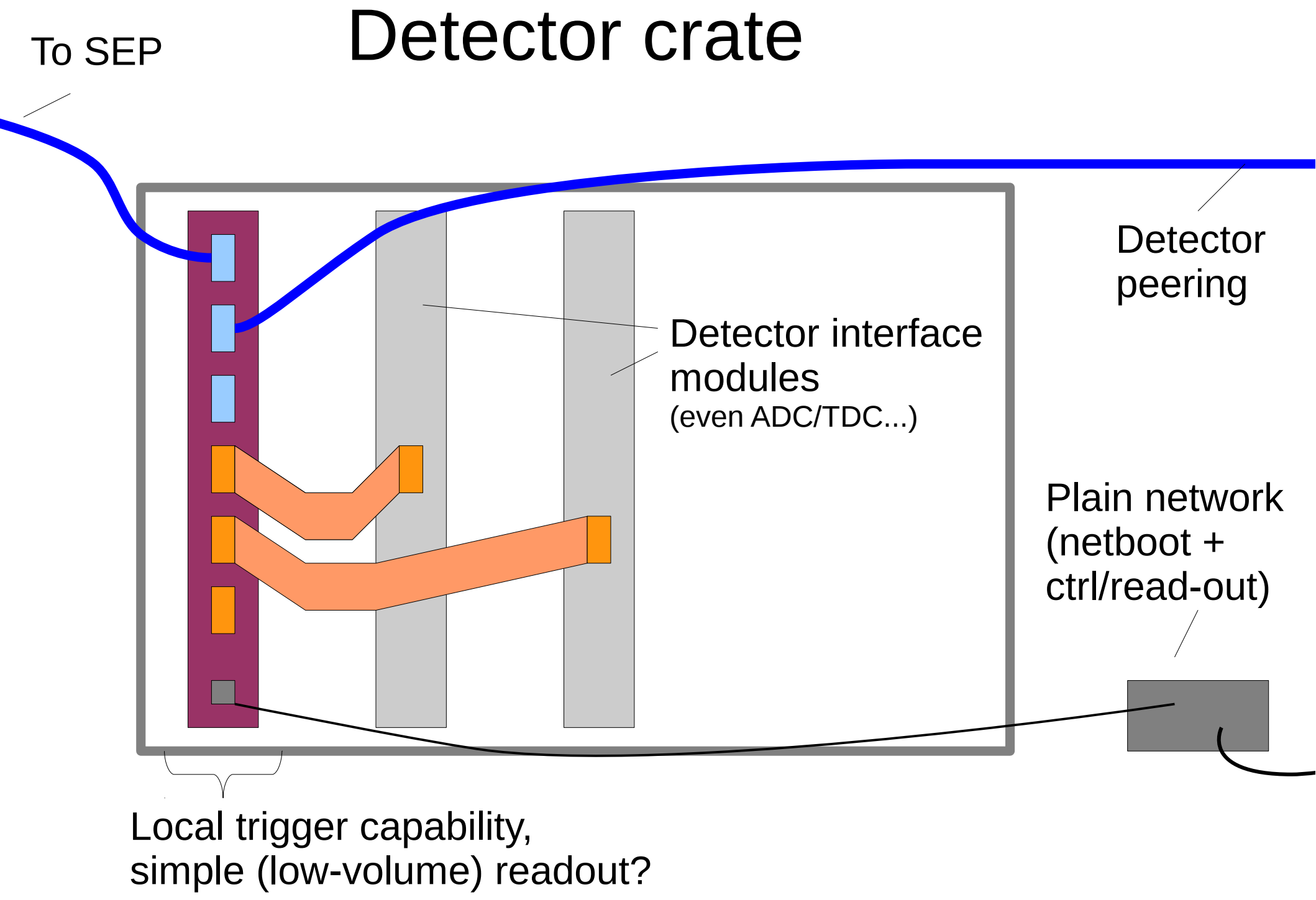
Loads firmware from flash onto user FPGA
Flash programmed from VME.

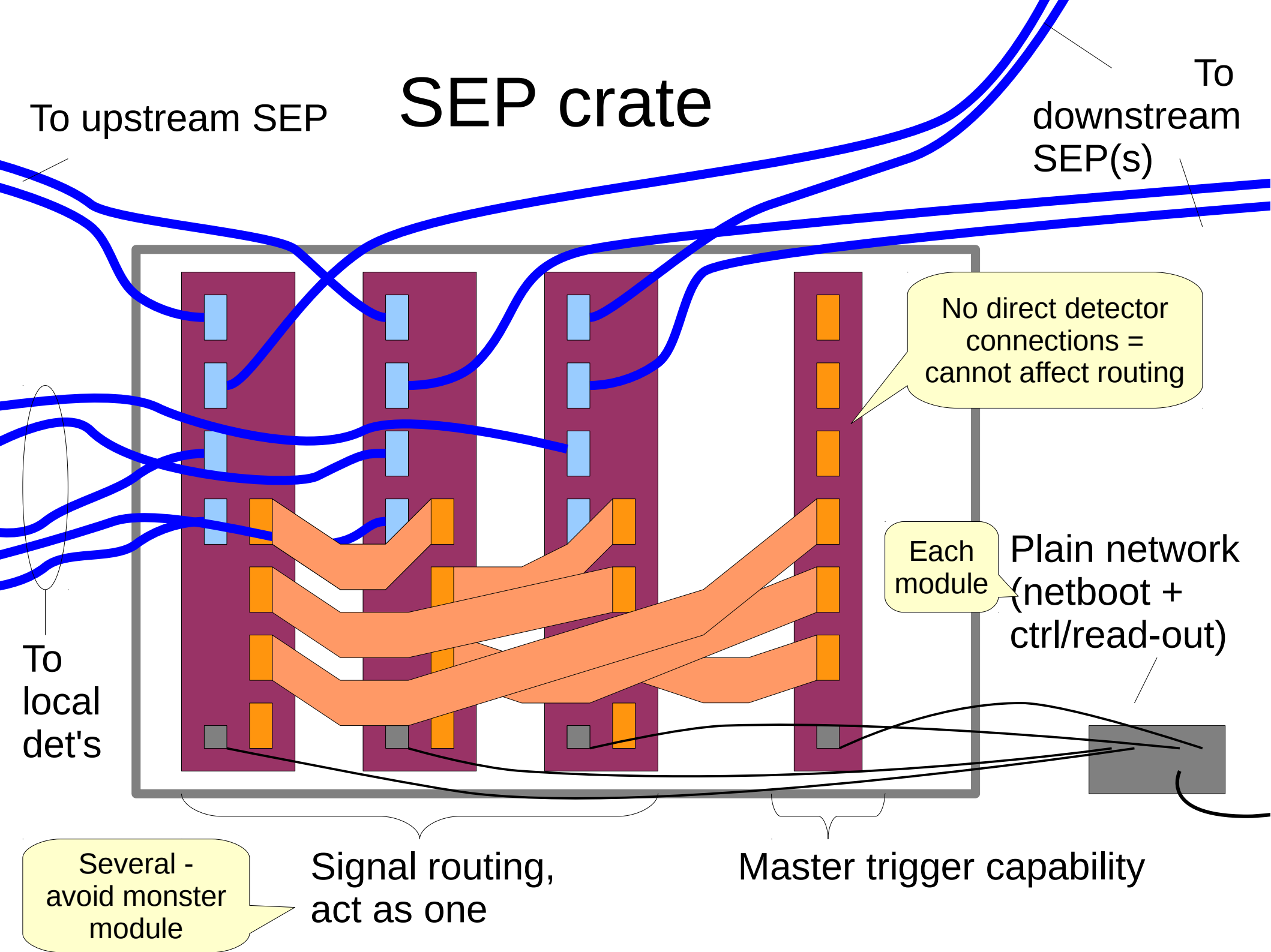
Suggested (with SOC CPU+FPGA)



Boots over network, init sys FPGA,
loads user FPGA firmware.
Read-out CPU. Could be VME master.

Detector crate




SEP crate
To upstream SEP
To downstream SEP(s)
No direct detector connections = cannot affect routing
Each module
Plain network (netboot + ctrl/read-out)
To local det's
Several - avoid monster module
Signal routing, act as one
Master trigger capability

Time distribution

Common time scale (WR)

TOF

Time-stamp events

BuTiS

< 20 ps/2 km

NO

GSI accelerator developments: BuTiS and WR groups

Naturally, special hardware

WR switch

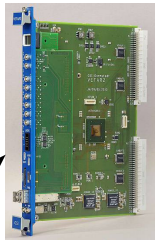
White Rabbit

< 100 ps/km

22 ps VFTX-VFTX (separate feeds)

1 ns / 8 ns

PEXARIA5



VETAR2

WR hardware

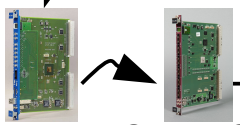
One central master

Serial TS (TRLO II)

NO

< 2 T clk, recv (20 ns @ 100 MHz)

Cheap & easy(?)



VETAR+RIO+VULOM = 'gray rabbit' (expensive conversion crate)

~600 LUTs of an FPGA