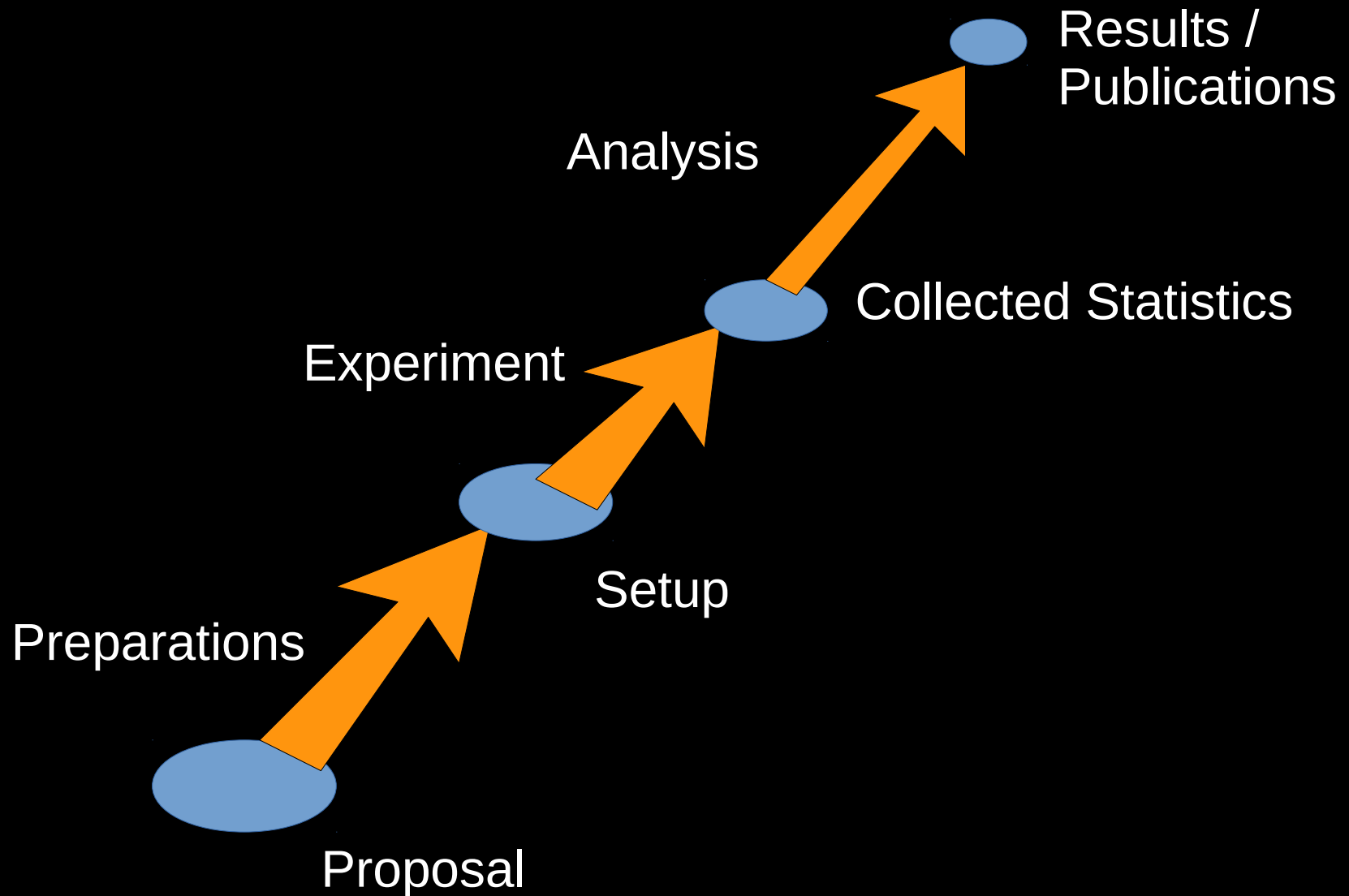


Statistics, dead-time & free-running

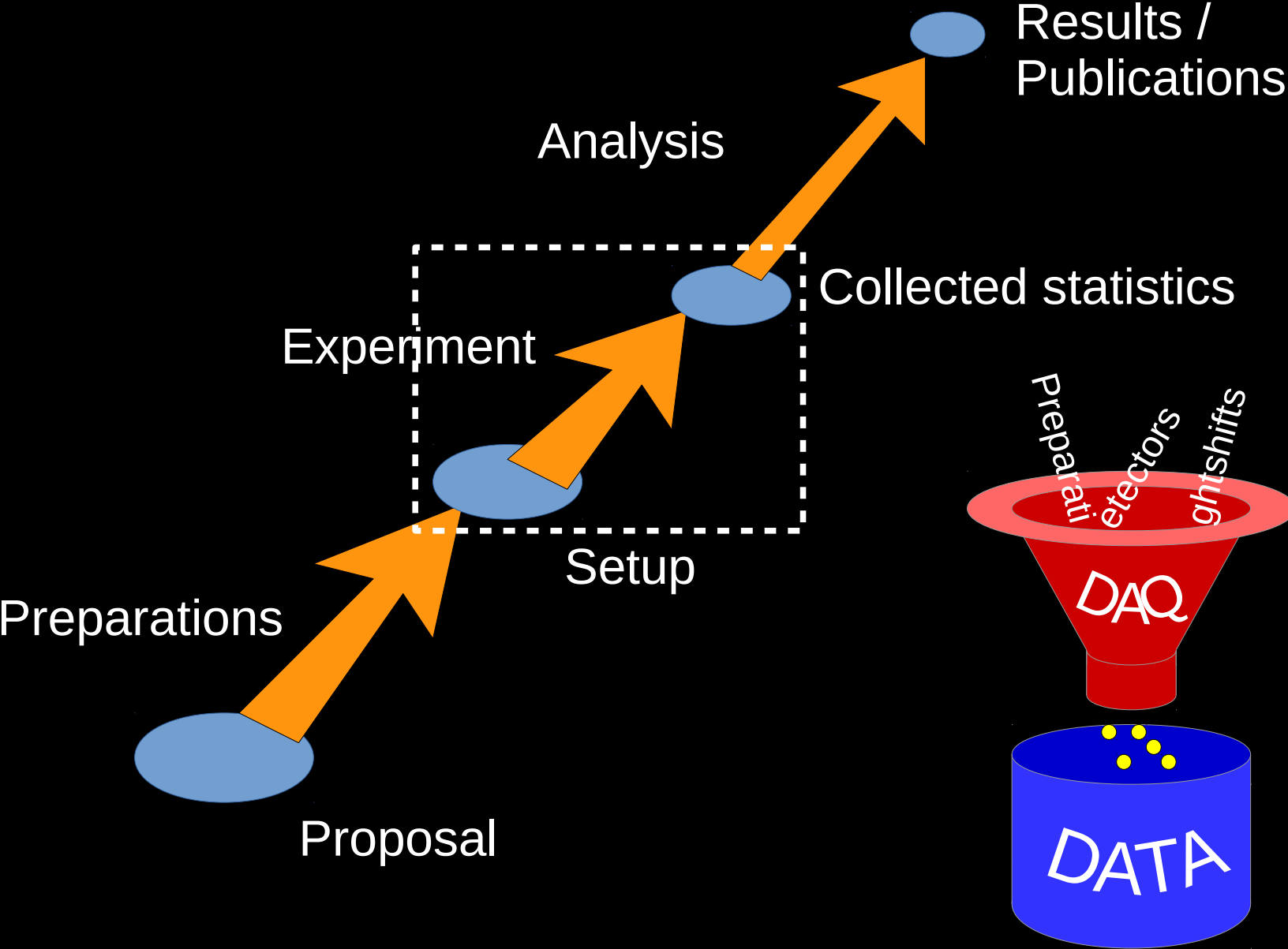
Håkan Johansson, Chalmers, Göteborg

Lichtenberghaus, Darmstadt, May 2019

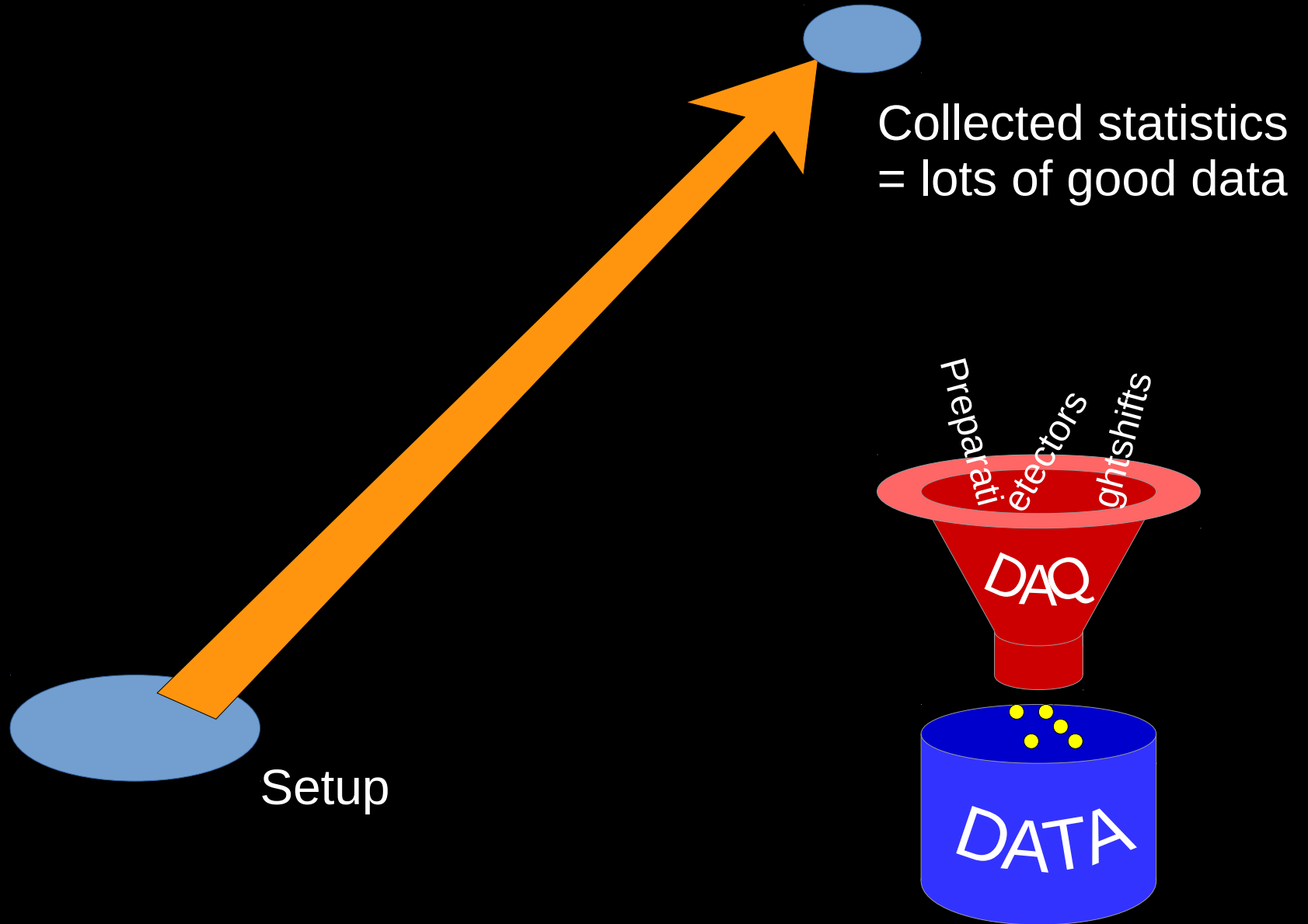
Experiment Lifecycle



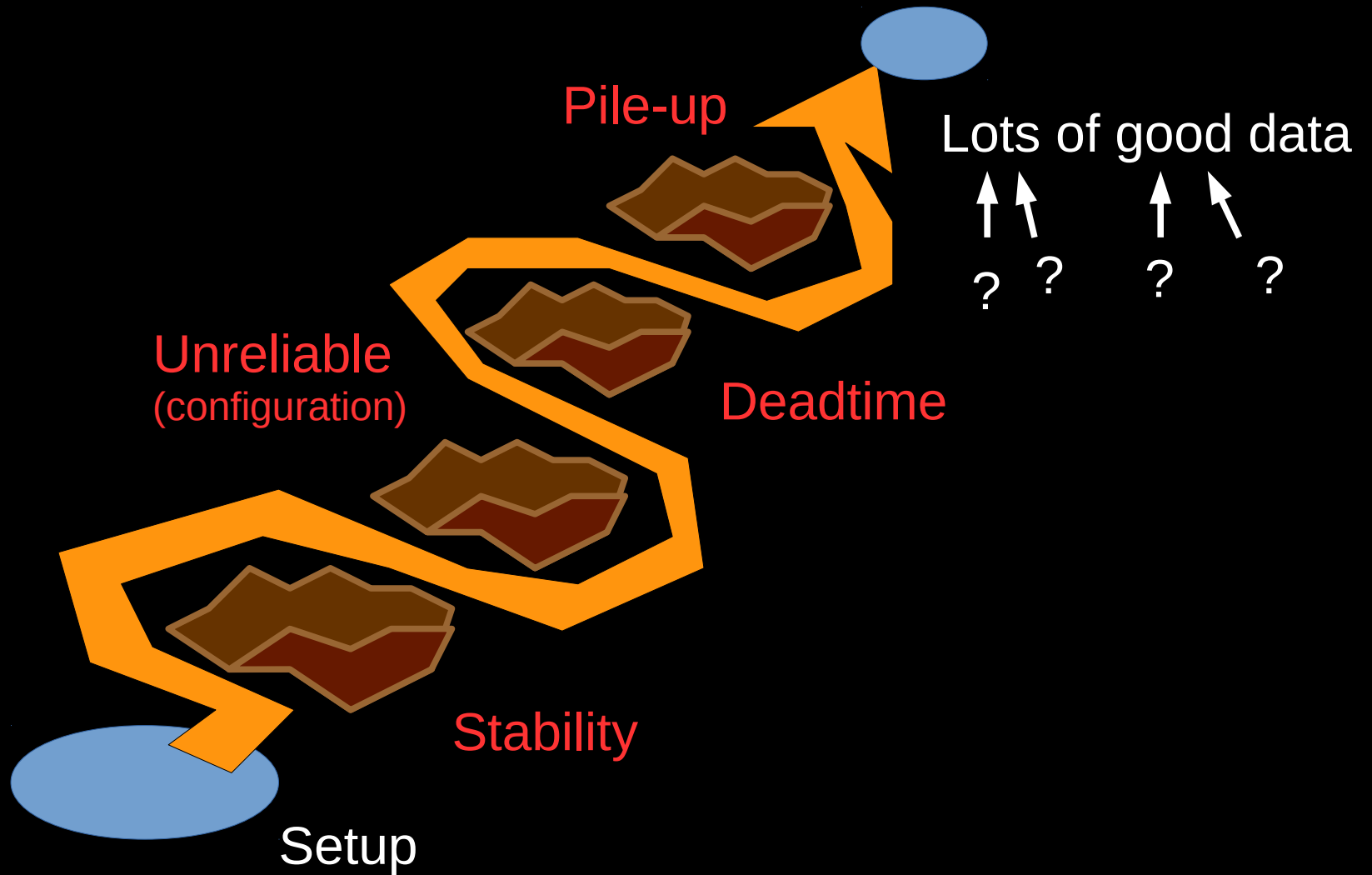
Experiment Lifecycle—Focus...



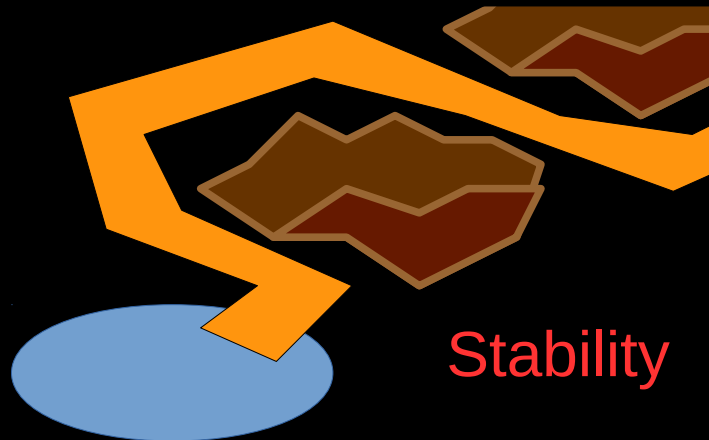
Experiment



Experiment Hazards



Stability Hazard



Diagnosis:

Hardware or software?

Likely: firmware issues!

Action:

Many components are involved...

Introduce checksums,
to pin-point *where* problems are.

S393: Aug 28 → Sep 12 (2010)

8 subsystems

→ 12 crashes/stuck (< 1/day)

(1 noted in elog)

Stability "level":

Users reported individual DAQ
error messages to operator!

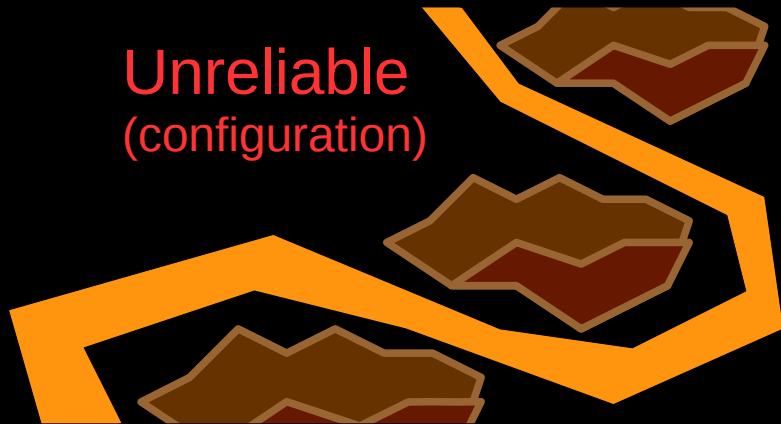
S444/S473/S454

10-16 subsystems in main DAQ

5 night hours: **9 subsystem hiccups**
(autorecovered)

(S473, elog #597)

Reliable configuration Hazard



Special concern:

- CALIFA
 - S444, elog #252
 - S454, elog #159, #274

Diagnosis:

Readback mismatch set values...

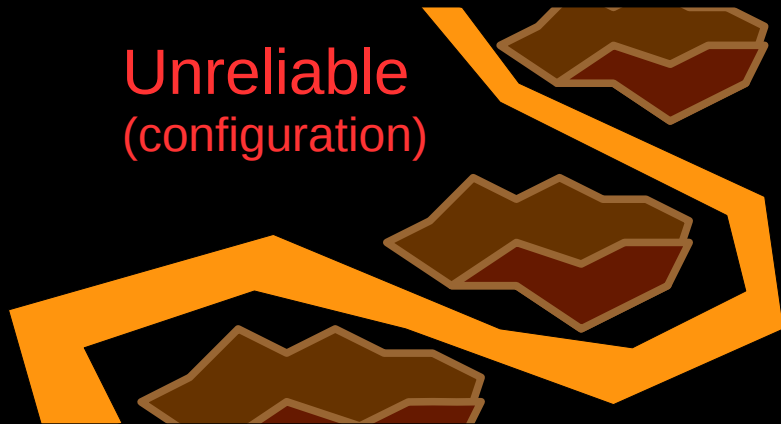
Firmware!

CALIFA FEBEX firmware
fails to meet timing by 8%!
(worst propagation delay
vs. clock period)

Action:

(Debug) & fix!

Reliable configuration Hazard



Unreliable
(configuration)

In **many signal paths!**
With many cards, not unlikely to **manifest in reality...**
When? Depends on which card, temperature, 'unlucky' clock cycle...

Diagnosis:
Readback mismatch set values...
Firmware!

Action:
(Debug) & fix!

CALIFA FEBEX firmware **fails to meet timing by 8%!**
(worst propagation delay vs. clock period)

The firmware can—as written—not be reliably run on the given FPGA (family).

Deadtime Measurements



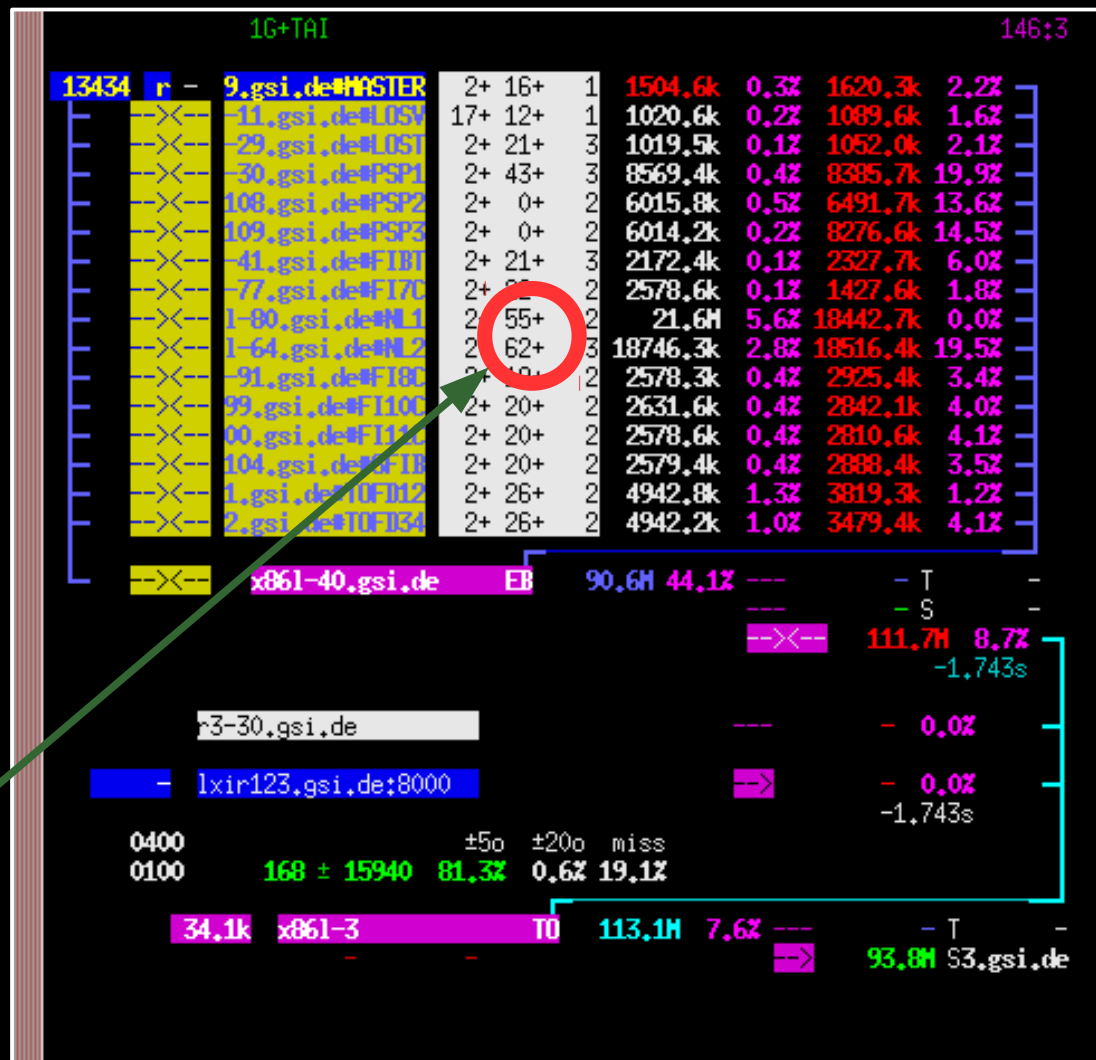
Deadtime

Diagnosis:

Measure individual subsystems
(introduced S473, [elog #568](#))

Action:

Deal with **slowest systems**,
(one at a time...)



Deadtime Limitations



Make sure early DT-release can be used reliably for all systems.

Investigate PC-internal (PCIe) communication overhead between CPU ↔ PEXOR/KINPEX.

(2.5 us/read, 0.5 us/write)
[fewer possible?, // over SFPs]

Diagnosis:

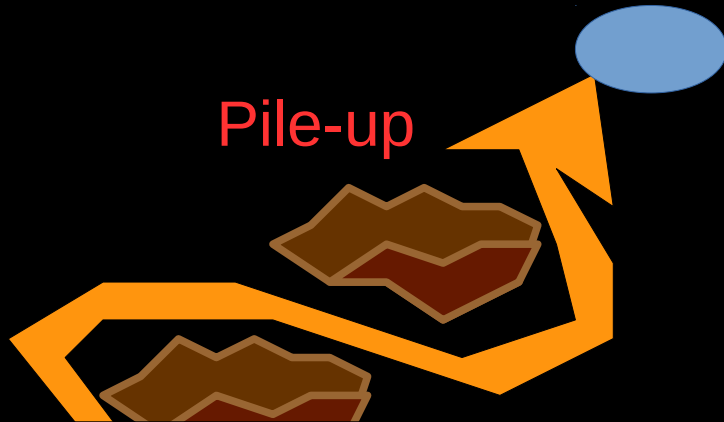
Measure individual subsystems
(introduced S473, [elog #568](#))

Action:

Deal with **slowest systems**,
one at a time...

Subsystem	Status	Value 1	Value 2	Value 3	Value 4	Value 5	Value 6
9.gsi.de#MASTER	2+ 16+	1	1504.6k	0.3%	1620.3k	2.2%	
11.gsi.de#LSU	17+ 18+	1	1020.6k	0.2%	1089.6k	1.6%	
20.gsi.de#LSU	2+ 21+	3	1019.5k	0.1%	1052.0k	2.1%	
30.gsi.de#SP1	2+ 43+	3	8569.4k	0.4%	8385.7k	19.9%	
108.gsi.de#SP2	2+ 0+	2	6015.8k	0.5%	6491.7k	13.6%	
109.gsi.de#SP3	2+ 0+	2	6014.2k	0.2%	8276.6k	14.5%	
41.gsi.de#FIB	2+ 21+	3	2172.4k	0.1%	2327.7k	6.0%	
77.gsi.de#FIB	2+ 22+	2	2578.6k	0.1%	1427.6k	1.8%	
1-90.gsi.de#NL1	2+ 55+	2	21.6H	5.6%	18442.7k	0.0%	
1-64.gsi.de#NL2	2+ 62+	3	18746.3k	2.8%	18516.4k	19.5%	
91.gsi.de#FIB	2+ 18+	2	2578.3k	0.4%	2925.4k	3.4%	
99.gsi.de#F110	2+ 20+	2	2631.6k	0.4%	2842.1k	4.0%	
100.gsi.de#F110	2+ 20+	2	2578.6k	0.4%	2810.6k	4.1%	
104.gsi.de#F1B	2+ 20+	2	2579.4k	0.4%	2888.4k	3.5%	
1.gsi.de#TOE12	2+ 26+	2	4942.8k	1.3%	3819.3k	1.2%	

Reaching the pile-up limit ?



Accelerator beam spills:
micro-structure in ejection → pile-up

Detectors can handle
(< 1 us pile-up) [S473](#), [elog #718](#)

Single-event DAQ not so easily...

Diagnosis I:

Much DAQ grief is caused by
trying to fight single-event deadtime

Diagnosis II:

Front-ends are free-running
But readout is event-oriented...

Action:

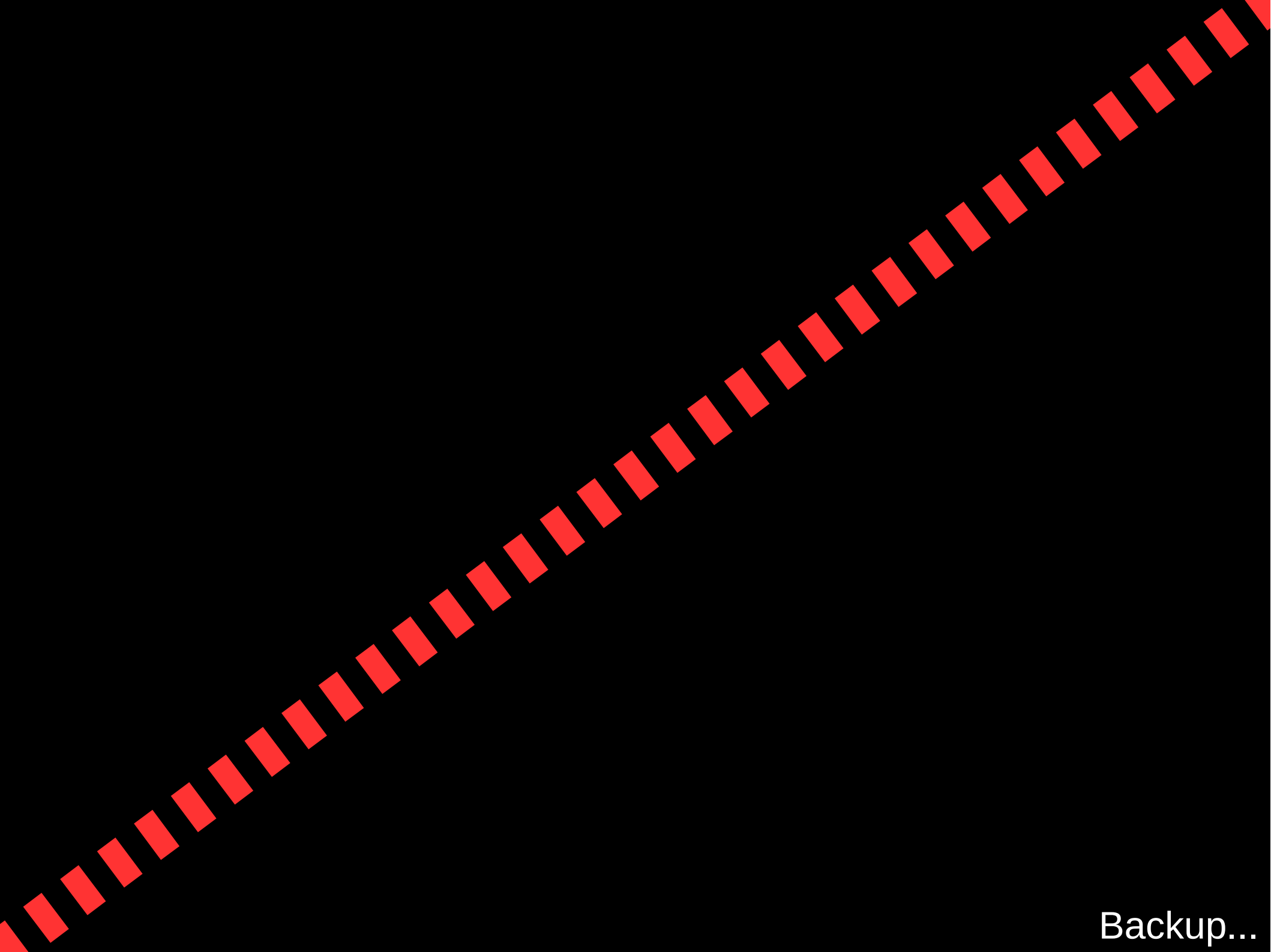
Dump all digitised data
→ software trigger

Use hardware to the limit...

Summary

- 4 x firmware:
 - Stability → firmware?
 - Reliability → firmware!
 - Deadtime → firmwares
 - Free-running → firmware...

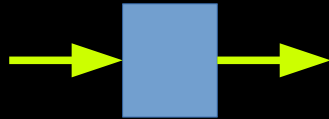
(and software)
- Next talk....:
 - firmware... :-)



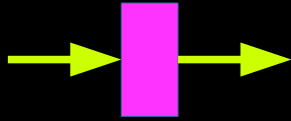
Backup...

Signal propagation delay in FPGA is due to:

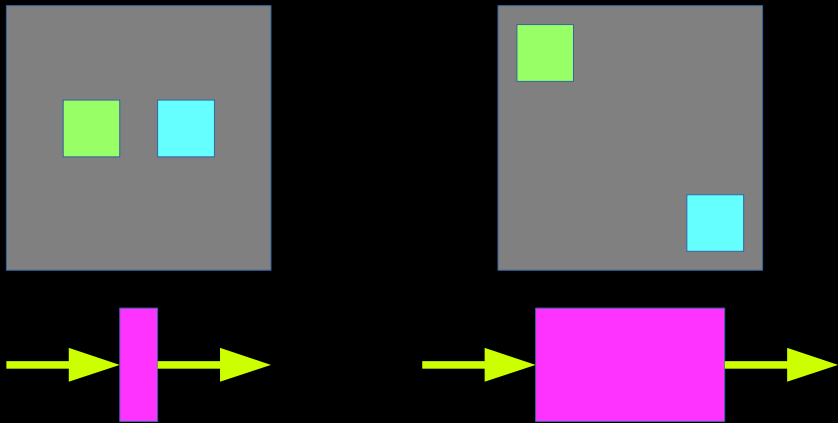
- Logic (LUTs):



- Routing:

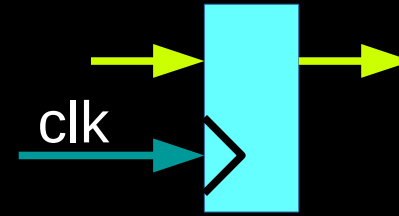


Routing delays generally depend on how far apart on the chip the **source** and **destination** are!

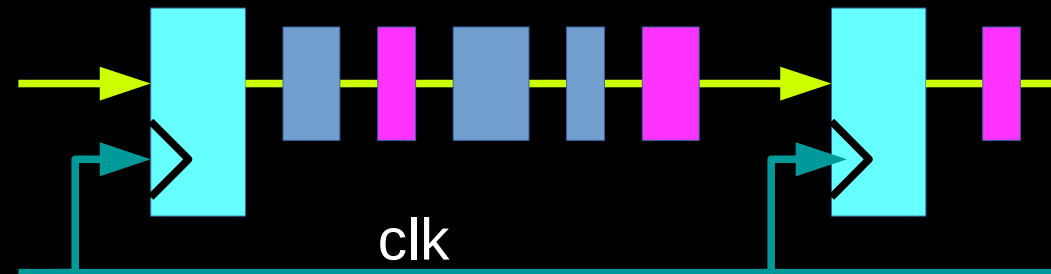


Place & route has to locate components such that **all** routes meet **timing!** (e.g. clock periods)

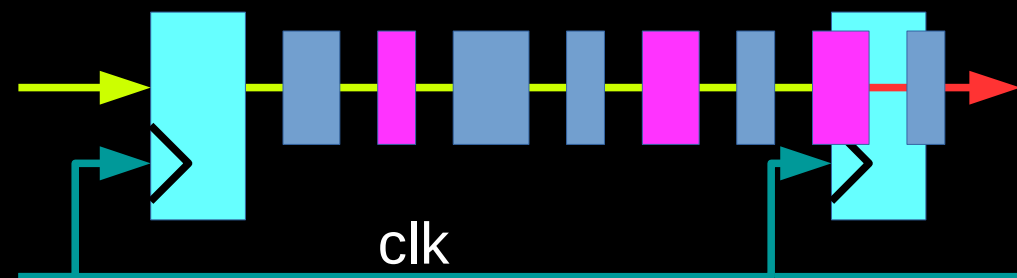
Flip-flops latch on the clock signal



Expressions are between flip-flops:



For expressions that have longer propagation than clock period, ...

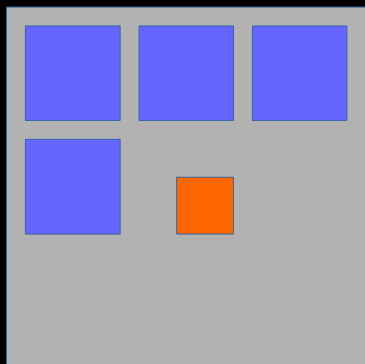


...results **unpredictable!**
(unless you have a time machine!)

BROKEN!

(not so) Preliminary analysis of why CALIFA FEBEX firmware fails to meet timing constraints

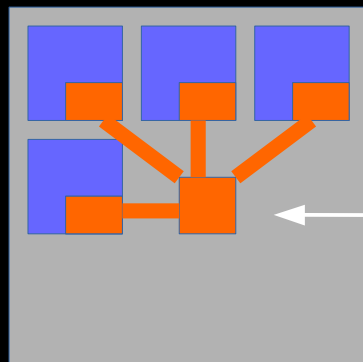
One **PSA** core
(4 channels) uses
~10 % of
FPGA
resources



With 4 cores
(16 channels)
FPGA is not
full.
(actual: 50%)

There is also the **GOSIP** core,
However, not in itself large.

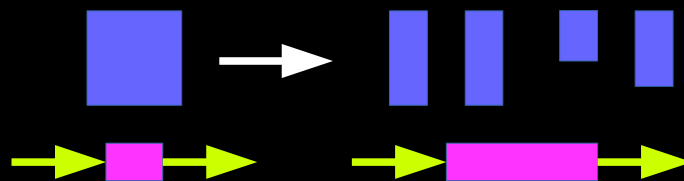
Cannot be viewed
separately!
PSA and **GOSIP**
tie together...



Here **GOSIP** is spread
over large area...

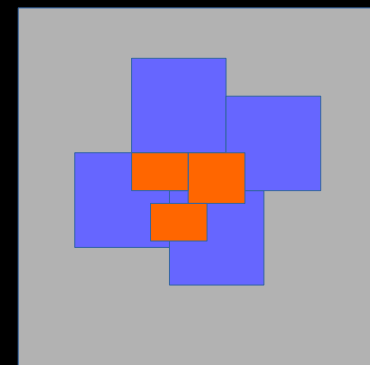
However...

Both **PSA** and **GOSIP** seem to
'just' meet timing:
If spread over larger areas,
Routing delays break timing.



Place & route **cannot solve**...
(more components requires it to
place some things further apart)
So does the best it can do...
(reduce the worst
timing failure).

(Also causes
long compile times.)



NeuLAND readout times

