

# fakernet

Use **standard internet protocols** to  
**read data** from **front-end modules**

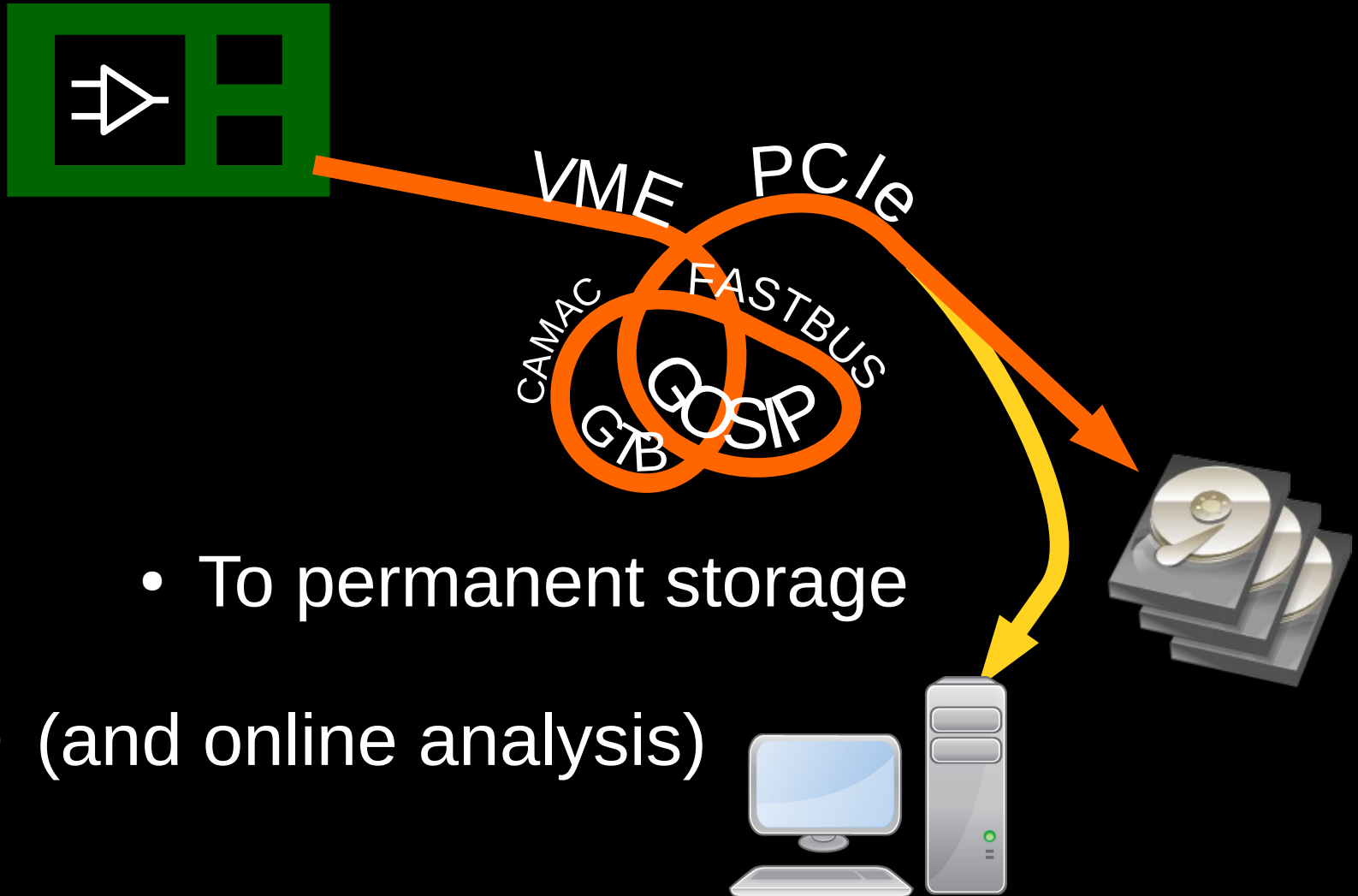
Idea/suggestion:  
Philipp Klenze (TUM)  
(nov 2017)

Hardware interface + testing:  
Anders Furufors (Chalmers)

Håkan Johansson, Chalmers, Göteborg

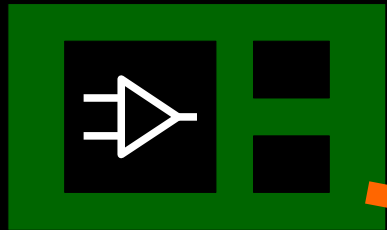
# Purpose of a DAQ

- Move data from front-end boards (ADC, TDC)



# Purpose of a DAQ

- Move data from front-end boards (ADC, TDC)



Nowadays  
(since ~10 years):

- via network  
(ethernet)

VME PCIe  
CAMAC FASTBUS  
GTB QOSIP

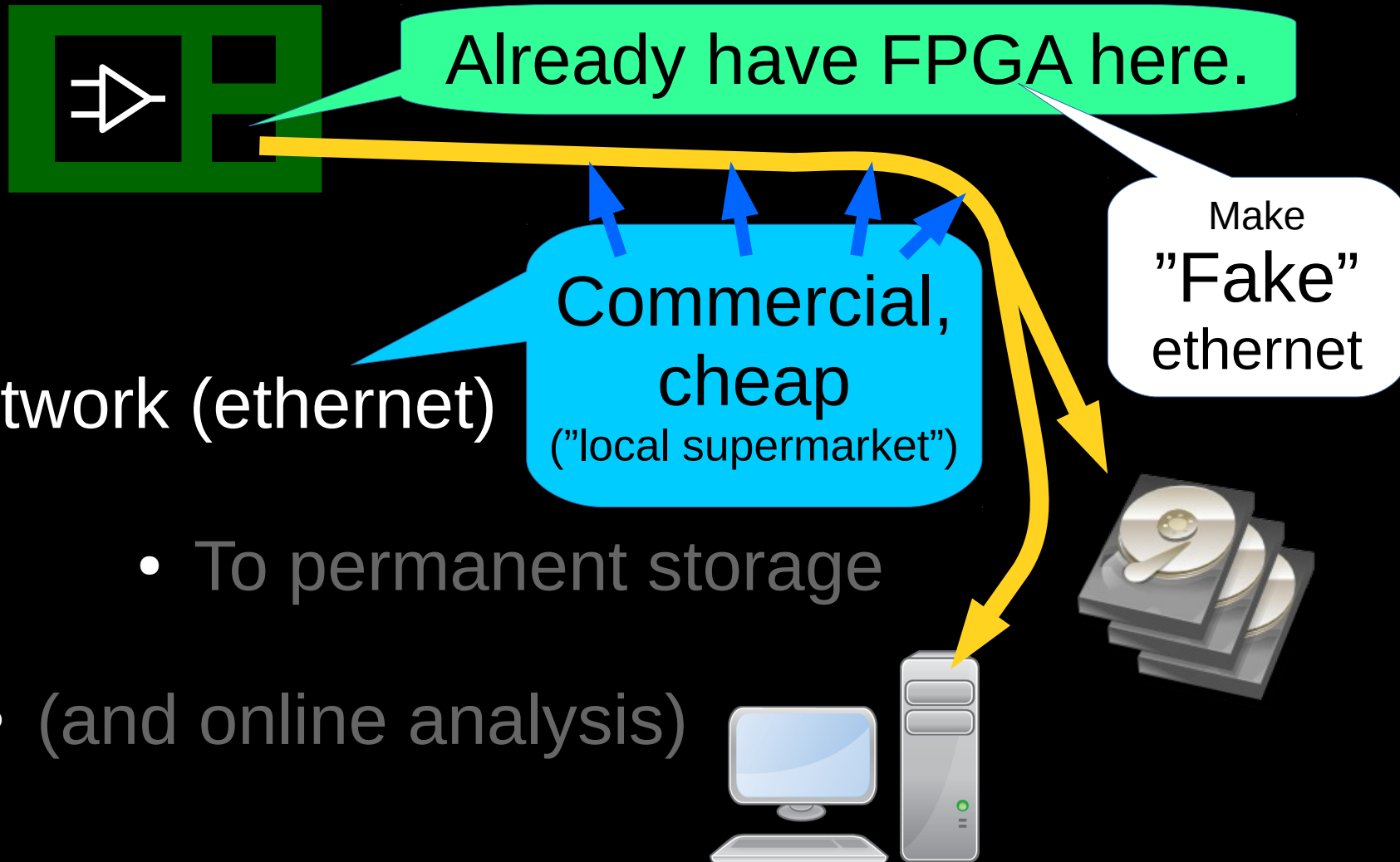
- To permanent storage

- (and online analysis)



# Transport data using TCP

- Move data from front-end boards (ADC, TDC)



- via network (ethernet)

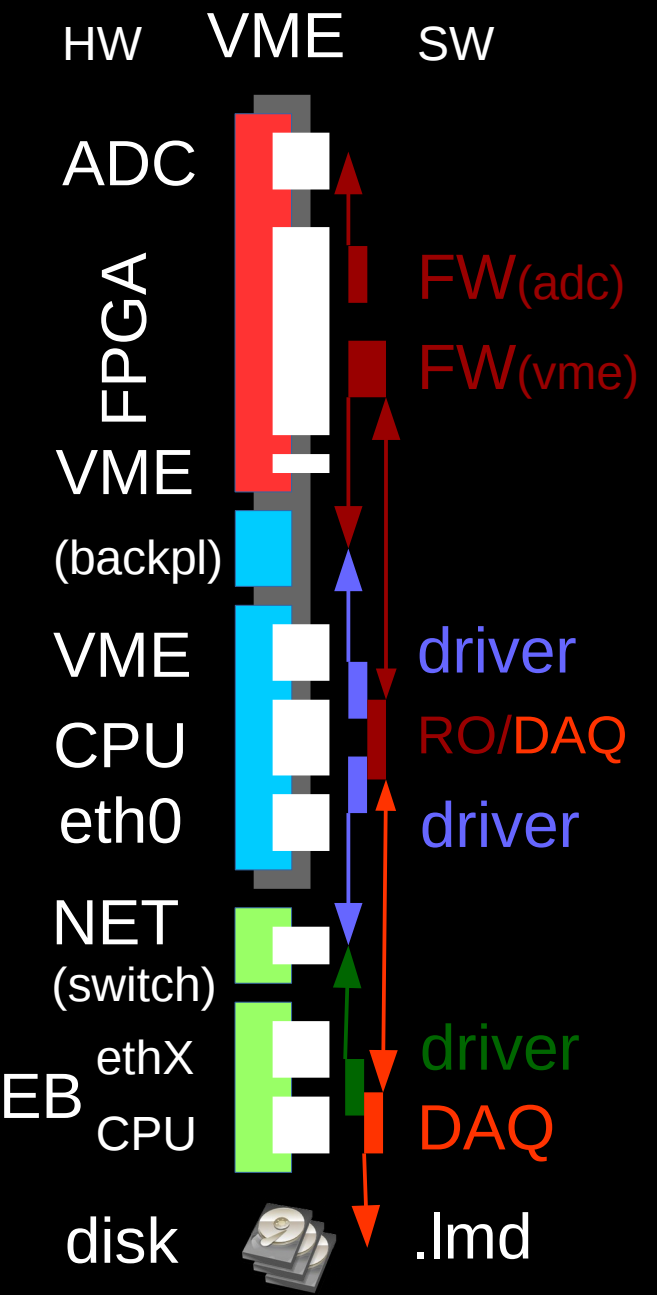
- To permanent storage

- (and online analysis)

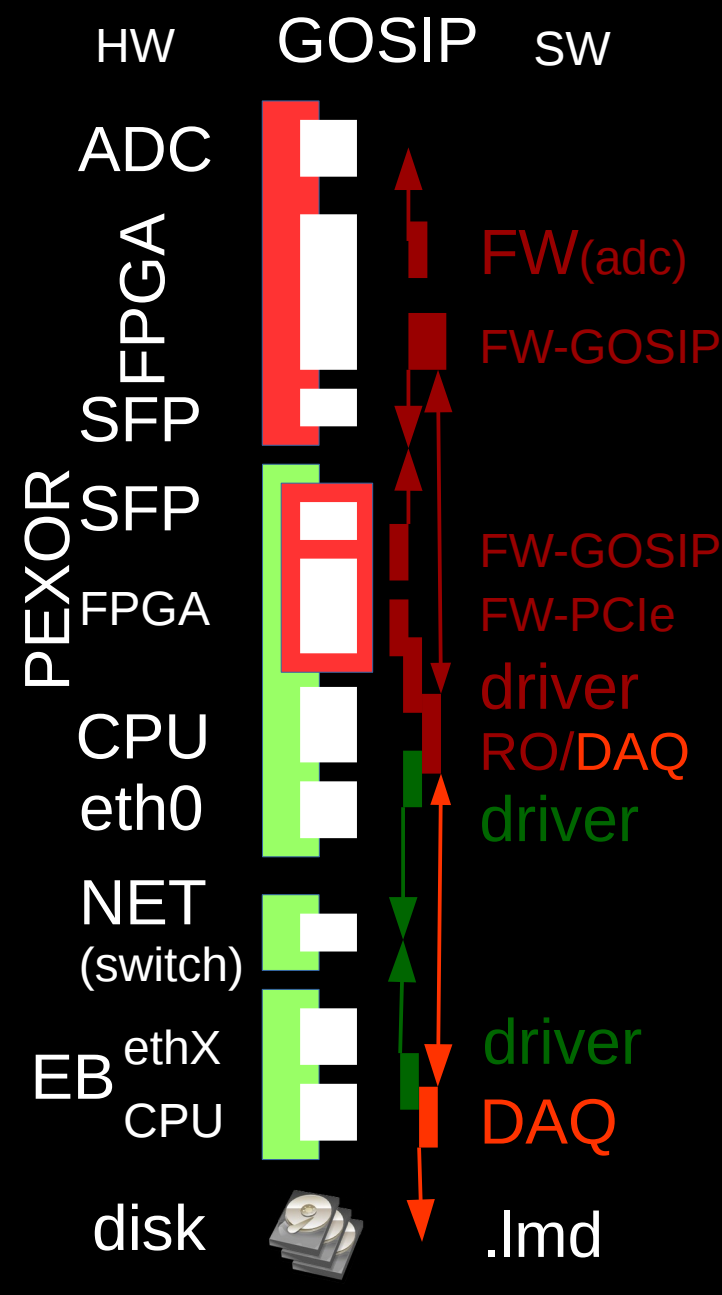
# Reaching network

"Classical system"

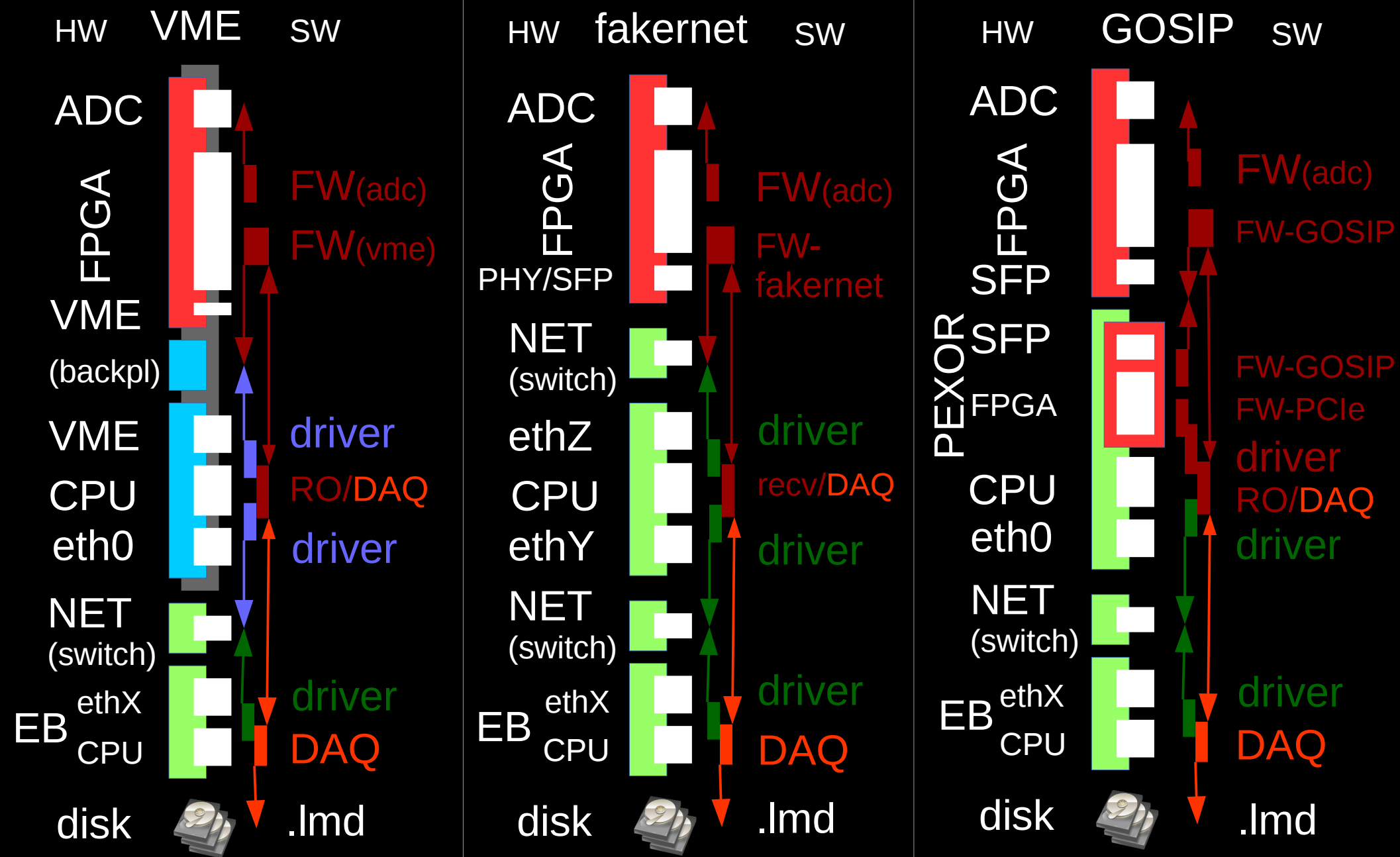
Example custom system  
Others e.g.: CAEN CONET



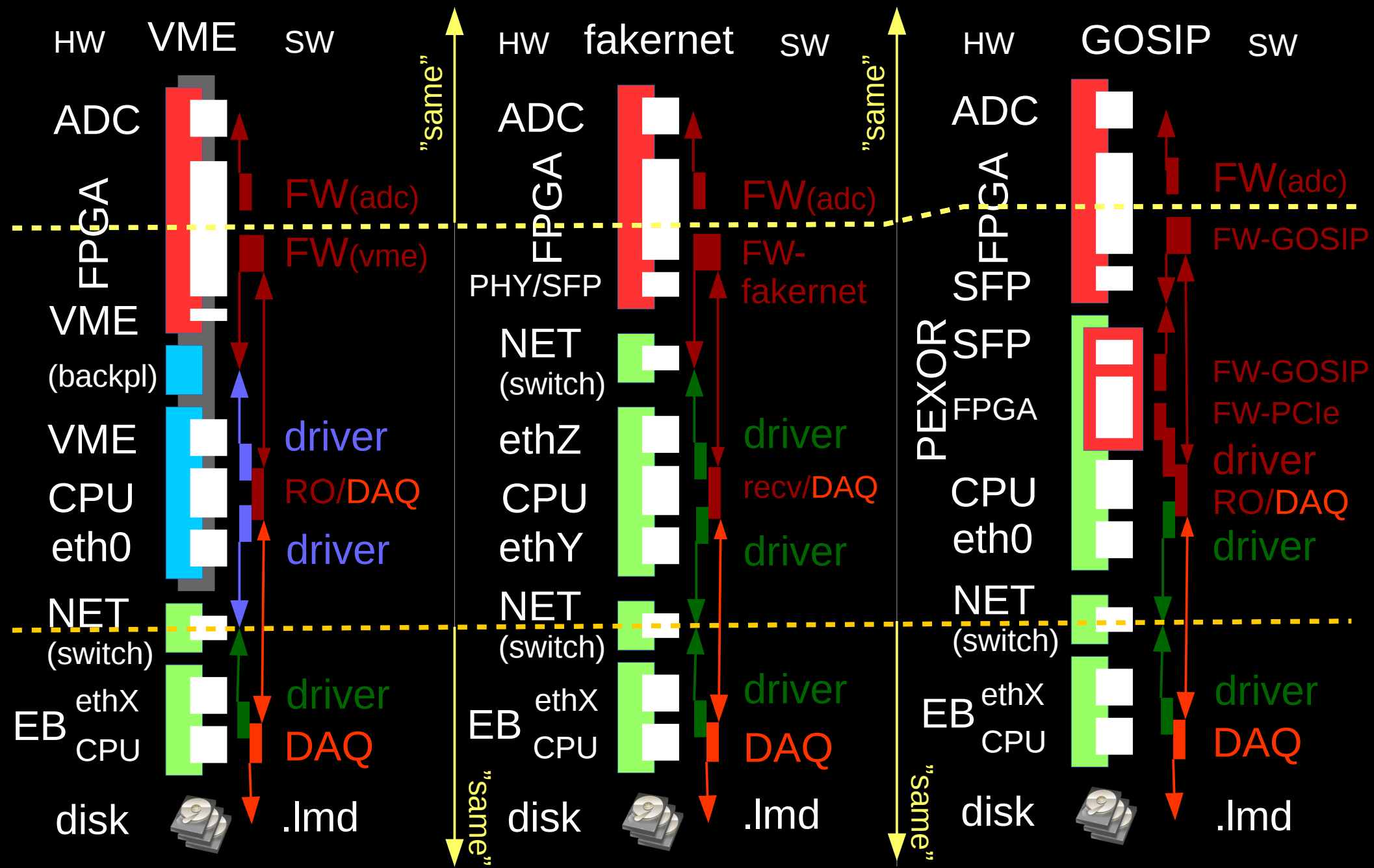
- Custom (board)
- Low-volume commercial (e.g. VME CPU board)
- Commercial (e.g. PC / switch)
- Custom firmware/software
- Common software
- Customized open-source (BSP packages)
- Generic open-source (e.g. GNU/Linux)



# Reaching network

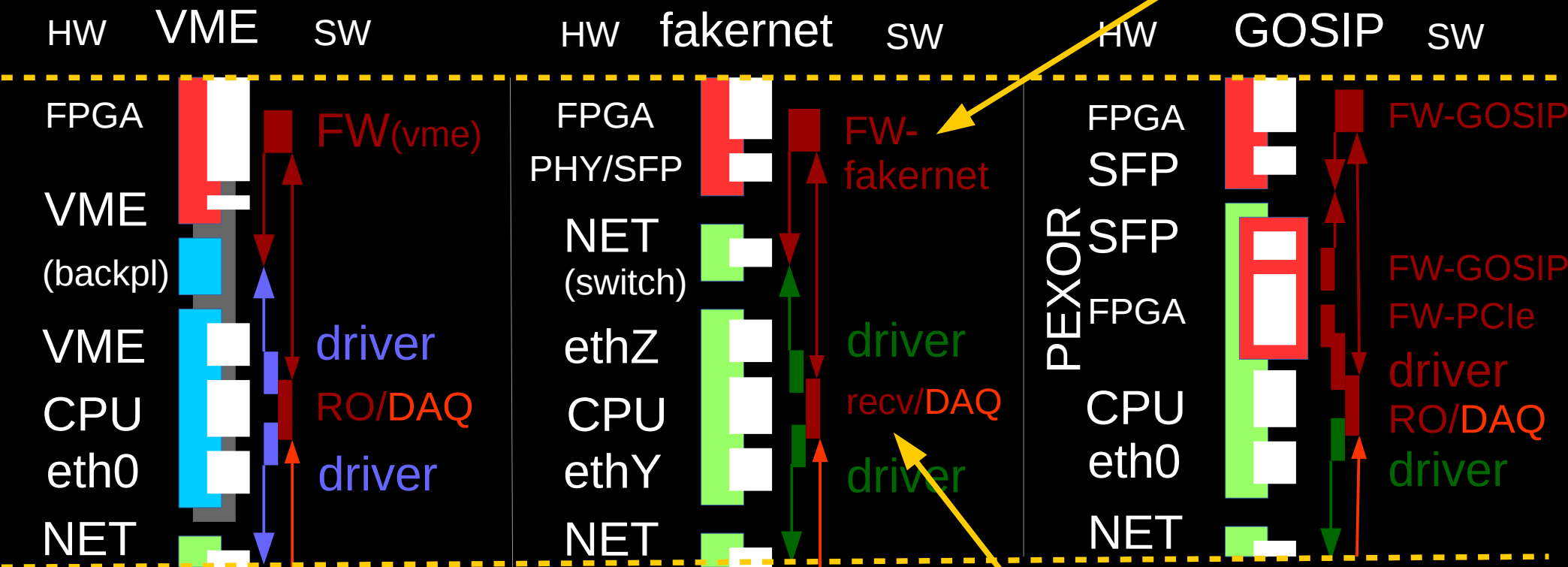


# Reaching network



# Reaching network

Fakernet  
VHDL...



- Custom (board)
- Low-volume commercial (e.g. VME CPU board)
- Commercial (e.g. PC / switch)

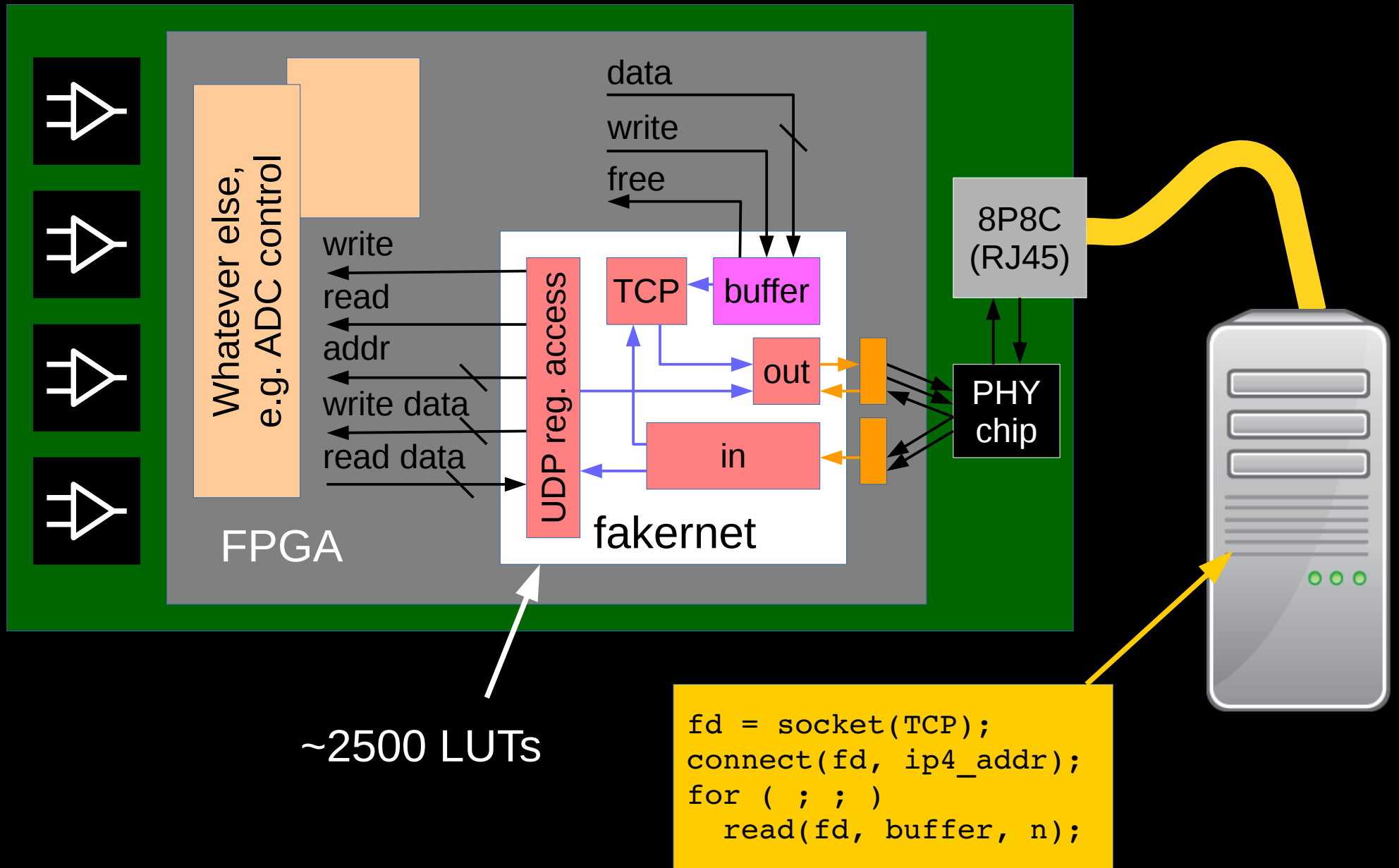
- Custom firmware/software
- Common software
- Customized open-source (BSP packages)
- Generic open-source (e.g. GNU/Linux)

```
fd = socket(TCP);
connect(fd, ip4_addr);
for ( ; ; )
    read(fd, buffer, n);
```

(Some simple C code.)



# Fakernet overview



# fakernet - Summary

- Data stream to TCP
  - @ line speed. (the VHDL code is > 1 Gbps-capable)
- Control access via UDP
  - 'Reliable' (by sequence counter)
- Directly to commercial network hardware
  - Private subnet—(not for generic network)
- Std. Ethernet & IP checksums from FPGA to CPU
- No special drivers
- ~ 2500 LUTs, needs PHY + 8P8C (RJ45) or SFP

100 Mbps  
tested with  
hardware

Comparison:  
VULOM4 has 20 kLUT

# fakernet - RST

- Data stream to TCP
  - @ line speed. (the VHDL code is > 1 Gbps-capable)
- Control access via UDP
  - 'Reliable' (by sequence counter)
- Directly to commercial network hardware
  - Private subnet—(not for generic network)
- Std. Ethernet & IP checksums from FPGA to CPU
- No special drivers
- ~ 2500 LUTs, needs PHY + 8P8C (RJ45) or SFP

Thank you!

and Philipp  
& Anders