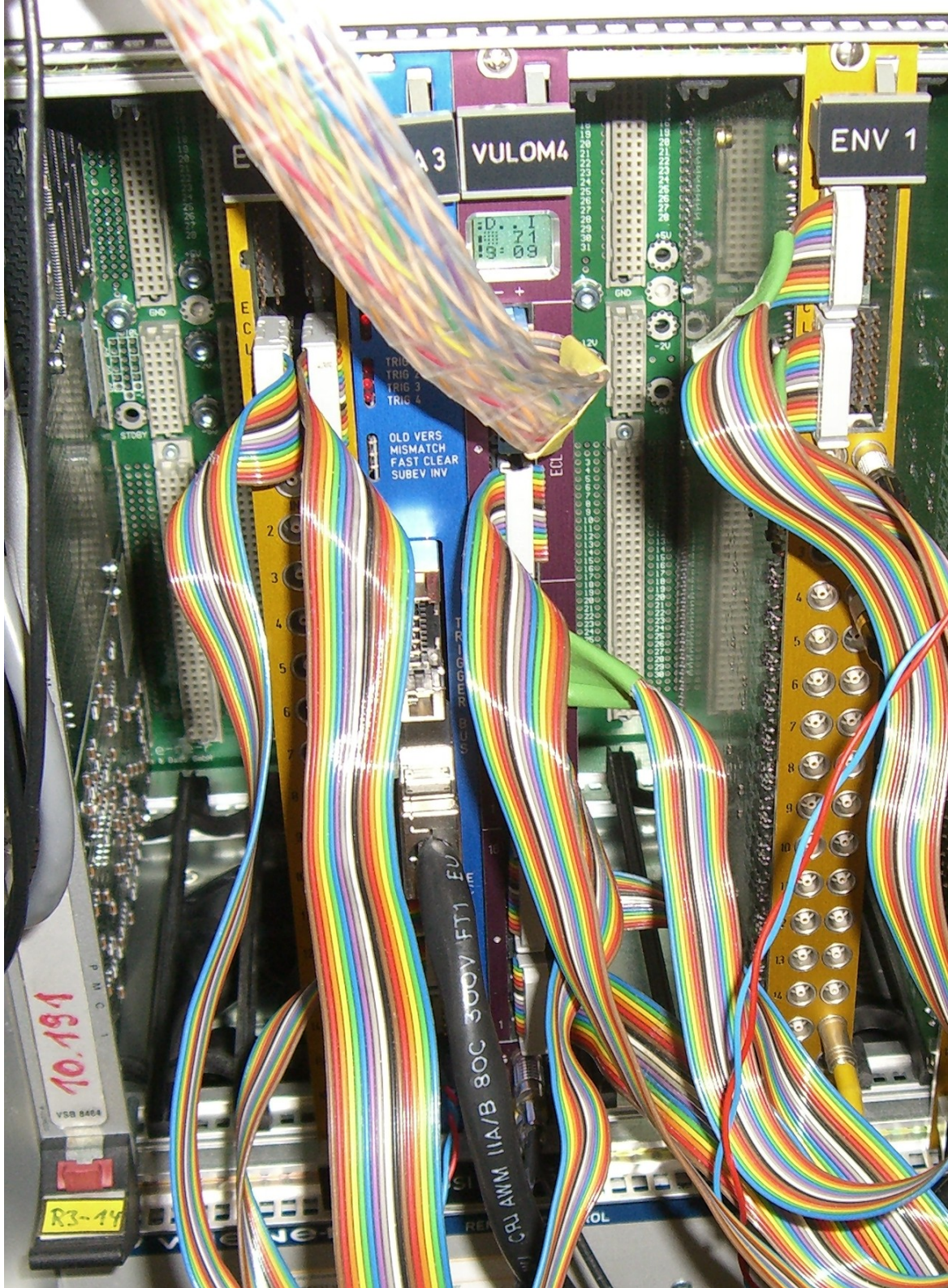
# TRLO II – now with TRIMI and serial timestamps v2

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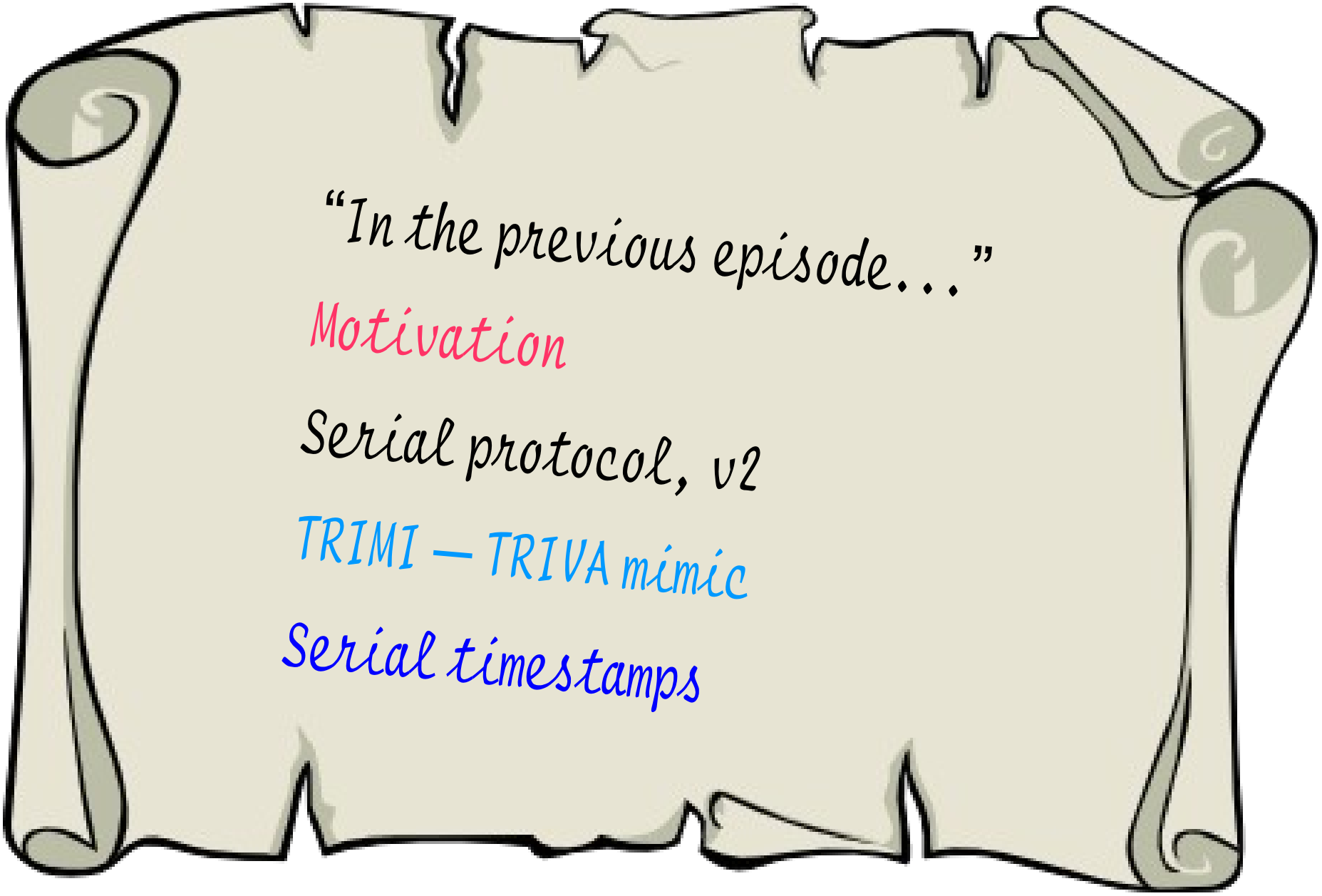
Chalmers, Göteborg

Liverpool, November 2013

# Outline:



"In the previous episode..."

Motivation

Serial protocol, v2

TRIMI — TRIVA mimic

Serial timestamps

# 2012: Trigger bus Cave C → S2 ?


Unexpected problem:

Trigger bus lost signal integrity Cave C → S2 (ground levels)

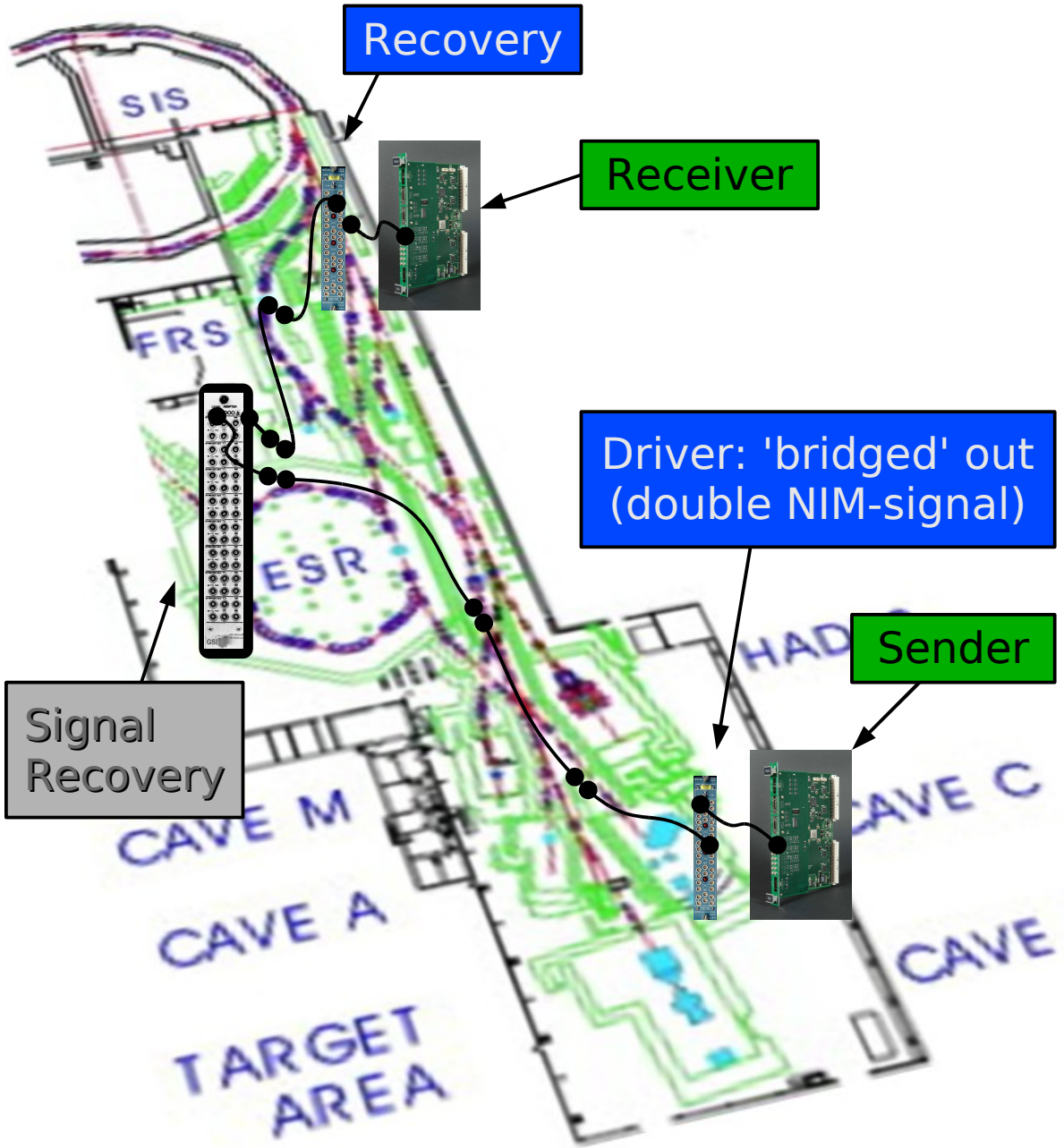
=> Common dead-time domain
with TRIVA @ S2 not possible.

=> Time-stamp distribution with TITRIS modules not possible.
(uses same type bus cable)

2012: Time-stamp distribution with two spare TRIDI1 modules and TRLO II. Using 'any' cable.

Timestamps Cave C → S2 !

# 2012: Serial timestamps Cave C - (FRS) - S2




Features for easy deployment:

- Uni-directional protocol
- 1 cable of 'any' kind
- (a trigger also needed) ($2^{nd}$ cable)
- No 'initialisation' - easy setup:

  1. Start sender,
  2. Follow signal (scope),
  3. Receiver auto-sync

- Loss of ≤ 3 protocol cycles → still in sync

# 2012: S406 systems

EB
x86g-10

x86g-71
TO

EB
x86-36

POS/ROLU
r4-10

NTF/DTF/CXB
r4-35

r4-46
RPC

r3-15
LAND

r3-14

r3-52
Si

r4-12
XB(l)

MASTER

r3-30
NeuLAND

Coimbra
RPC

"S2" (master)

r4-43

x86-63
MFI

r4-11
XB(r)

Object-oriented DAQ - several:
- Dead-time domains
- Time-stamp protocols

München
CsI

r4-28
$LaBr_3$

TRIVA / TRIXOR
trigger bus
VULOM
TRIDI

DAQ setup: D. Rossi, H. Simon

# 2012: Main DAQ

EB

x86g-10

x86g-71

TO

POS/ROLU

NTF/DTF/CXB

r4-10

r4-35

r3-15

LAND

r3-14

r3-52

Si

r4-12

XB(l)

MASTER

r3-30

NeuLAND

r4-11

XB(r)

Trigger bus pains:

- fault here →
- problem there.

(trigger mismatch → DAQ crash)

"Don't get me wrong:"

# The TRIVA is great!

[VME Trigger Synchronisations Modul]


TRIVAx robustness

MBS:
- Uncompromising event synchronisation
- Stability

Lately, some scalability issues:

- Trigger bus cable at long distances?
- Rapid reconfiguration of multi-branch system
  (slave addition and removal during experiment setup)

Any alternative needs to be as stable...

# TRLO II TRIVA mimic 'bus': Plan

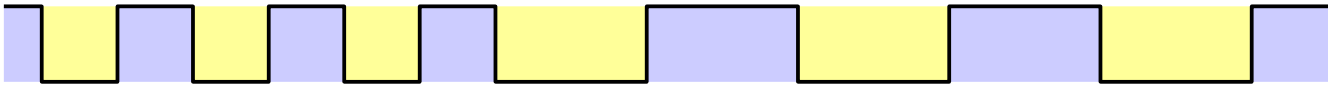
- Serial protocol → Minimise cable needs.
  → 'Any' cable type. Including optical.
- Unidirectional → Easy deployment – autosync.
  → Support tree-like cable arrangement.

(Deadtime return also needed.)
(Simple 'OR' enough; with VULOM as fan-in → individual monitoring.)

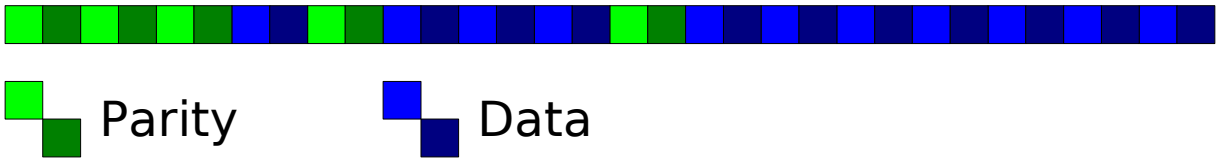
- Backwards compatible. (VME register space) → Use MBS unchanged.
- Clock frequency independent. → Usable on other boards with FPGA/CPLD control.
- Aux. software messages. → Insert subsystems on-the-fly.

# Serial protocol

- Pulses 0 or 1 .
  50 % 1s, 50 % 0s.

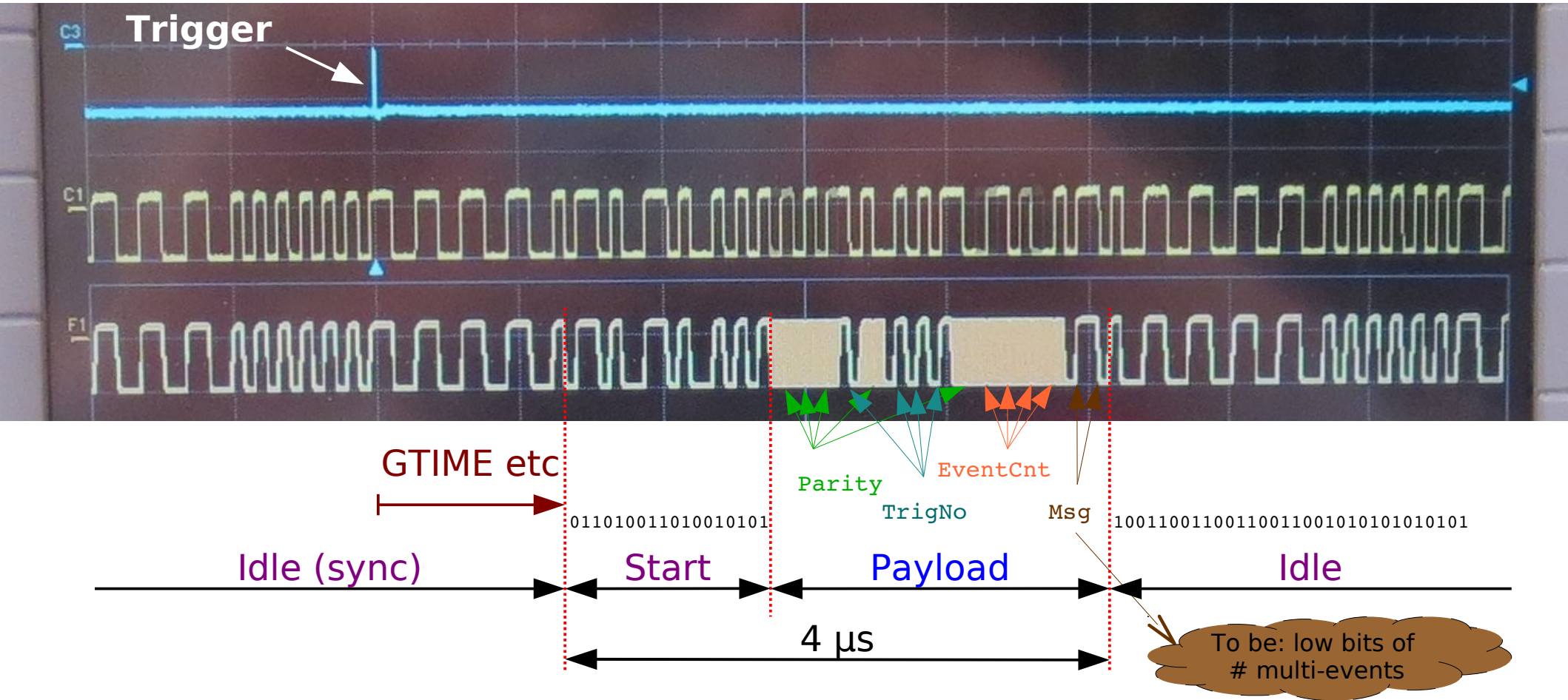


- Each payload bit sent as two pulses; second inverted.
- Never more than two same (1 or 0) in a row.
  → never more than 4 slots between same edge.
  (Used for first rough frequency lock.)
- Receiver: phase and frequency tracking.
- Special (idle) patterns for synchronisation.
  → Automatic inversion handling.
- Payload forward error correction: [16,11] Hamming Code
  → together with bit duplication: 3-bit errors correctable.

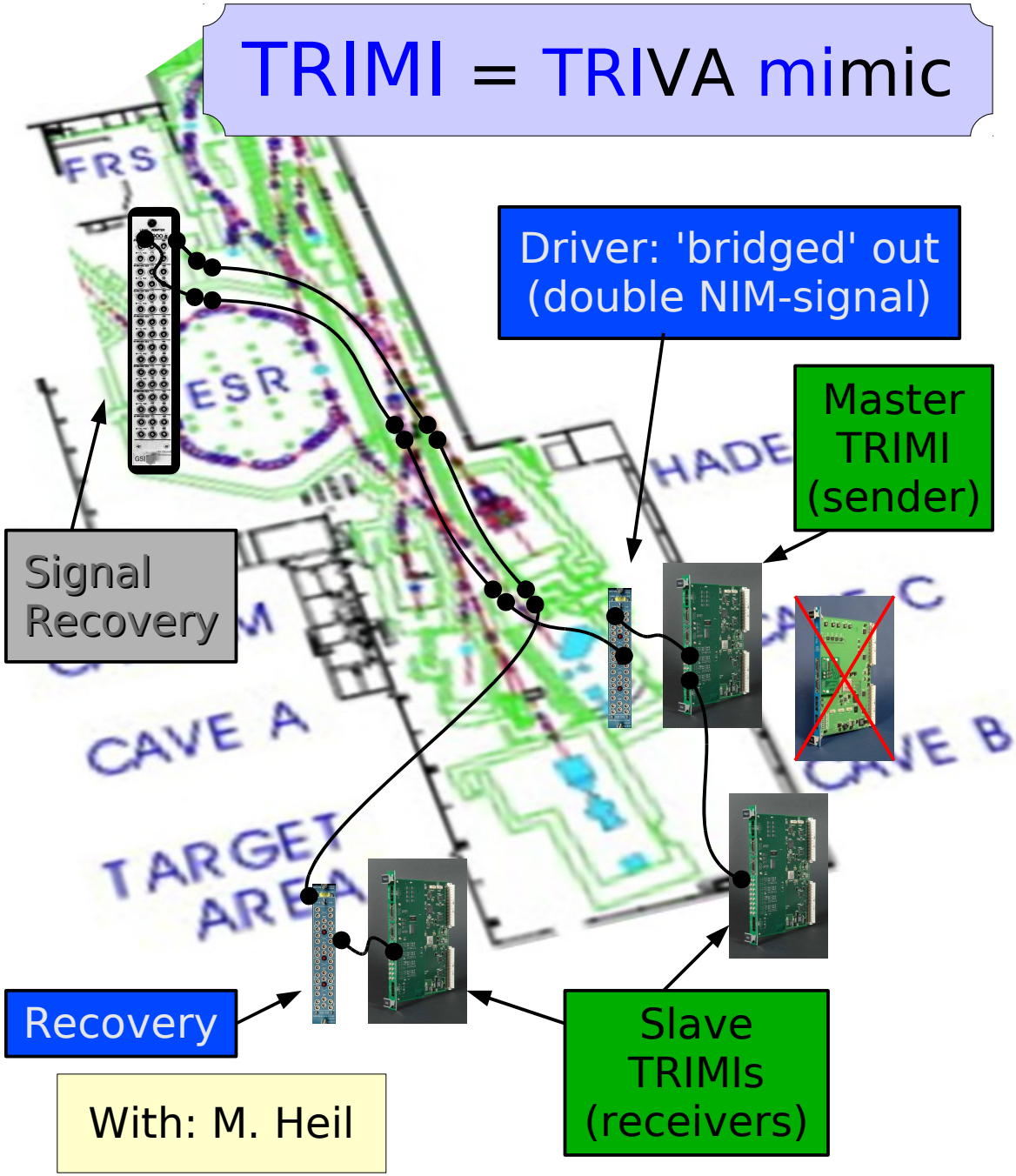


# TRIMI protocol

- Continous idle pattern (→ recv. freq./phase sync)
- Trigger payload after start pattern
- Other header pattern for reset and software message (8 bits)

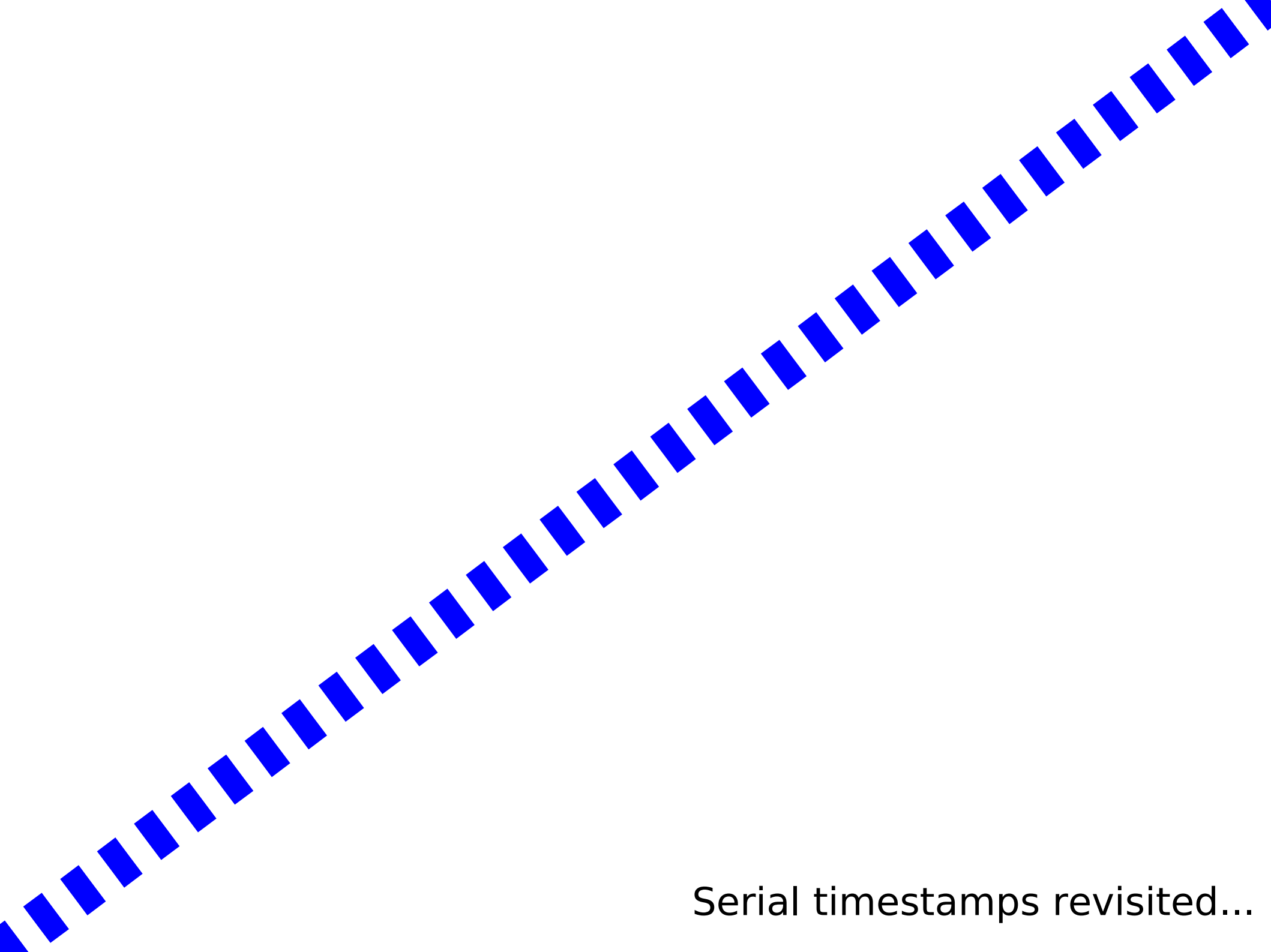


# Serial trigger test Cave C - (FRS) - Cave C

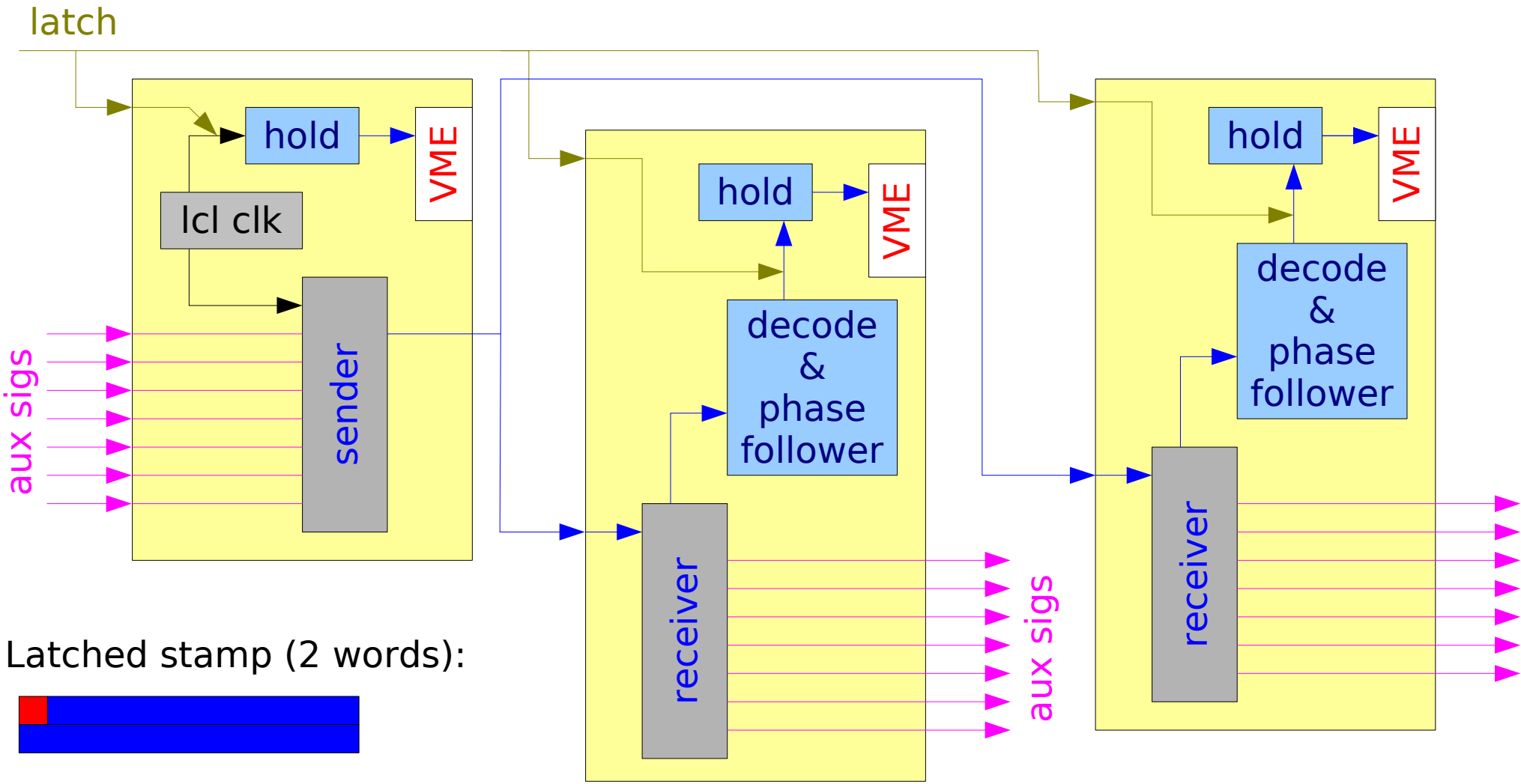



Easy deployment:

- Uni-directional protocol
- 1 cable of 'any' kind
- (DT return also needed) ($2^{nd}$ cable)
- No 'handshake' startup - easy setup:
  1. Start sender,
  2. Follow signal (scope),
  3. Receiver auto-sync ('any' frequency)
- Loss of ≤ 3 bits/msg → error-correction


Serial timestamps revisited...

# Serial timestamps with mux




Latched stamp (2 words):

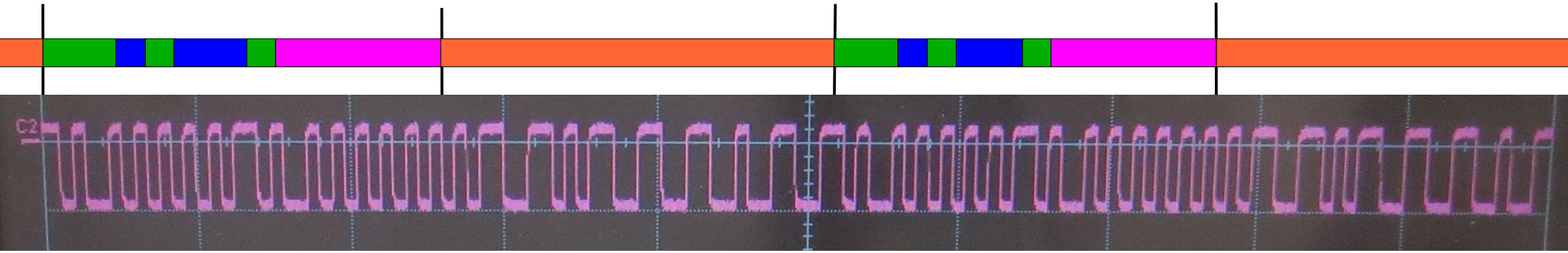


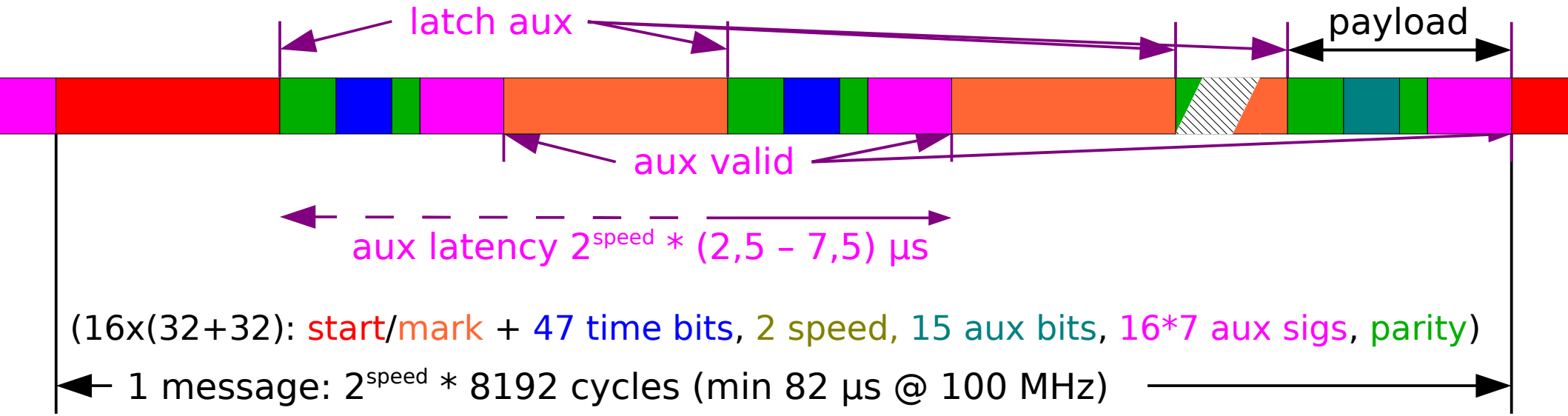
- synchronised?
- time of latch

Simplified from previous version. No CPU-side post-processing.

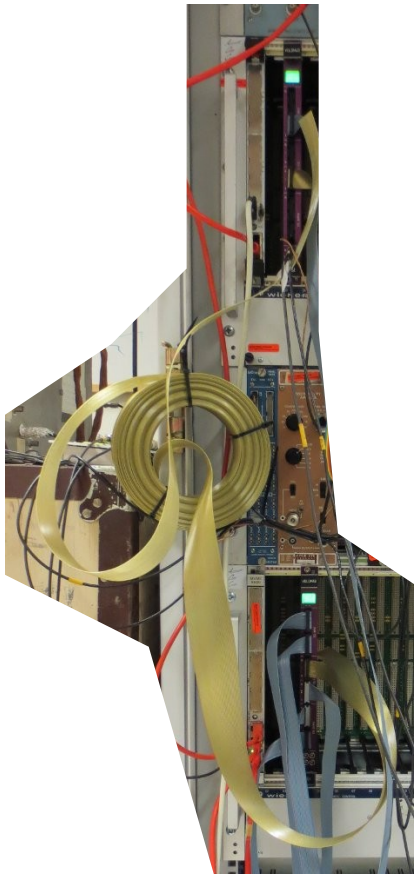
# Serial timestamp protocol

- Continous bitstream (→ recv. freq./phase sync)
- Each payload has 7 aux signals and 4 bits of time, 5 parity
- Header pattern for sync, different before first payload

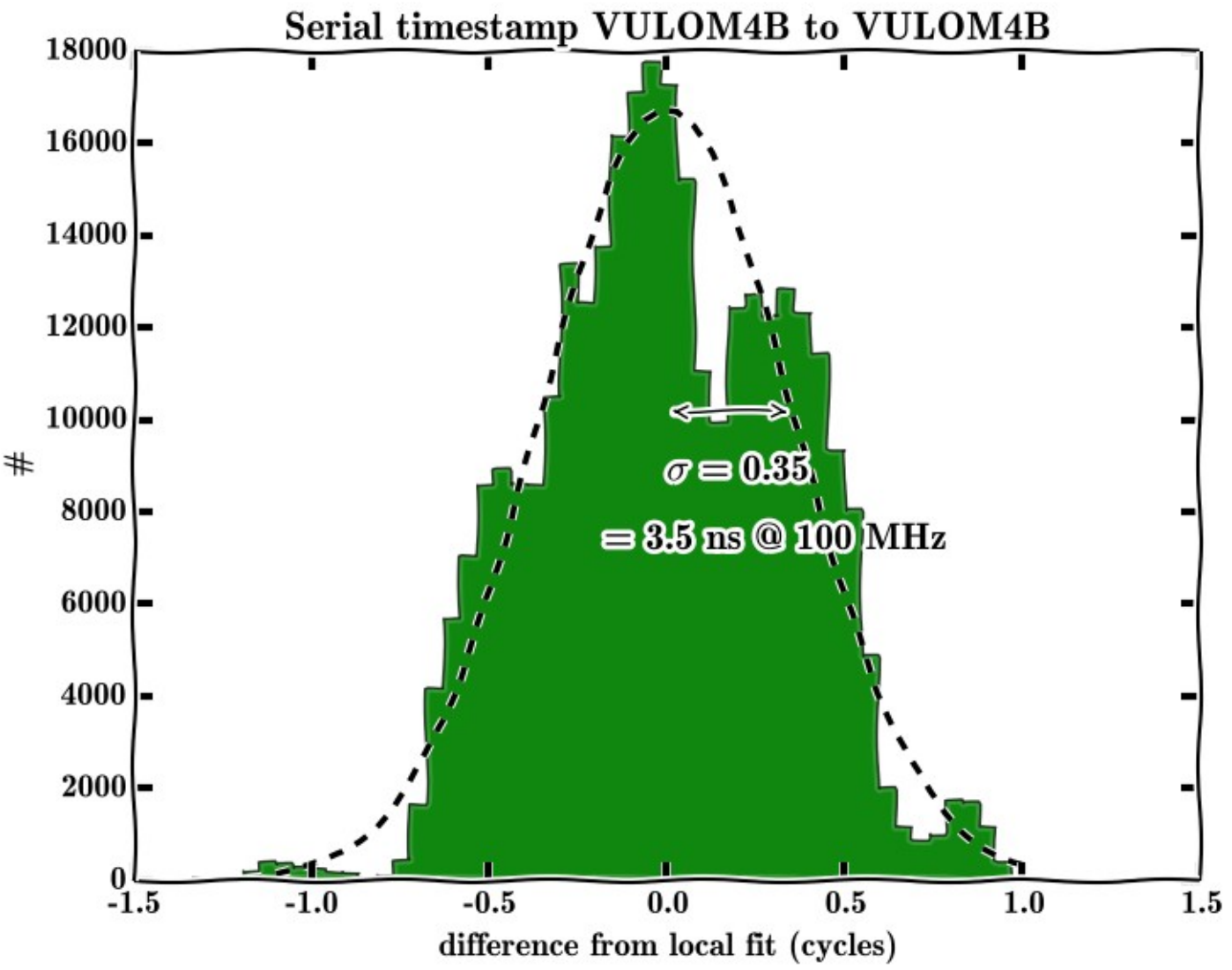




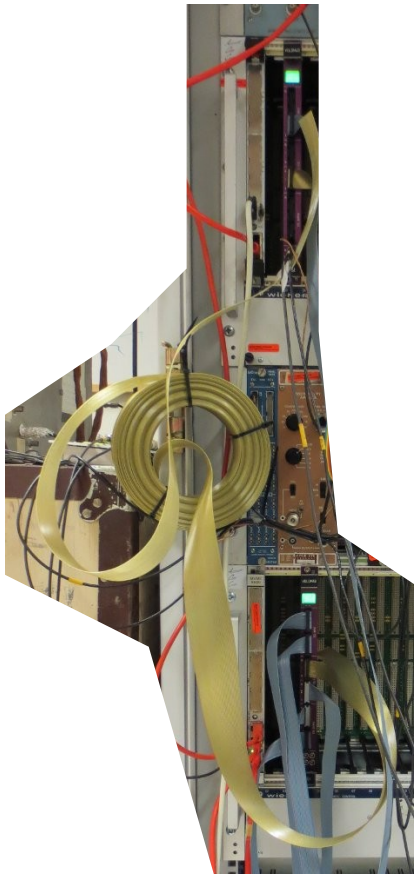
# Serial timestamp precision

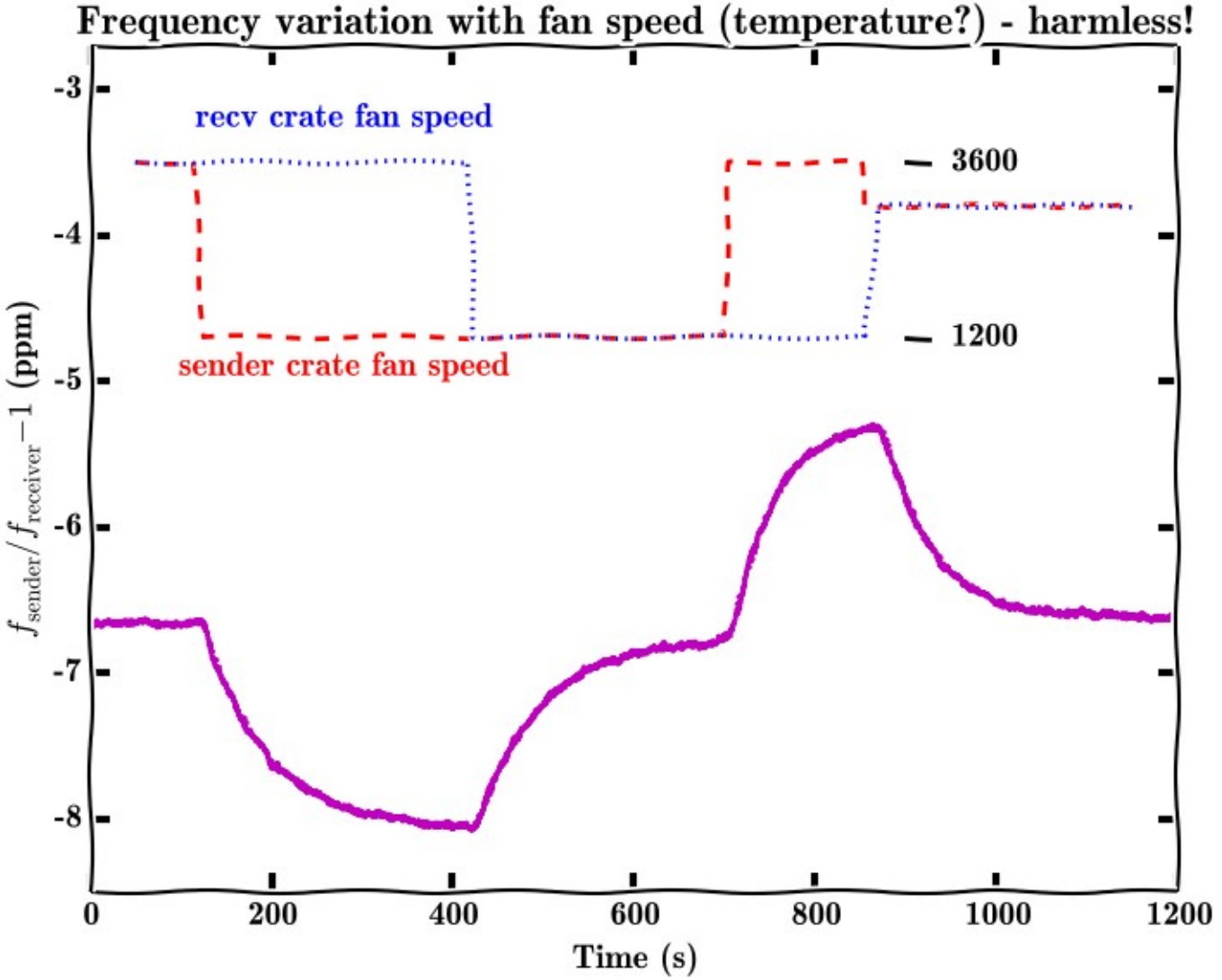


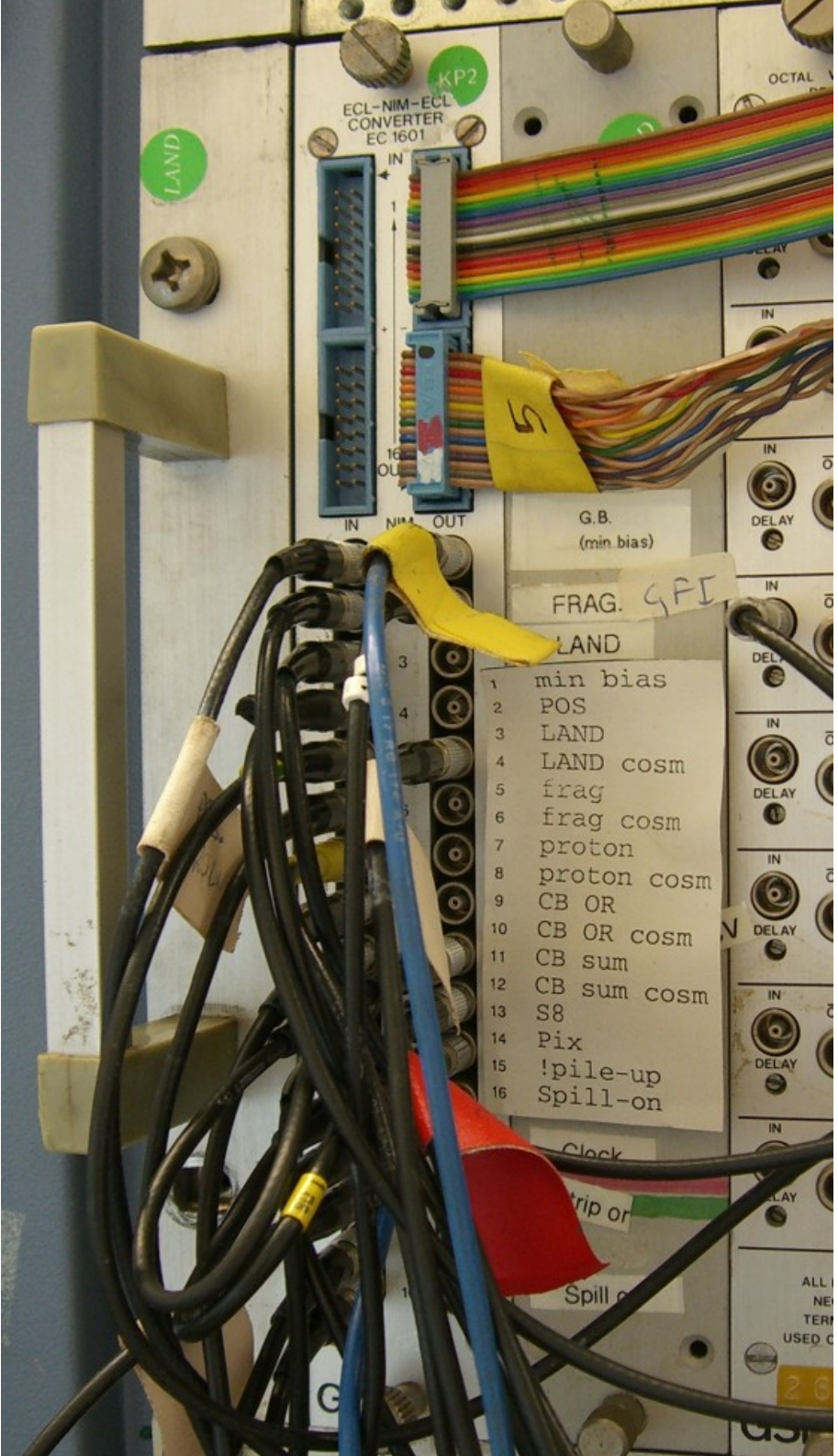
Humps due to receiver following signal by ± 0.5 local clocks?



# For FUN – oscillator vs. oscillator






# Finale!

# Thank you!

With thanks to: J. Hoffmann, J. Frühauf, W. Ott, N. Kurz, H. Simon, A. Henriques, M. Heil, B. Löher, A. Charpy, C. Forssén...

FPGAs are FUN!

- although getting the v2 serial messages to work has been a loooong...

http://fy.chalmers.se/~f96hajo/trloii/

Live by the compiler timing messages!