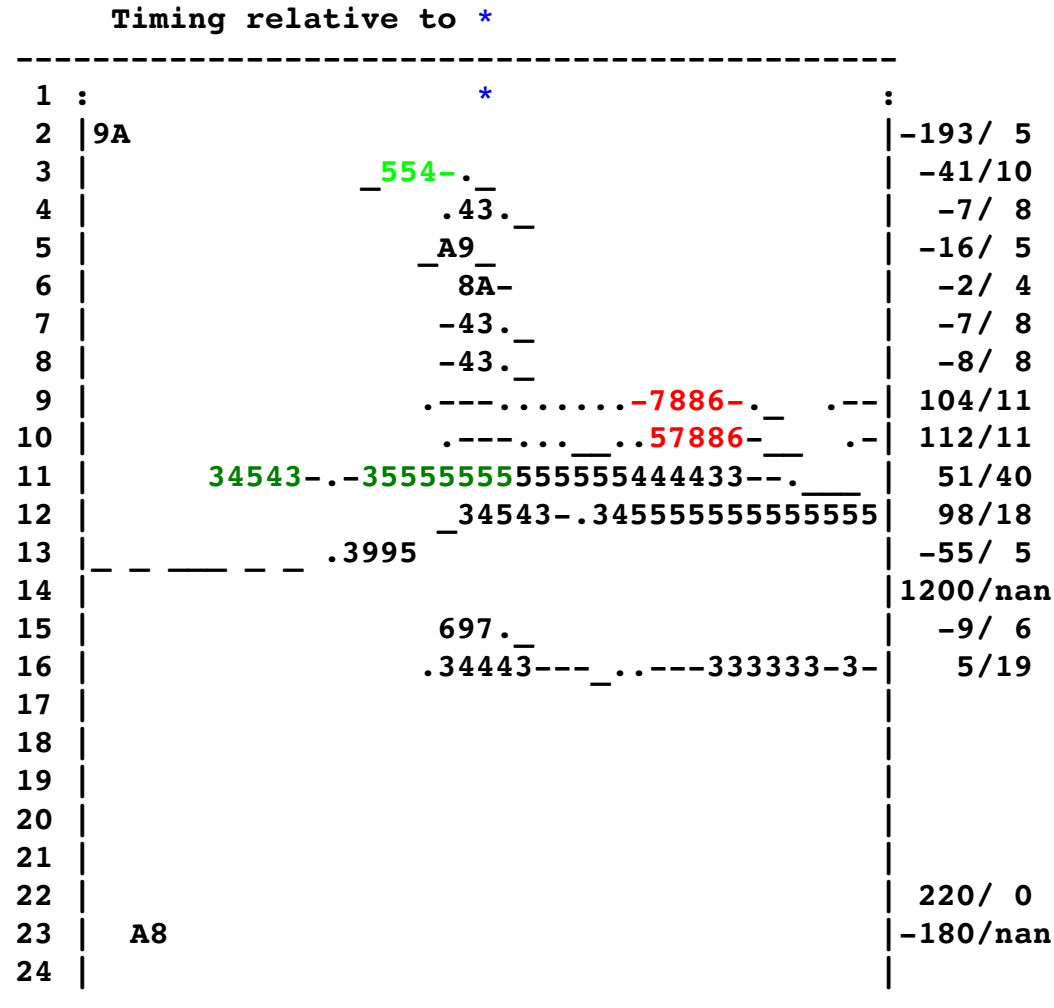


# TRLO II – flexible FPGA trigger control

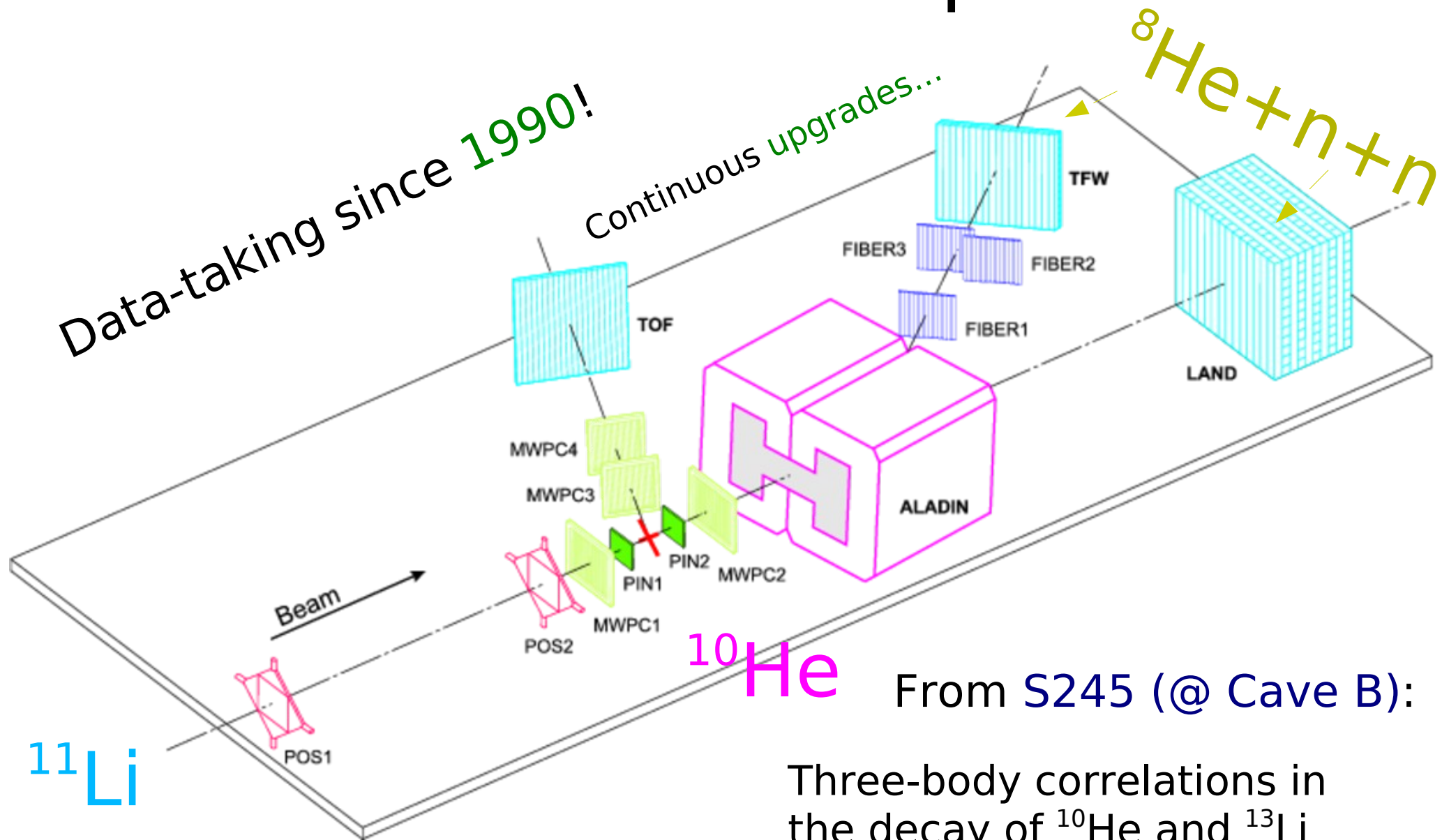


Håkan T. Johansson, Chalmers, Göteborg

With Ana Henriques, Lisbon

Lund, October 2010

# ALADiN-LAND setup → $R^3B$



From S245 (@ Cave B):

Three-body correlations in the decay of  $^{10}\text{He}$  and  $^{13}\text{Li}$

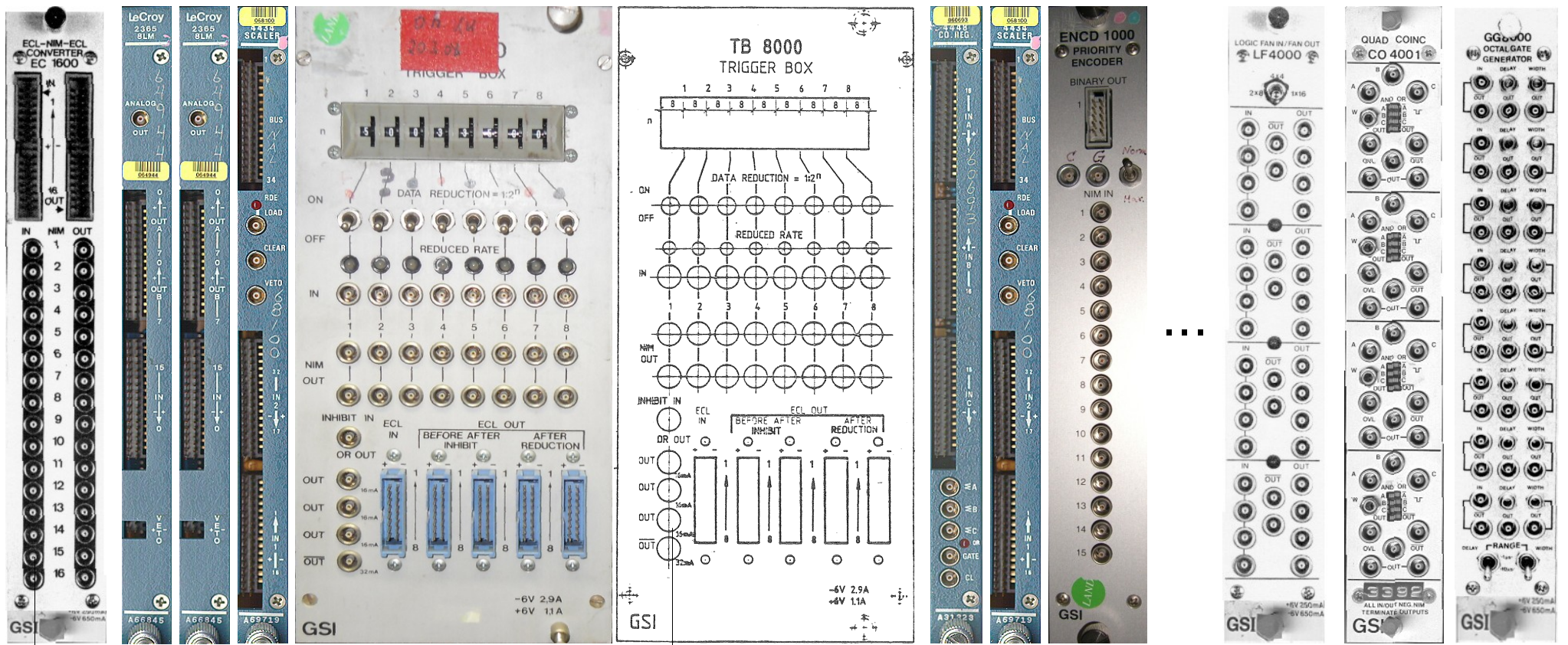
H.T. Johansson, Yu. Aksyutina, et. al.  
Nuclear Physics A, Vol 847 (2010) pp. 66-88

# The trigger has to be *fast*...

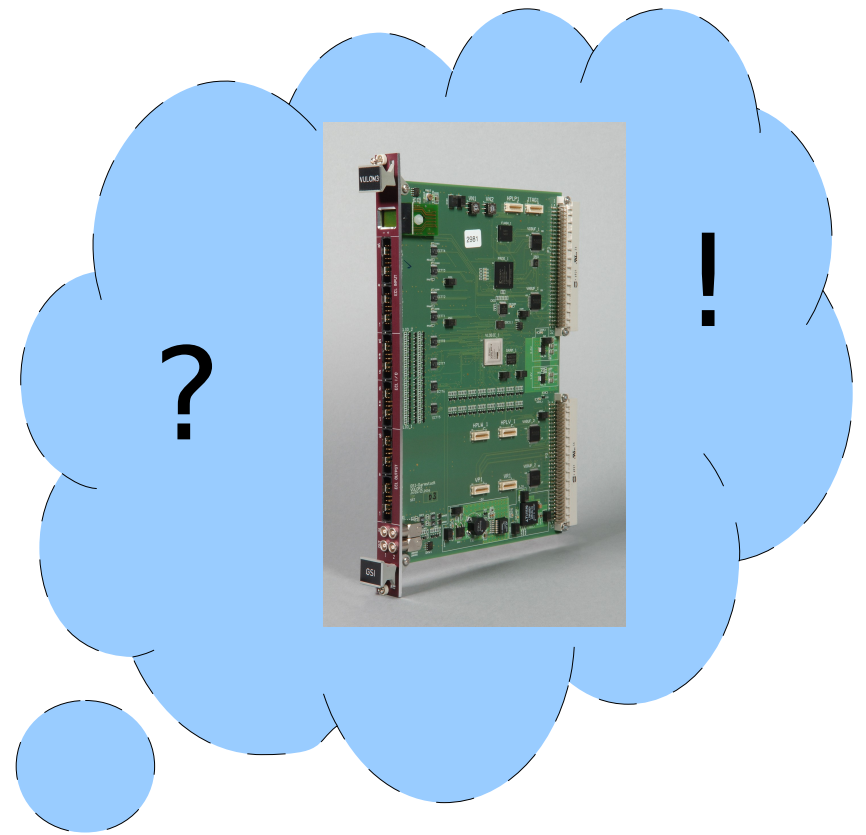
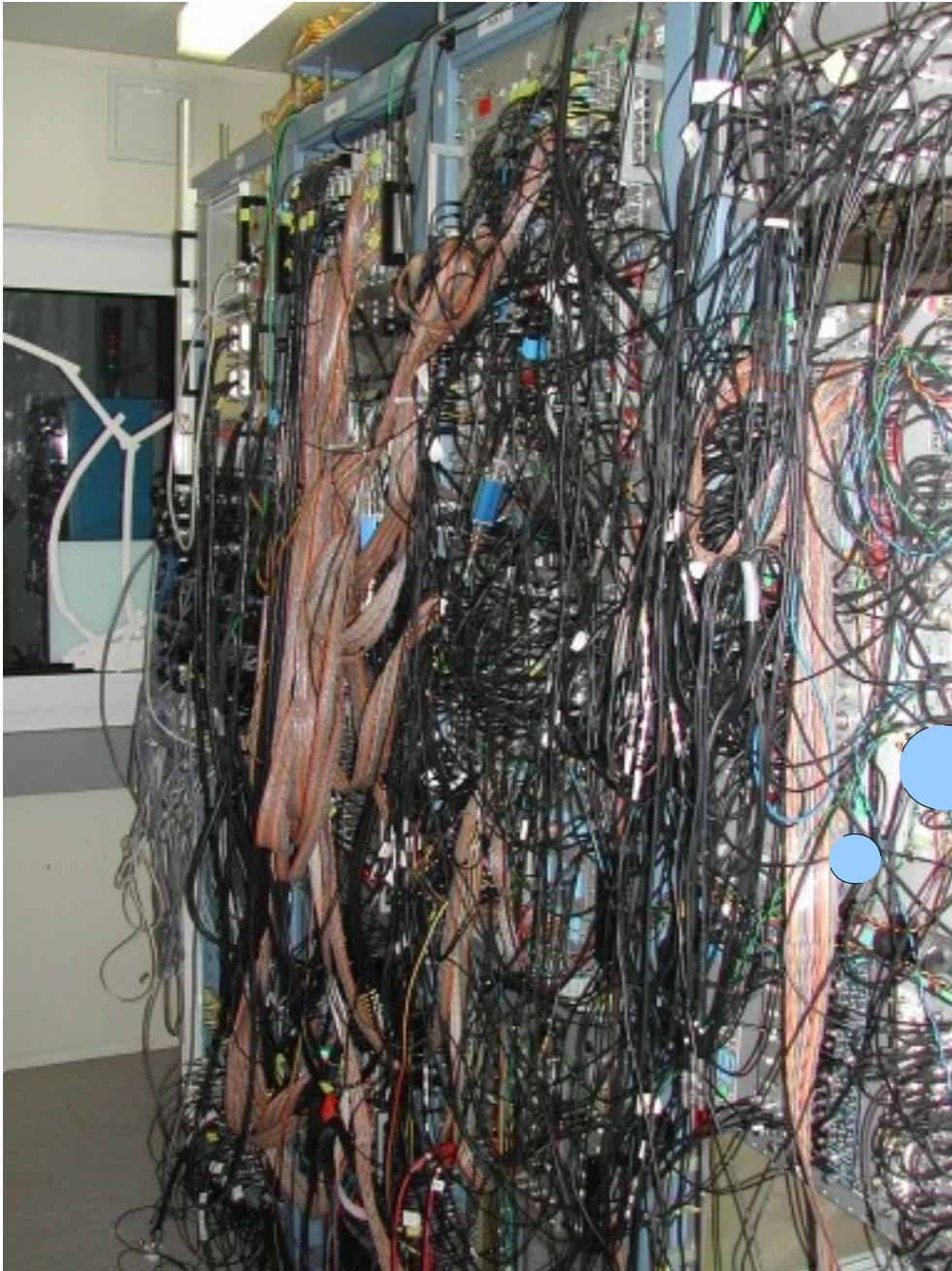
Detector signals  
 Logic matrix  
 → coincidences  
 Scaler

Trigger boxes:  
 deadtime veto  
 downscale

Pattern unit  
 Scaler  
 Priority encoder



Master start in 45 ns



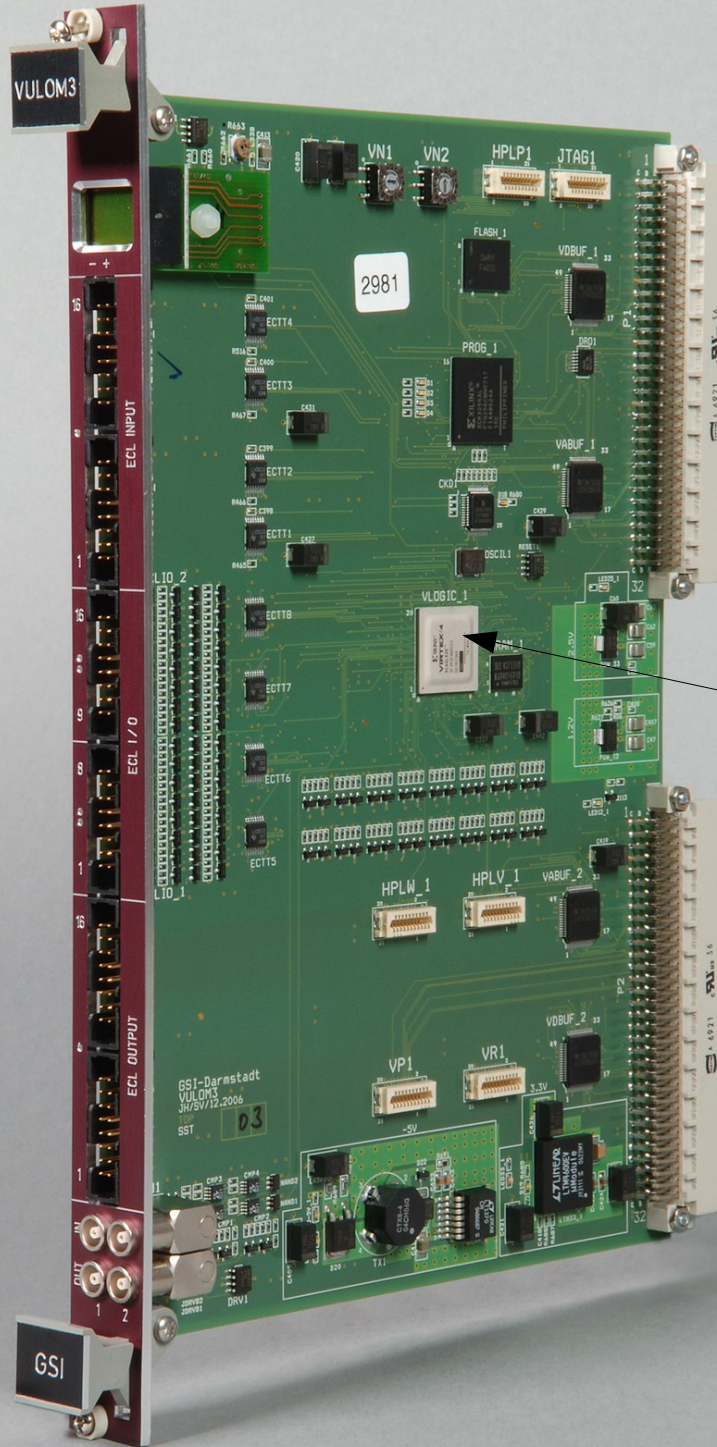
VULOM  
(VME universal logic module)

by J. Hoffmann, **GSI**

Original TRLO firmware  
by J. Frühauf, **GSI**

Inputs

Outputs



VME

FPGA

# Fast-path: detector signals → master start

Timing-critical  
trigger decision

All logics: 100 MHz (10 ns)

Decision in 2 **clock cycles**:

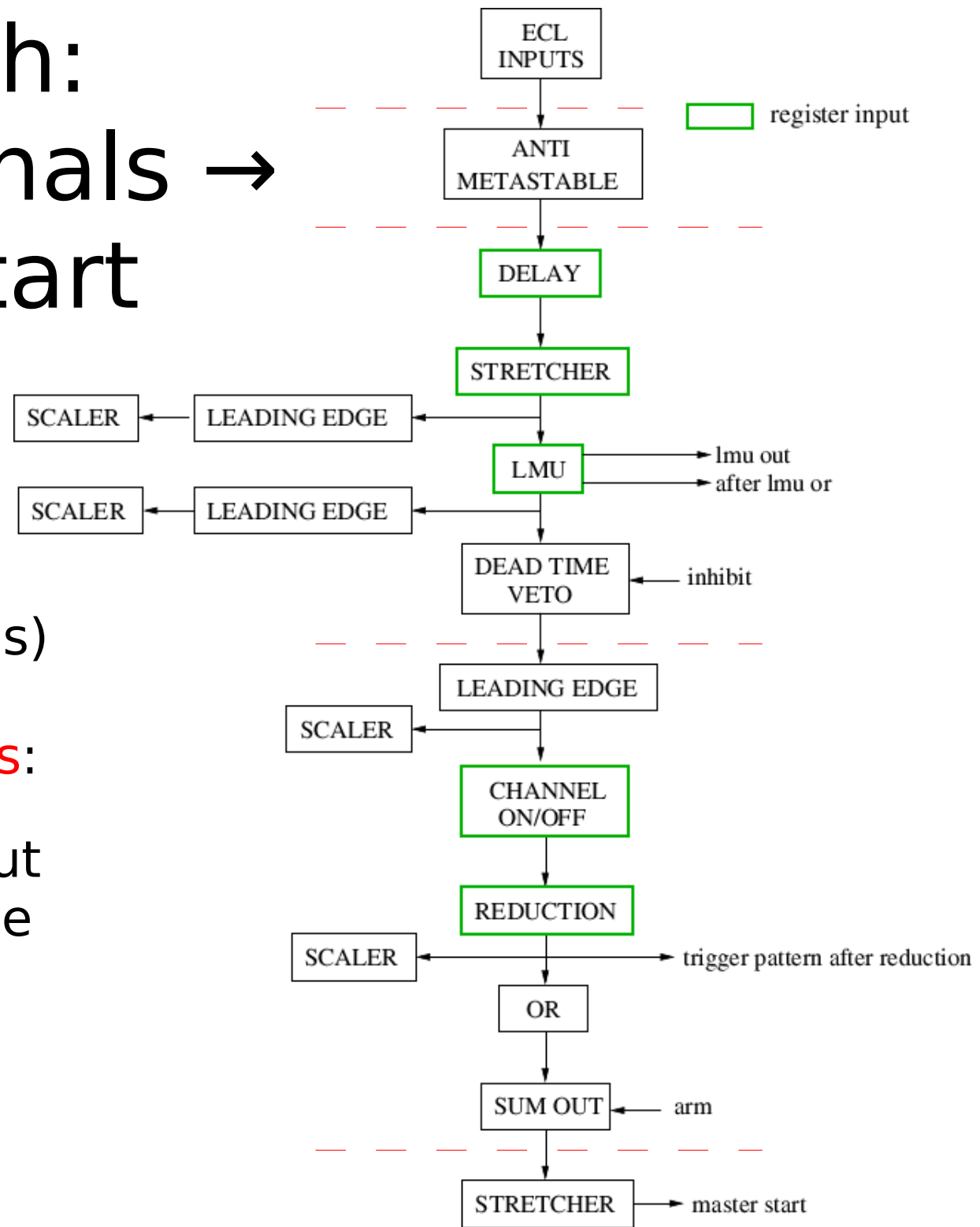
18 ns: module in + out

5 ns: anti-metastable

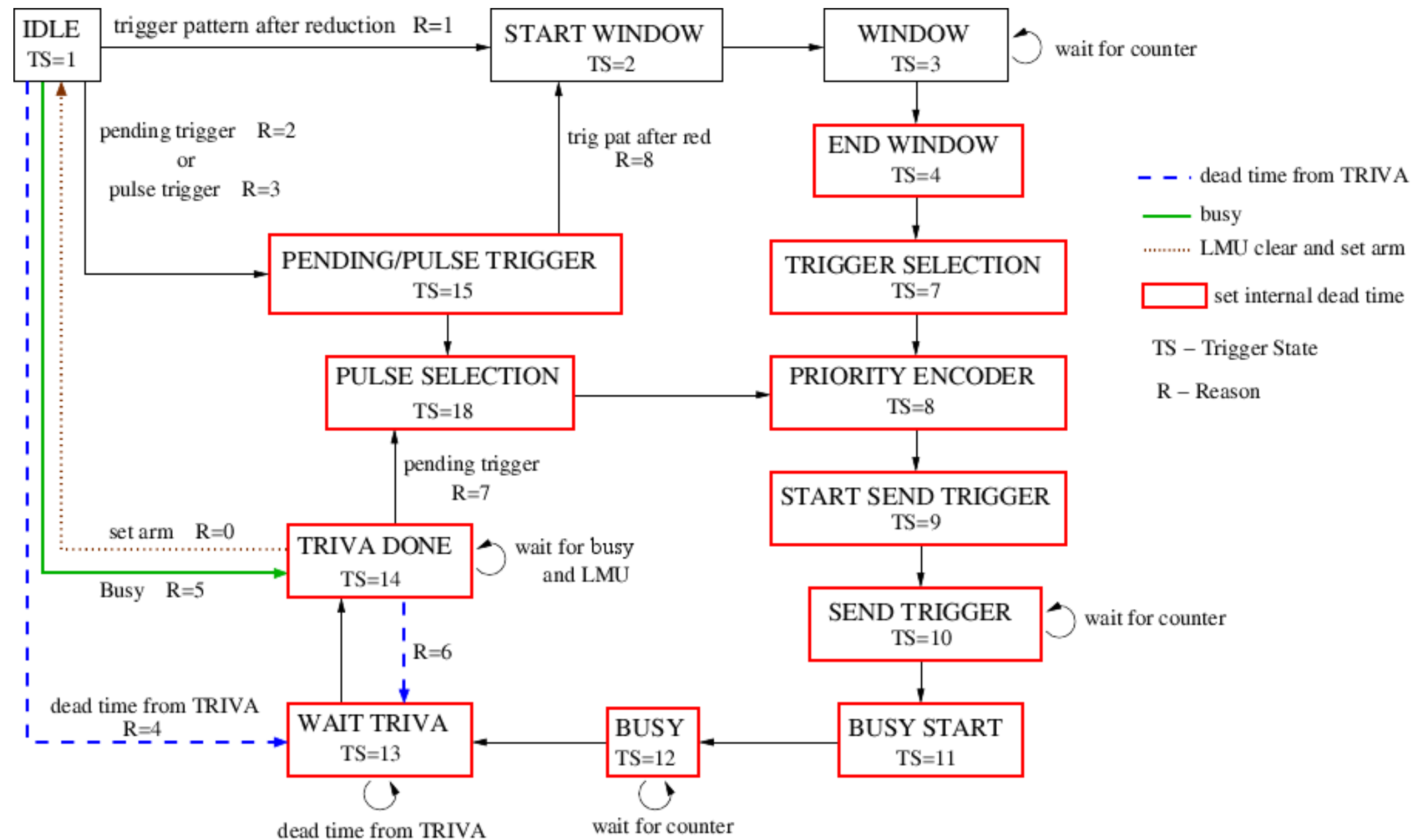
20 ns: decision

10 ns: clock jitter

45-55 ns: master start



# Trigger state machine



# Stable VME interface definition

VME registers as C structure,  
with named entries,  
generated by compilation

Version number is MD5  
of full VHDL code

Named constants

Setup registers in block  
RAM for readback.

Aggressive checksumming  
of output data.

```
#define TRLO_MD5SUM_STAMP                0xccb60dee

// Constants for 'direct_mode':

#define TRLO_DIRECT_MODE_LOGIC           0x0
#define TRLO_DIRECT_MODE_DIRECT         0x1
#define TRLO_DIRECT_MODE_LOGIC_OR_DIRECT 0x2

typedef struct trlo_output_map_t
{
    /* 0 0x0000 */ uint32_t version_md5sum;
    /* 1 0x0004 */ uint32_t compile_time;
    /* 2 0x0008 */ uint32_t timing_tick;
    /* 3 0x000c */ uint32_t deadline_tick;
}

typedef struct trlo_setup_map_t
{
    /* 0 0x2000 */ uint32_t mux[122];
    /* 122 0x21e8 */ uint32_t direct_mux[26];
    /* 148 0x2250 */ uint32_t direct_mode[26];
    /* 174 0x22b8 */ uint32_t direct_or[3];
    /* 177 0x22c4 */ uint32_t scaler_mode[8];
}

// MUX src indices:

#define TRLO_MUX_SRC_ECL_IN(i)           ( 0+(i))
#define TRLO_MUX_SRC_ECL_IO_IN(i)        (16+(i))
#define TRLO_MUX_SRC_LEMO_IN(i)          (24+(i))
#define TRLO_MUX_SRC_WIRED_ZERO          (32)
```



# General logic

- **Pulsers** (programmable frequency).
- **PRNG** (pseudo-random sequence).
- **LMU** (not the same as in fast-path).
- **Downscale**.
- **Delay** and **stretch** (a.k.a. gate-and-delay).
- **Edge-to-gate** conversion (e.g. spill mimic).
- **Fan-in** (masked all-or).
- **Coincidence**.

# Monitoring

- **Scalers**. Latched 32-bit with selectable input.  
Hybrid **flip-flop** / **block RAM** -> **few resources**. (25 ff/ch)
- **Timer latches** (latch global timer on a signal edge).
- **Multi-entry buffer** for the **timer-latches**.  
Block **RAM fifo**.
- **Self-triggering soft-scope**.  
Block **RAM circular recording**. Block **RAM multi-trace fifo**.
- Input **pattern latch**.
- Front-panel **LEDs**.
- Front-panel **display**.



# Multiplex everything!

Any signal destination can use any source.

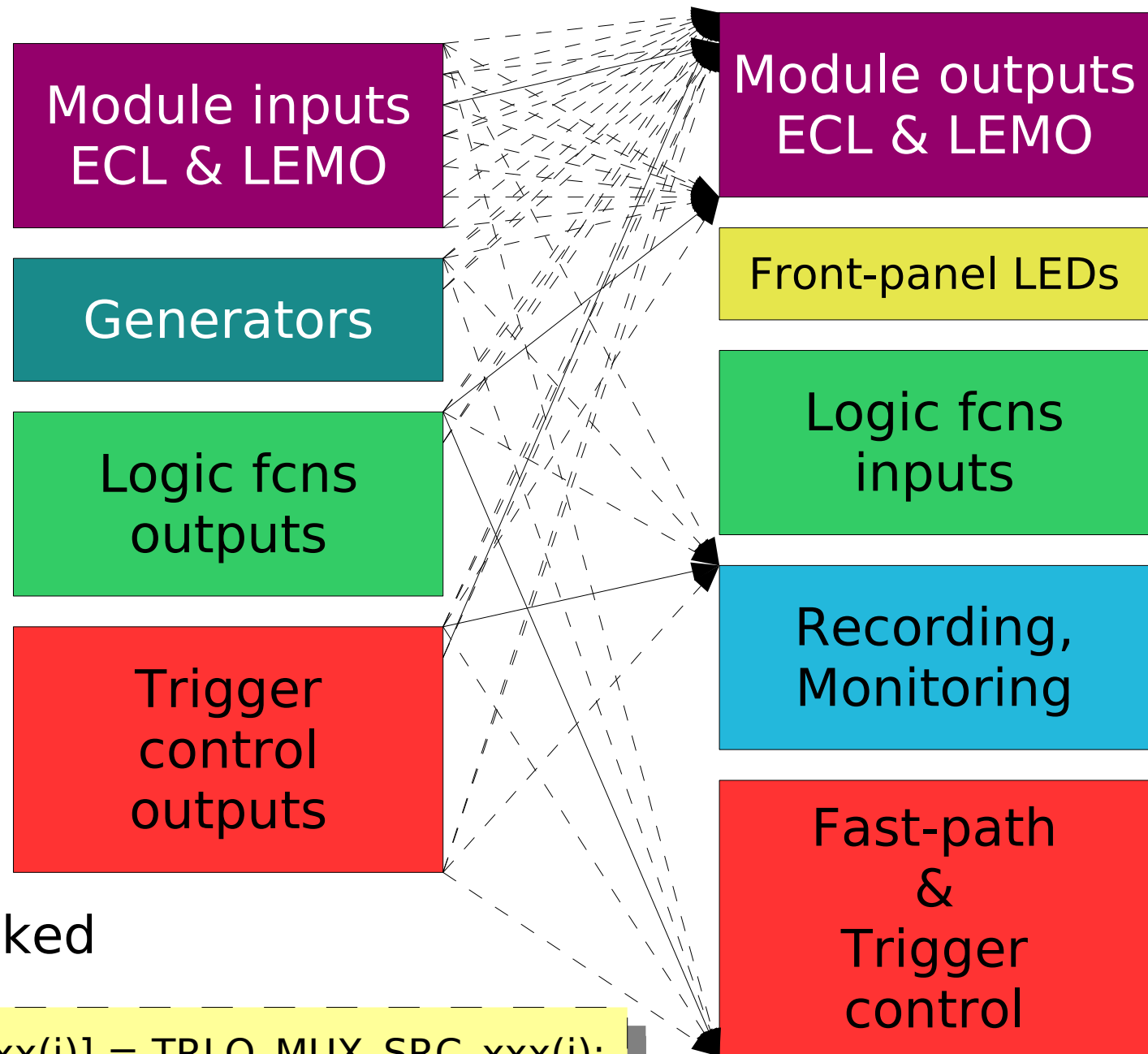
Routing cost:  
2 cycles = 20 ns

Exceptions for timing-critical fast-path:

use fixed **ECL in**

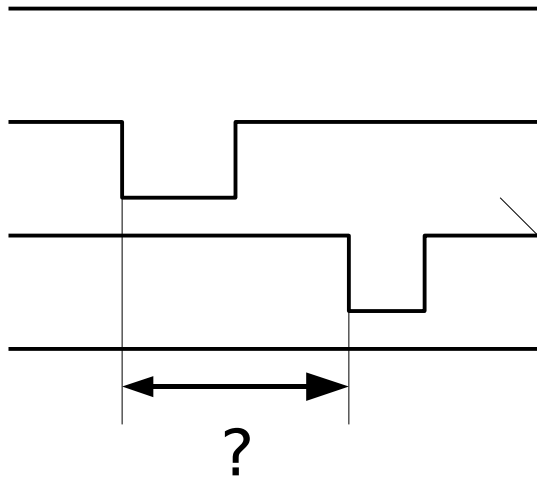
master-start to any **output**, bitmasked

```
mux[TRLO_MUX_DEST_XXX(j)] = TRLO_MUX_SRC_XXX(i);
```



# Trigger alignment - measurement

The triggers need to be aligned to make good coincidences



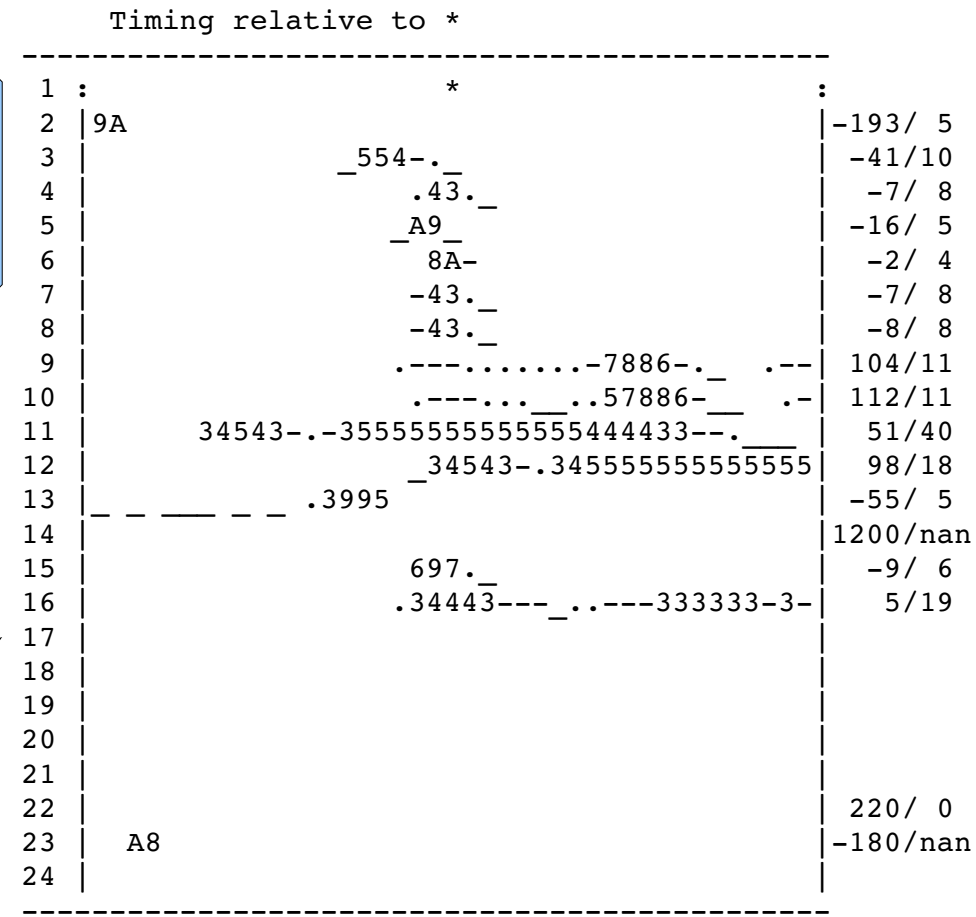
FPGA:  
self-triggered  
multi-event  
softscope

VME readout

```

...
Ch 22: 138-255e
Ch 23: 98-110
End
Start
Ch 9: 125-142
Ch 10: 126-143
Ch 11: 114-131
Ch 12: 127-144
Ch 21: 0-255e
End
Start
Ch 9: 125-142
Ch 10: 126-143
...
    
```

Analysis  
(histogramming)



2-log counts/bin ( \_ . - = 0,1,2)

# Pile-up measurements

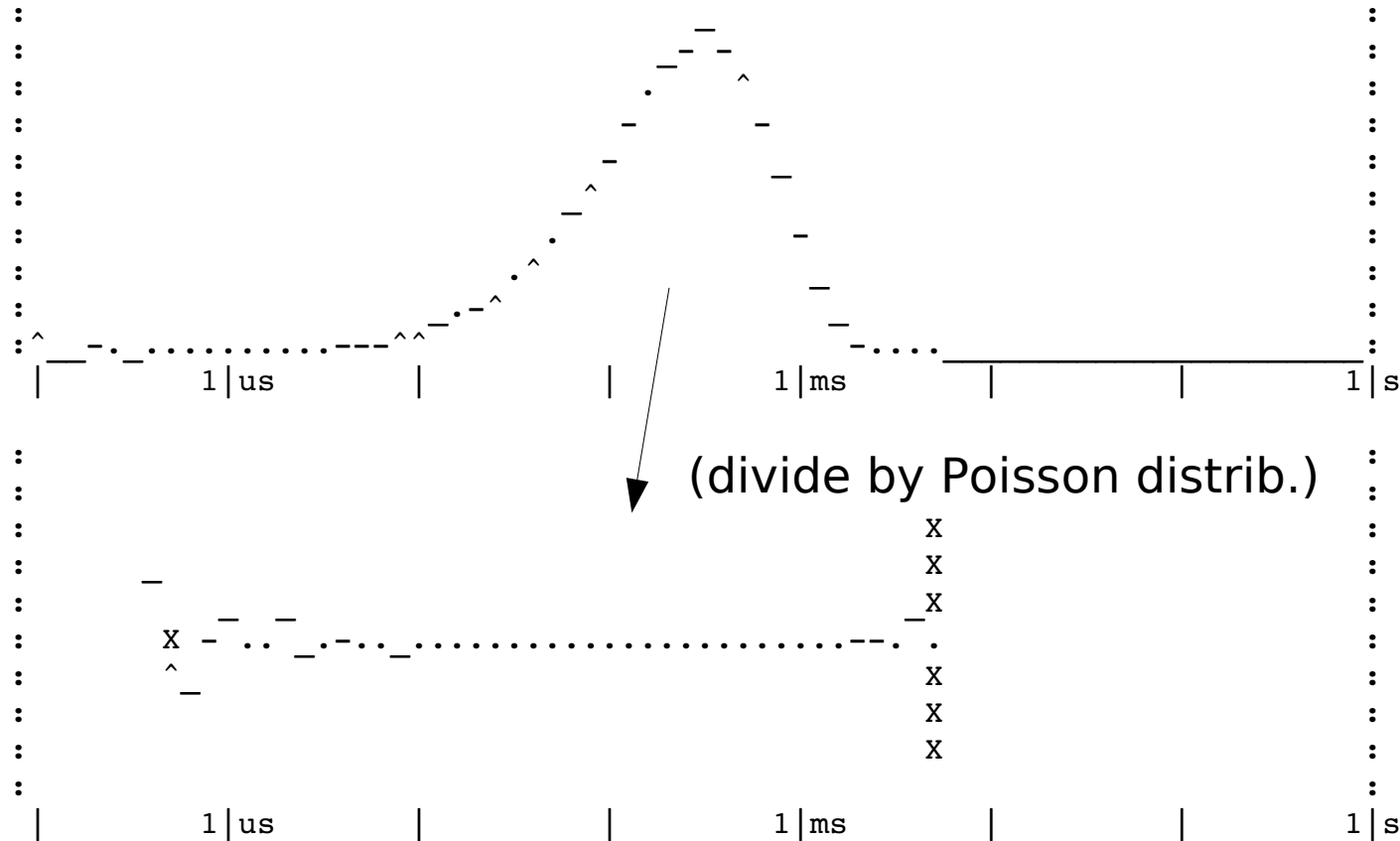
Record **inter-arrival** times of signals

Every **ion** entering the **cave** → off-line **pile-up rejection**

Hits: 1482288 Lost: 1 Cut: 70 = 1.000 s Total\_t: 525.246 s Rate: 2822.1 Hz

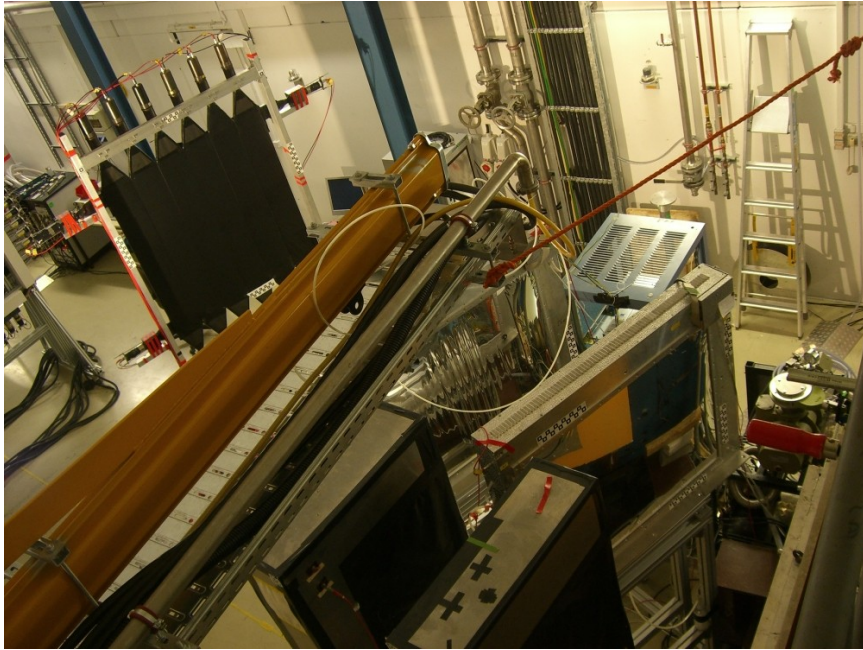
Example: →

almost perfectly  
random detector  
trigger signal  
(cosmics+noise)



# In operation:

S393 S306b S389

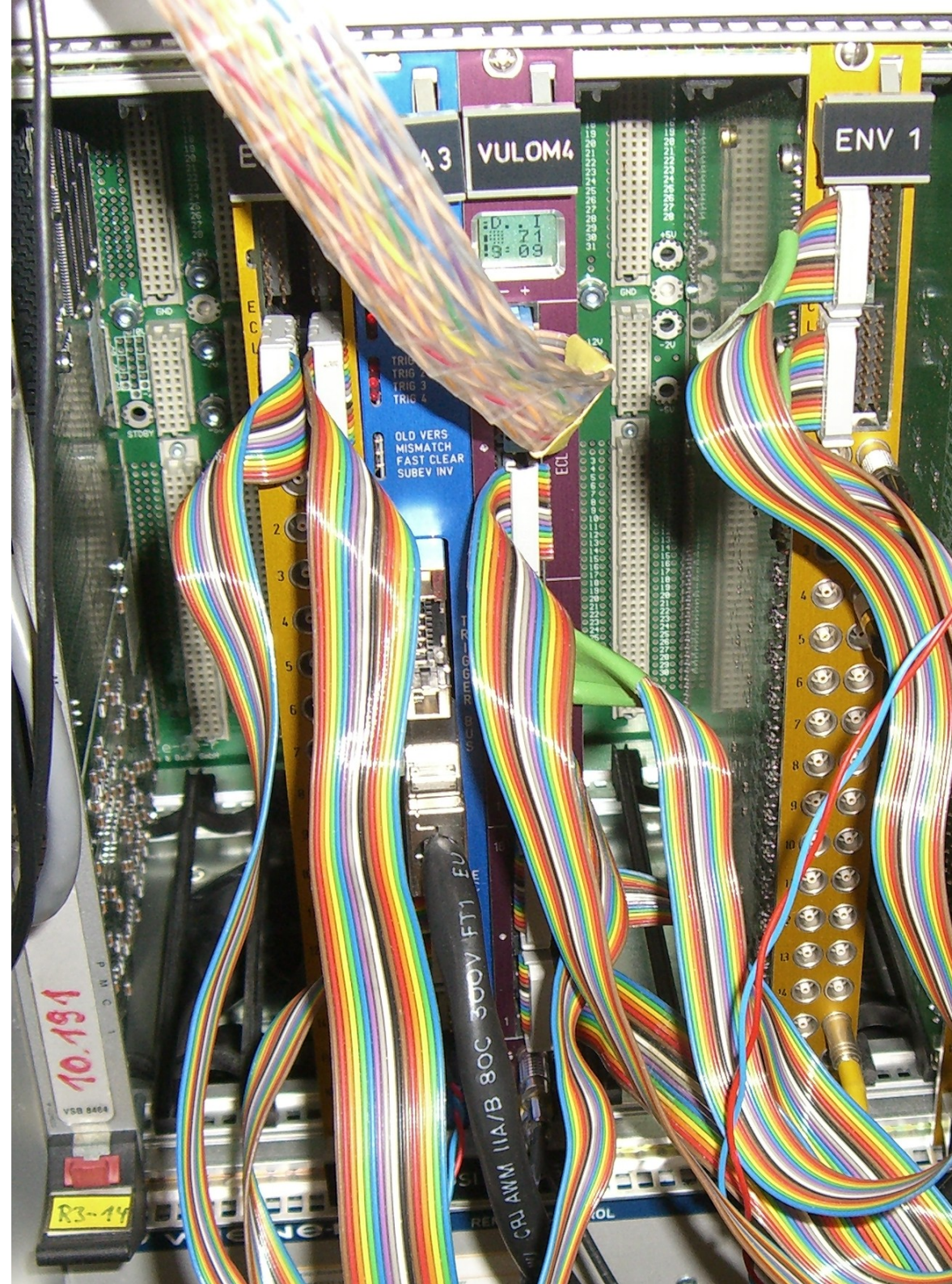


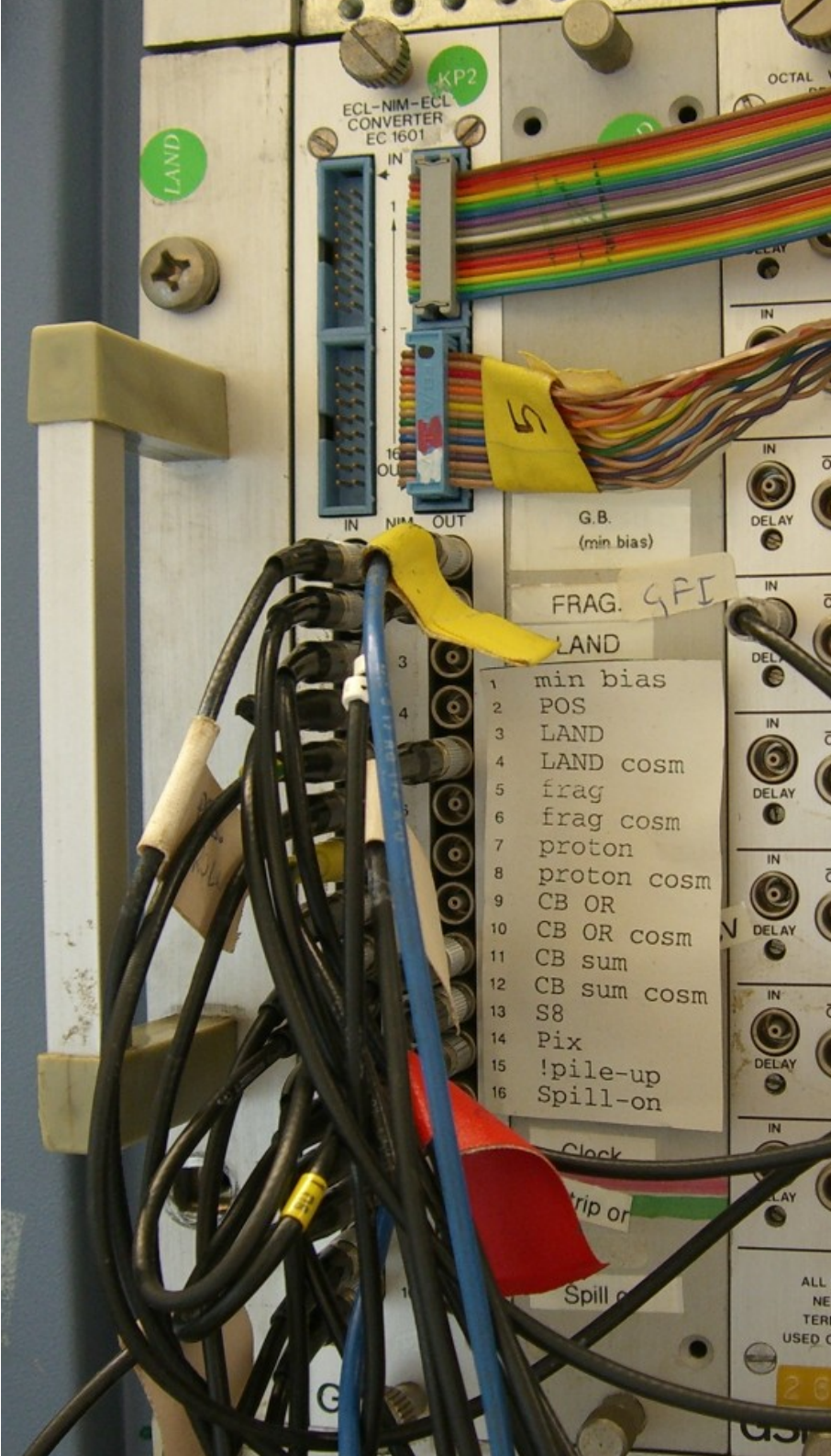
(Aug - Oct 2010)

Preceded by **intense**  
*code* inspection →

**0** critical bugs found

**2** minor bugs found in the wild





# Finale!

# Thank you!

FPGAs are **FUN!**

Live by the compiler timing messages!