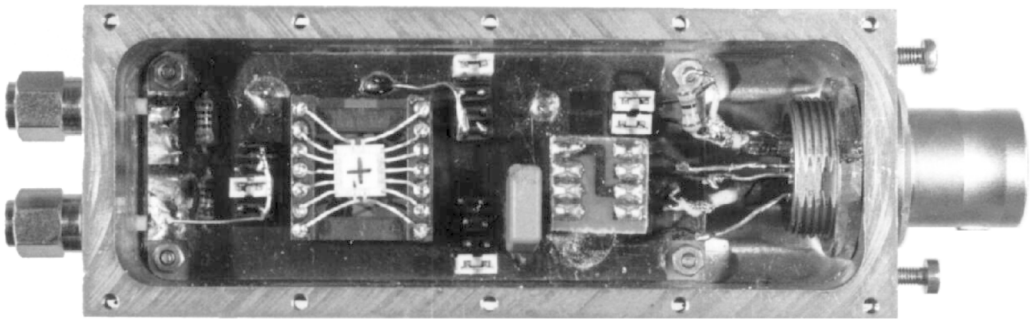
A Cryogenic Preamplifier using a GaAs Field Effect Transistor Input Stage



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Abstract

We have successfully implemented a preamplifier capable of operating in an ambient temperature of 4.2 K. The amplifier utilizes a GaAs Metal-on-Semiconductor Field Effect Transistor (MESFET) input stage which can be immersed in liquid helium. Two MESFETs have been tested, the first had a gate area of 0.049 mm^2 while the other had an area of 0.012 mm^2. With the larger MESFET, the amplifier had a spot noise at 100 kHz and 4.2 K of 1.2 $nV/\sqrt{Hz}$ at a gain of 9000 and a pass band from 400 Hz to 700 kHz. The smaller FET was found to be noisier with anomalous low frequency fluctuations for drain currents above 1 mA. The smaller MESFET achieved a spot noise voltage at 100 kHz and 4.2 K of 2.8 $nV/\sqrt{Hz}$ at a gain of 5700. It was possible to turn on the amplifier at 4.2 K indicating a substantial amount of free charges in the material at this temperature.

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1. Introduction

In low energy physical systems it is often necessary to cool a sample to avoid drowning the phenomenon of interest in thermal noise. This occurs when the thermal energy k_BT becomes equal to or greater than the system's energy scale eV. Therefore the requirements on the amplifier becomes more demanding in low temperature experiments. Such experiments demanding temperatures at 4K and below are usually carried out in a cryostat. The sample is mounted inside the cryostat and then connected to a room temperature preamplifier. The preamplifier has an important function; to match the sample to the measurement electronics without adding noise to the signal. The connection between the sample and the preamplifier is done with coaxial cables and/or DC-lines. These cables inevitably acts as distributed capacitors which together with the samples equivalent output resistance makes up a low pass filter limiting the system bandwidth. The cables also pick up ever present ambient noise. By moving the preamplifier inside the cryostat one can reduce these unwanted effects since the cable lengths are reduced. The preamplifier acts as a buffer and match the cables to the sample. It also provides gain to the signal making it less sensitive to noise pick up. Another benefit of a cooled amplifier is the reduction of its internal noise [1]. One type of noise stems from charges moving randomly which modulates the current in the device. By lowering the temperature this random motion is lowered resulting in a lower noise. Other types of noise are shot noise and telegraph noise which are also affected by the temperature of the surroundings.

When choosing the technology for such an amplifier one is limited to GaAs metal-on-semiconductor field effect transistors (MESFET). This is very unfortunate since all commercially available operational amplifiers and almost all discrete transistors are made in Si. Due to its large donor bandgap, Si suffers from carrier freeze-out and consequently its conductance approaches zero at 4.2K and below whereas GaAs can be doped so that a substantial amount of charge carriers are excited at 4.2K [2]. Most op-amps use bipolar junction transistors (BJT). Such transistors rely on minority charge carriers in their base region. Since the minority charge carrier concentration drops at low temperature, these devices have a current gain near one when cooled, compared to 100 and greater at room temperature. Majority charge carriers do not show this strong temperature dependence and devices using them as charge transport mechanism, such as FETs, can be used at low temperatures [2]. As a consequence of the material and device related properties, the GaAs FET family is a candidate for cryogenic usage.

Due to their high mobility, GaAs-MESFETs for UHF and microwave applications are today commercially available. Unfortunately most FETs don’t work at 4.2K although there have been certain types, currently not in

production, that have been reported to work well. For example, the Plessey GAT 1/010 GaAs MESFET had a spot noise level of 1.5 nV/√Hz at 6 MHz and 4.2K [3] while a UHF amplifier using this device with spot noise of 0.19 nV/√Hz at 430 MHz and 4.2K has been reported [4]. This device is now discontinued. The 3SK166 is a UHF GaAs MESFET today commercially available from Sony Electronics which has been reported to work at cryogenic temperatures [5]. One problem with microwave FETs is their small gate area. This lowers the input capacitance but requires higher drain currents to get as high transconductance as a large gate FET. The small gate also makes the device sensitive to single impurities giving a peaked low frequency noise spectrum instead of the usual 1/f noise. In general, microwave devices are not optimized for 1/f noise at frequencies below some 100 MHz which makes them hard to use in DC amplifiers.

The MESFET should neither be confused with the MOSFET (Metal-Oxide-Semiconductor FET) which is used in all microprocessors today (CMOS technology), nor the HEMT (High Electron Mobility Transistor) which rely on a two dimensional electron gas (2DEG). The MESFET uses a reverse biased Schottky diode whereas a MOSFET uses an insulating oxide barrier. Furthermore the MESFET creates a channel by gate-controlled material inversion as is the case in a MOSFET, but not in the HEMT which uses the 2DEG as channel.

2. Amplifier Design

2.1 Circuit Description

The circuit presented below is very similar to that described in ref. 5. The circuit which we have used is shown in Fig. 2-1. The input signal voltage is connected differentially to the input connectors at the gate of Q1 which is the cooled GaAs MESFET[1]. The MESFETs came mounted in a 14-lead wide ceramic flat-pack. The two dies, labeled + and - contains four MESFETs each, two with a gate width of 1024 μm and two with 3072 μm. The difference between the two dies was the gate length, 4μm for the + die and 16 μm for the - die. The die with the larger gate area is hereafter called the larger MESFET and the smaller is called the smaller MESFET. A 20MΩ input resistor sits across the input terminals in order to bias the gate and also to get a well defined input impedance of the amplifier (the gate resistance of Q1 is 100 GΩ or more at cryogenic temperatures). Q1 acts as a transconductance amplifier i.e. a voltage controlled current source which converts the gate-source voltage to a drain current. This current flows from the source electrode of the room tempered JFET Q2[2] through a 50Ω coaxial cable. The source input impedance of Q2 is made small ($\approx 1/g_m$ where g_m is the transconductance) by AC grounding its gate capacitively. The drain resistor connected to Q2, which sets the voltage amplification is therefore effectively isolated from the cryogenic FET. This is important since the drain output impedance of Q1, r_0, goes down at cryogenic temperatures making it look less like a current source. The signal output is the drain of Q2 which is AC coupled to following op-amp stages. This type of transistor interconnection of Q1 and Q2 is called a cascode configuration and its benefits are discussed in section 2.2.

The operating point of the cascode can be set with three trim potentiometers located at room temperature. The source of Q1 is connected via a DC line to a 5 kΩ trimmer in series with a 100 Ω resistance. This trimmer sets the drain current of Q1 as can be seen from inspection of the gate-source network. The 100Ω series resistance provides a simple way of monitoring the drain current by measuring the voltage drop across it. The bias network is capacitively bypassed to ground to increase the gain. A bias network is connected to the Q1 drain - Q2 source node. It consists of a 50 kΩ trimmer which can be used to set a different drain current in Q2 than that in Q1 making it possible to trim the DC bias at the output for optimum dynamic performance. It was necessary to insert a 5 kΩ protection resistance in series with the trimmer since many JFETs burned up due to forward biasing of the gate-source p-n barrier. This protection found to be satisfactory. Finally, the gate of Q2 is biased by a 5 kΩ

[1]The MESFETs which were optimized for low temperature applications, were supplied by Randall K. Kirschman.

[2]Q2 is a 2N4416 manufactured by Motorola.

trimmer. This trimmer sets the drain-source voltage of Q1. A parallel capacitance bypasses the trimmer to ground.

The cascode is followed by three non-inverting op-amp stages which together provide a gain of 400. The op-amps used were all OPA637 from Burr-Brown which need a gain greater than five to be stable. The first two stages each have a gain of 50, while the last has a gain of 8. The gain-bandwidth product of these amplifiers is 80 MHz, yielding a cut off frequency at 11.3 MHz for the first two and 10 MHz for the last stage. Inserted between each stage is a high-pass RC network, with a corner frequency of about 0.2 kHz. They remove DC components and eliminates the need for offset trimming the op-amps. Since the capacitors are in the signal path they are polypropylene types in order to get a good high-frequency performance. Two outputs with different gains are available; 250 and 2000. It was required to isolate the op-amp outputs from the capacitive loads that coaxial cable make up. The added capacitance adds a phase-shift to the negative feed-back making the amplifier unstable. An isolation of 50 Ω sufficed, and also resulted in matching the outputs to 50 Ω loads.

All power supply connections are in series with a 1 µH RF choke and shunted with 4.7 µF parallel with 100 nF to ground. The 4.7 µF are electrolytic types buffering large surge currents and the 100 nF are polystyrene types providing a good short-cut to ground for transients. Originally the RF chokes were 1.5 mH but they formed a LC tank with the shunting capacitors. The resonance frequency was about 10 kHz and modulated the power supply leads which was first detected as a peak in the frequency response. The modulation was checked with an oscilloscope connected to the power supply lines and a 10 kHz signal applied to the signal input. This indicates that rejection of power supply noise by the cascode is poor, which probably stems from the low output impedance of the MESFET making the source bias circuit susceptible to power supply variations. The 1 µH chokes removed the 10 kHz resonance. Protection diodes were inserted in between the power supply pins. The diodes are reverse-biased under normal operating conditions. If the applied voltage is reversed the diodes are forward biased, conducting heavily. The resulting current surge will burn the power supply's fuse removing the voltage (The fuse must of course have a lower current rating than the diodes).

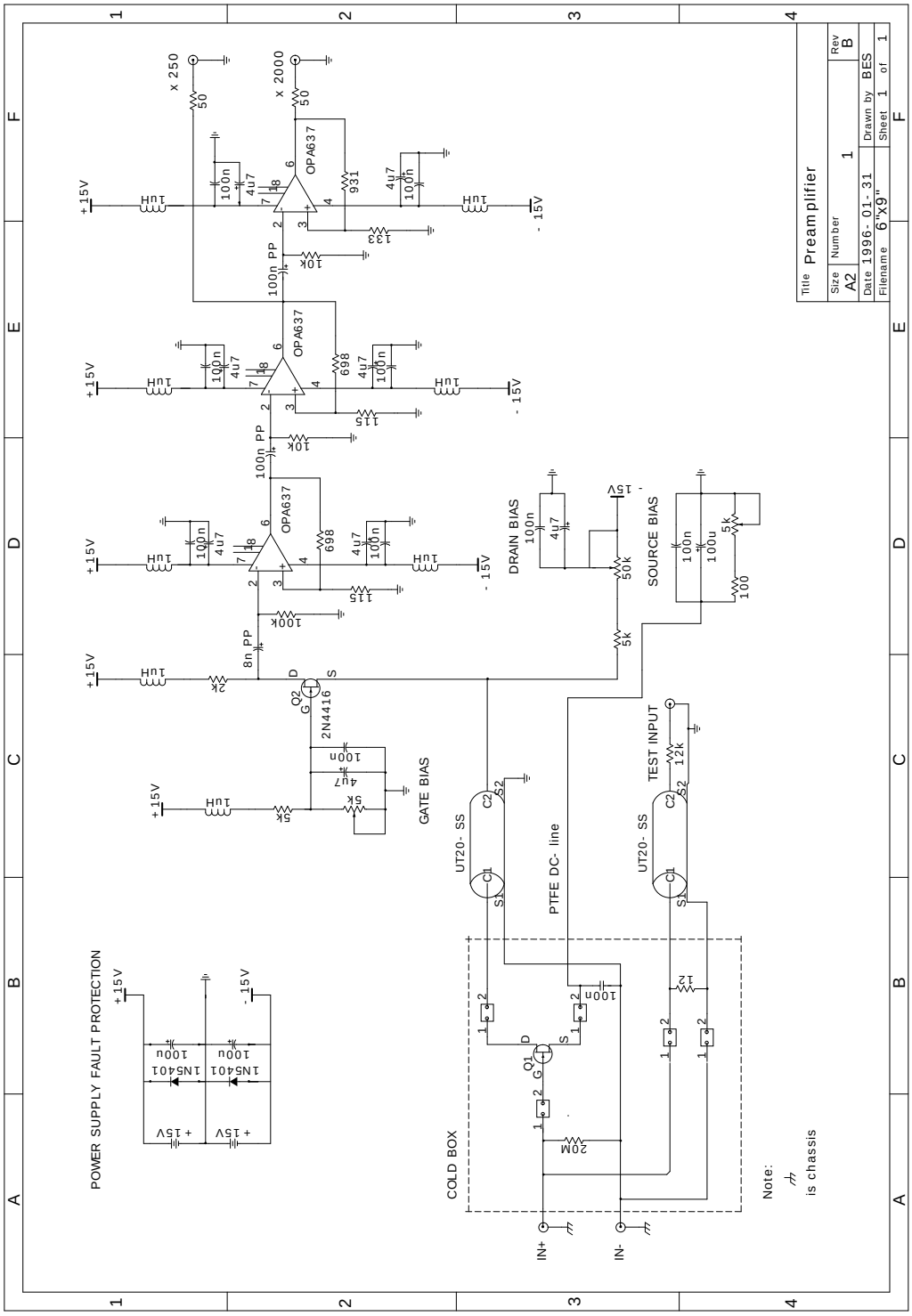

Fig. 2-1. The circuit schematics. The inputs are labeled IN+ and IN- and the outputs x 250 and x 2000. Components within the dashed box are situated at cryogenic temperature.

2.2 The cascode

The cascode configuration is a circuit providing a large bandwidth (which shouldn't be confused with the cascade configuration). The circuit eliminates the so called Miller effect which is the capacitive feedback from drain to gate electrode of the FET. This effect limits the upper frequency in a common-source circuit. The Miller effect and the Cascode are extensively discussed in ref. 6.

Lee describes a cryogenic preamplifier using GaAs MESFETs in a cascode [5]. It consists of a cryogenic part containing MESFETs in parallel connected by a coaxial cable to a room temperature part with a common Si JFET completing the cascode. The cascode is followed by conventional op-amp stages. The gain of the cascode is given by

$$A_V = g_m \frac{r_{0-cs}}{r_{0-cs} + r_{s-2}} \frac{R_d r_{0-2}}{R_d + r_{0-2}} \approx g_m R_d \qquad (1)$$

where g_m is the transconductance of the MESFET, $r_{0\text{-}cs}$ is the drain output impedance of the MESFET, $r_{s\text{-}2}$ and $r_{0\text{-}2}$ are the source input impedance and the drain output impedance of the JFET respectively, and R_d is the resistor at the drain of the JFET.

2.3 Experimental Apparatus

Physically the amplifier is made up of three parts, the cryogenic electronics contained in 'the cold box', the room temperature electronics contained in 'the warm box' and a dipstick connecting the two boxes. With the boxes mounted on the stick, the cold box can then be inserted in a 2" neck helium dewar. The cold box must be shielded and must be small enough to fit inside the cryostat. The dipstick must be a poor heat conductor to conserve liquid helium but yet present a low electric resistance for the signals. The warm box must be shielded to avoid interference.

The cold box, shown in Fig. 2-2, was milled from a brass block. Two SMA connectors connects to the input terminals of the amplifier. The SMA connects their centers to the gate and signal ground respectively. The signal ground is thus separated from the chassis (See also section 2.4). Because the MESFETs came four per package, jumpers were installed to be able to connect each MESFET independently. Another pair of jumpers makes it possible to connect/disconnect the test signal leads to the amplifier input. The drain of the MESFET is connected to the center lead of a coax. The shield of the coax is connected to signal ground. The source of the MESFET is connected to a DC line. The coaxes and DC lines are housed in a single LEMO connector, chosen

for its capacity of two coaxes and ten DC lines. The LEMO then connects to the dipstick. The components are soldered onto a double-sided copper-clad printed circuit board (PCB) with a thickness of 0.5 mm. The bottom plane of the PCB is used as the solder side and all circuit paths are drawn here. To get a good ground-plane the top plane is left completely copper-covered, except for component pin holes which are countersinked.

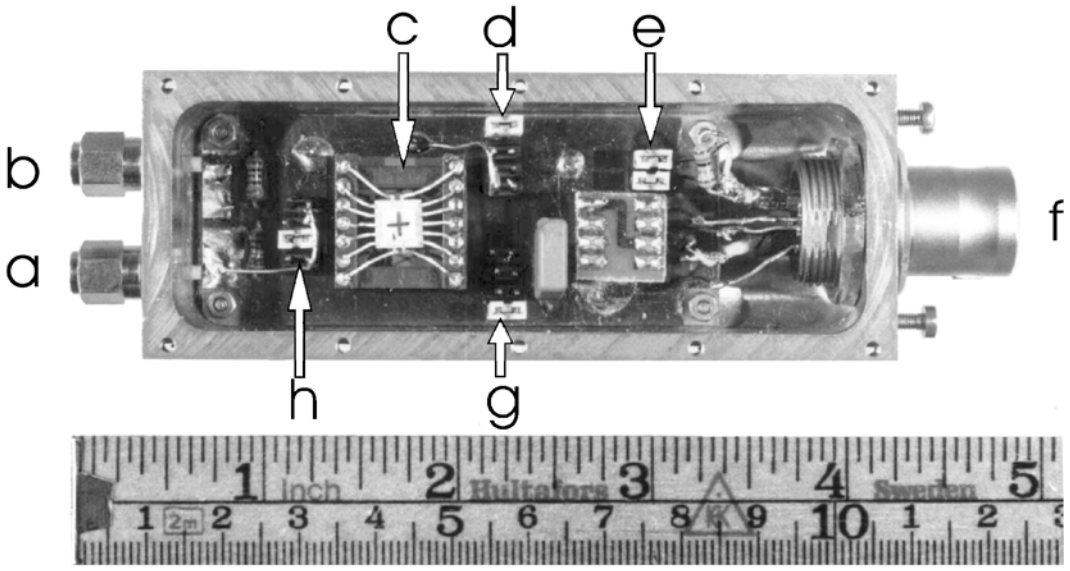

Fig. 2-2. The cold box, which is to be mounted in the cryostat. a) IN- input, b) IN+ input, c) MESFET chip, d) drain jumpers, e) test coax jumpers, f) LEMO connector (to dipstick), g) source jumpers and h) gate jumpers.

The dipstick is made of a thin walled stainless steel tube onto which brass sockets are soldered, one at each end of the tube. The sockets house the LEMO connectors. The length of the tube is 1 (one) m. The stick is mounted through a KF-50 flange to make a vacuum connection to the dewar. The stick is greased with vacuum grease and can then slide through the flange making it possible to set the box height relative the helium level. The coaxes used in the stick are 1 m of UT 20-SS, a semi-rigid coax with a center lead diameter of only 5 mils (0.13 mm). The material is stainless steel, chosen for its relatively poor heat conductivity. The DC lines are Teflon-insulated silver-coated wires of AWG 36 with a small diameter 0.40 mm to minimize heat leaks. The lines were twisted in pairs and these pairs were twisted in turn to minimize pick-up loop area.

The warm box contains the JFET, the three trimmers and the op-amp output stages as well as input/output connectors all housed in an aluminum shielded box. It is shown in Fig. 2-3. Lines from the cryogenic stage enters the LEMO contact. The test input leads are separated directly and connected via a series resistor to a BNC connector mounted in the chassis. The series

resistance was chosen rather arbitrarily to 12 kΩ. The signal from the MESFET is fed to the JFET located at a small printed circuit board (PCB) just below the LEMO connector. The drain of the JFET is then fed through a small piece of coax to the main PCB were the signal is filtered and amplified and is finally output at two BNC connectors. The three bias lines are fed from the LEMO connector via the small PCB to the main PCB through a ribbon cable and ends up at the trimmers were biasing is adjusted. A good ground-plane is achieved on the main board in the same way as in the cold box.

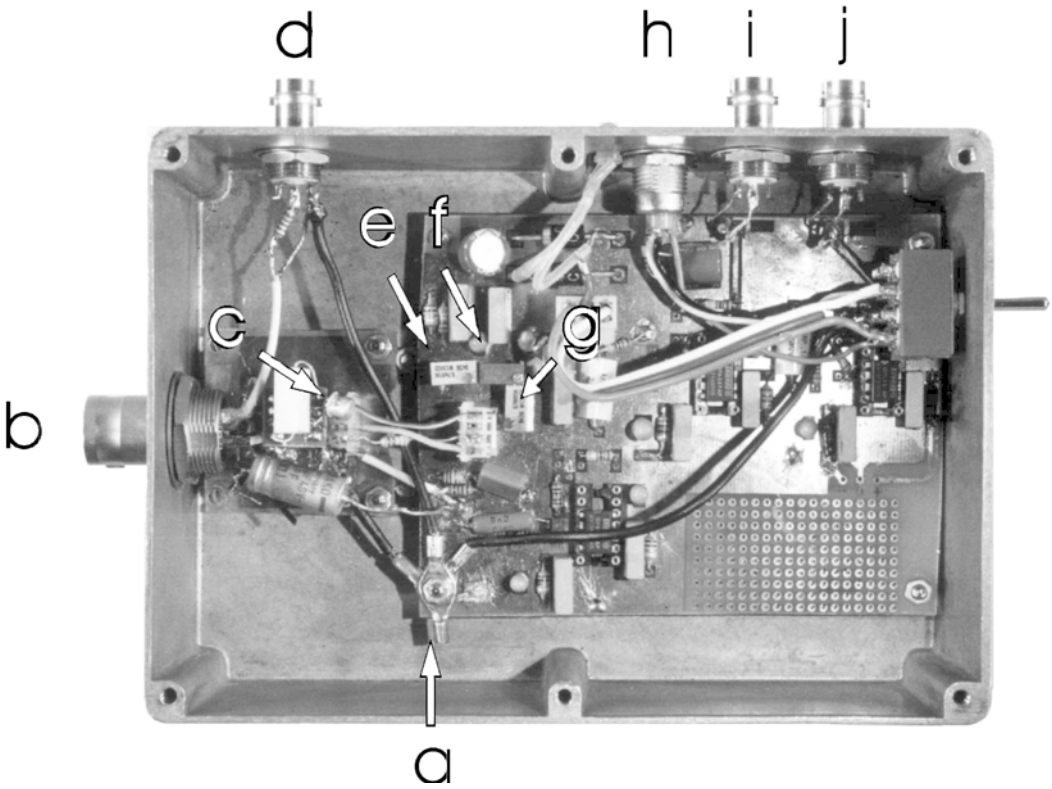

Fig. 2-3. The warm box. A small PCB to the left in the picture contains the upper part of the cascode. The larger PCB contains the op-amp stages, the trimmer resistors and power supply circuits. a) common ground point, b) LEMO connector (to dipstick), c) Si JFET, d) test input, e), f) and g) are gate, drain and source trimmers respectively, h) power supply input, i) x 250 output and j) x 2000 output.

2.4 Grounding Techniques

The circuit is designed using a single ground-point philosophy i.e. all subsystems' signal grounds should be connected in a tree-like fashion, branching from one common ground point without any loops. This ground point is shown in Fig. 2-3. Here the small PCB, test input and power ground meet at the same screw. The screw then connects to the main PCB by a nut and the screw head contacts the chassis to get a shielded box. The two outputs

i) and j) which are isolated from the chassis, are not grounded this way but are instead connected directly to the top ground-plane of the main board.

3. Experiments

The most important properties of an amplifier are its amplification as a function of input frequency (often called the frequency response), and the internally generated noise in the amplifier. To measure the frequency response one inserts a sinusoidal signal of known amplitude and frequency and then measure the output signals magnitude and phase compared to the input. The resulting curves are then often plot in a Bode diagram where the phase and gain are given as functions of frequency. The noise of an amplifier is often modeled as an equivalent voltage noise generator and current noise generator at the input of a noiseless amplifier [7]. To obtain the magnitude of the voltage noise generator, the input is grounded shorting the current noise generator. A noise spectrum is measured at the output and by dividing the spectrum by the frequency response of the amplifier the input voltage noise is obtained. By connecting a sufficiently large resistor between the signal input and ground terminals, the voltage noise contribution from the current noise generator flowing through the resistor, is much greater than the voltage generators contribution. However, a resistor has in itself a Johnson noise power proportional to the resistance. The equivalent noise current is now obtained by measuring the output voltage and dividing it by frequency response to get total noise voltage at the input. The current noise contribution can be separated from the Johnson noise of the resistor and the voltage noise generator since the noise components are uncorrelated. The result is divided by the resistance to get the input noise current. Only voltage noise was measured in this work.

3.1 Instrumentation

The frequency response was divided into two intervals, set by the measurement equipment. A Hewlett-Packard HP35665A Dynamic Signal Analyzer was used in the frequency range 10 Hz - 50 kHz, 50 kHz being the upper limit of the HP running in this mode. In the 50 kHz - 30 MHz range a Stanford DS345 Function Generator and a Fluke PM3328A Digital Oscilloscope controlled by a measurement computer were used. The Stanford is capable of producing an accurate sinusoidal signal up to 30 MHz while the Fluke can acquire signal frequencies up to 100 MHz and also calculate the RMS. voltage of a trace. The computer was a Macintosh running LabView software.

Noise spectra were taken by the HP which had built-in FFT analysis features. The upper frequency limit in this mode was 100 kHz. To get a good resolution the frequency range was divided into two intervals, 10 Hz - 1 kHz and 1 kHz to 100 kHz, each with 400 points. No noise spectra were taken above 100 kHz.

3.2 Methods

Experiments were carried out for two different MESFETs , with gate areas of 0.049 mm^2 and 0.012 mm^2. For each FET the frequency response and noise spectra were measured at different bias points. A bias point is defined by a double number, the MESFET drain current I_d and its drain - source voltage V_{ds}. The DC level at the cascode output, V_{dc} thus effects the bias point for the upper JFET, but this parameter was held constant at 7.5 V midway between 0 and 15 V.

At room temperature each bias point was set by first trimming the drain current to its desired value using the source trimmer. The DC voltage was then set by the drain trimmer to about 7.5V to maximize the cascode dynamic range. Last, the drain-source voltage was set by the gate trimmer. It was found necessary to iterate the last two steps to close in on the desired bias point. The drain current was independent on the two voltages. The bias points were measured with a hand-held Fluke DMM. It has a 3 digit accuracy which is quite sufficient in this application. The drain current was deduced from the voltage drop across the 100 Ω resistance at the source of Q1 (discussed in the previous chapter).

The amplifier was cooled by immersing the cold box in liquid helium at 4.2 K in a dewar. The dipstick could be locked at different heights above or below the liquid surface level to obtain different temperatures. Measurements were only conducted at 4.2 K however. When a MESFET is cooled, its output resistance drops. This means that its drain current is no longer independent on the drain-source voltages. Thus the drain current drifts when adjusting the drain-source voltage. As a consequence all three biasing steps had to be iterated to obtain the correct bias point instead of only the last two as in the room temperature case.

To check whether or not there were any free charges at 4.2 K, the bias was removed and the FET was allowed to cool for one hour. When the bias was returned, the FET conducted immediately indicating a substantial amount of free charges at 4.2 K in this sample.

4. Results

4.1 Large gate area FET

The equivalent input noise voltage at 100 kHz (spot noise) and at 4.2 K for various bias points for MESFET A- is shown in Fig. 4-1. Trends can clearly be seen. The noise goes up with increasing drain-source voltage V_{ds} but goes down with increasing drain current I_d. By analyzing the complete noise spectra it is found that the total lowest noise was achieved at an bias of I_d = 4 mA and V_{ds} = 1 V yielding a spot noise at 100 kHz of 1.2 nV/√(Hz).

In Fig. 4-2 the pass band gain (defined as the gain between the lower and upper frequency cut-offs) is shown in a bias map. The gain goes up with increasing drain current as well as with increasing drain-source voltage. The peak gain is about 11000, and the gain at the bias point with lowest noise is 9000. The transconductance g_m of a FET usually goes up with increasing drain current. Since the gain of the cascode is proportional to the MESFET g_m (see chapter 2) it will therefore rise with increasing drain bias. The op-amp stages had a total gain of 400 giving the cascode a gain about 27.5 peak gain, and 22.5 at lowest noise bias (see below).

The effect of cooling the amplifier is shown in Fig. 4-3(a). The minimum noise level decreased by a factor of 5 when going from 300 K to 4.2 K. The gain remained almost constant as can be seen in Fig. 4-3(b). The lower cut-off frequency which is defined as the -3 dB point relative the pass band gain can be extracted from this graph and is about 390 Hz.

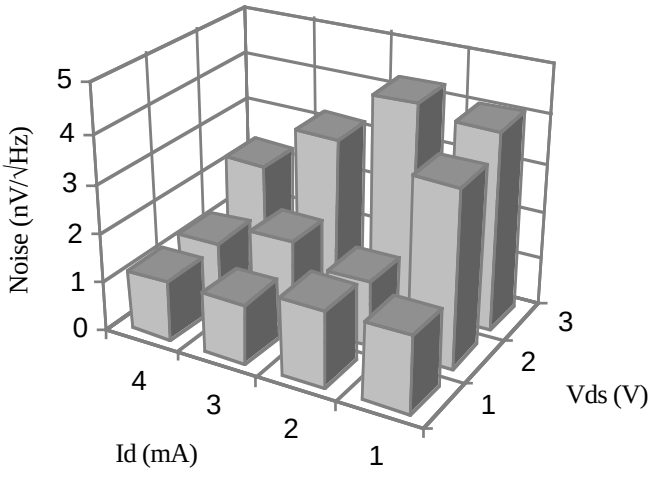

Fig. 4-1. Spot noise at 100 kHz for various MESFET bias for the large MESFET. Although the spot noise has a minimum at 2 V and 2 mA the lowest noise spectrum was found at a bias of 1 V and 4 mA.

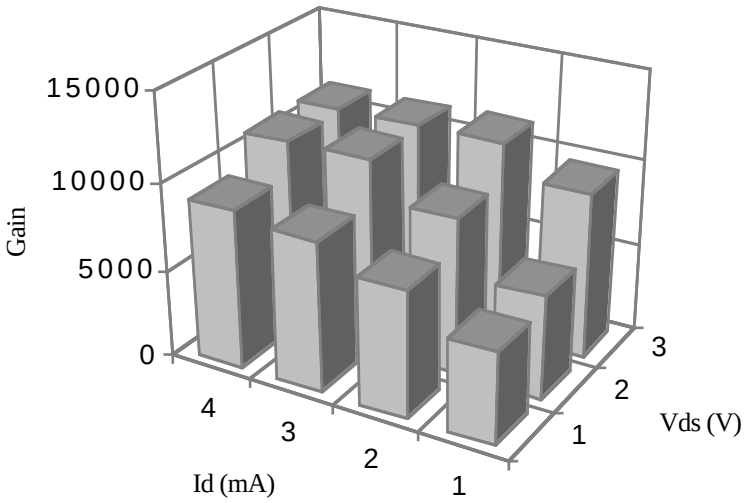

Fig. 4-2. Pass band gain at 50 kHz as a function of MESFET bias for the large MESFET.

A complete frequency response is shown in Fig. 4-4 from which the upper cut-off frequency (defined in the same manner as the lower cut-off) can be determined to 700 kHz.

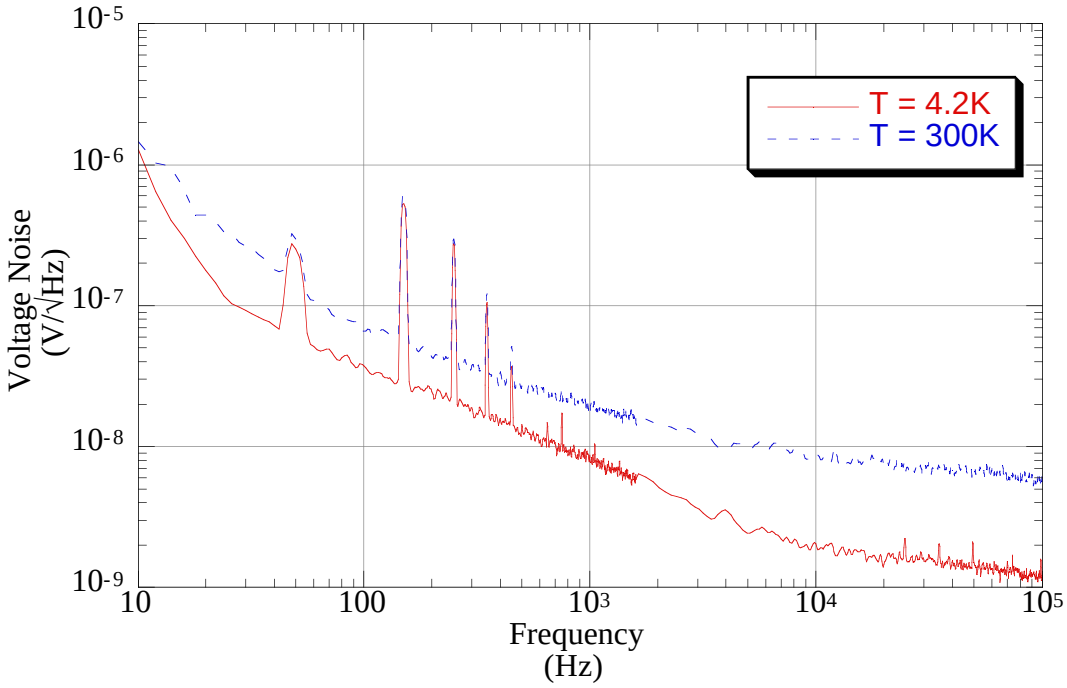

Fig. 4-3(a). Noise spectra at the lowest noise bias for different temperatures for the large MESFET. The peaks below 1 kHz at 50 Hz and odd multiples thereof, comes from magnetic noise pick-up from the power lines via circuit ground loops.

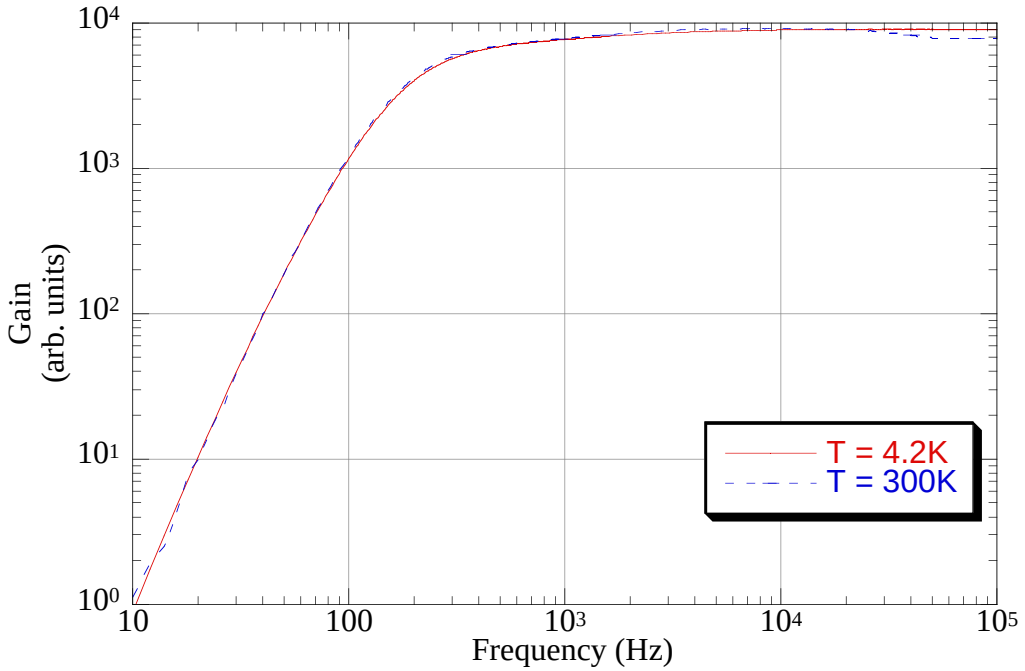

Fig. 4-3(b). Frequency response at lowest noise bias for different temperatures for the large MESFET. A little dip was found above 30 kHz at room temperature.

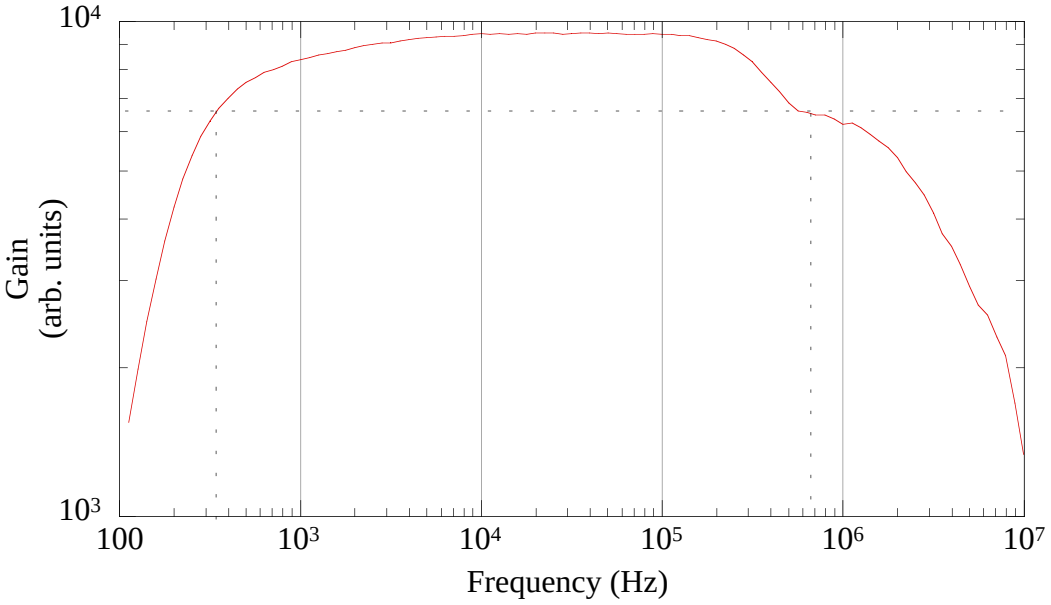

Fig. 4-4. Total frequency response curve at 4.2 K for the large MESFET. The horizontal line shows the -3 dB level from the maximum gain. The lower and upper cut-off frequencies are found at the intersection of the -3 dB line and the frequency response and are 390 Hz and 700 kHz respectively. The dip seen at 700 kHz is of unknown origin.

4.2 Small Gate Area FET

The small MESFET showed spurious noise bursts for a large number of bias points. The bursts made the amplifier unusable and were found at drain currents larger than one mA. Therefore the MESFET had a very limited operational bias range and only three points could be measured. The spot noise at 100 kHz and at 4.2 K for these points are shown together with in Fig. 4-5. The lowest noise was 2.8 nV/√(Hz) obtained for the bias I_d = 1 mA, V_{ds} = 0.7 V. The noise goes up with increasing V_{ds}. The gain is shown in Fig. 4-6. The pass band gain at lowest noise bias point is 5700. The gain goes up for increased V_{ds}. Overall, the amplifier performed poorly with this MESFET.

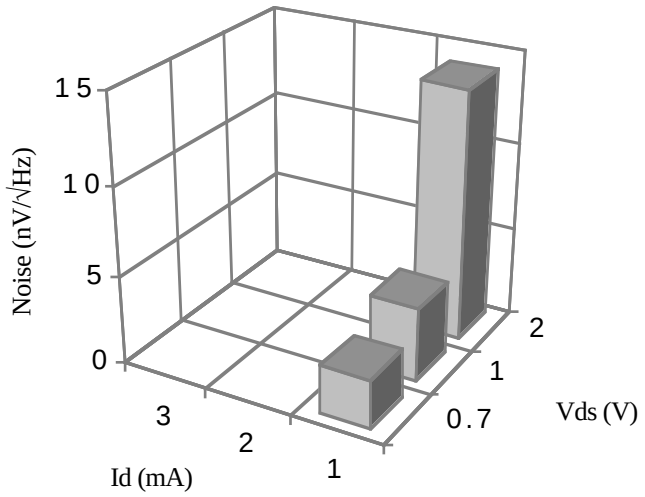

Fig. 4-5. The spot noise at 100 kHz and 4.2 K for the small MESFET. Only bias points without bursts were measured.

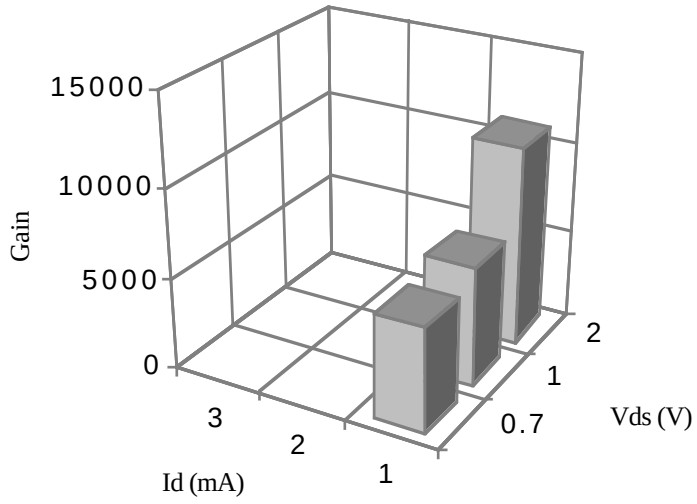

Fig. 4-6. Pass band gain for various bias points at 4.2 K for the small MESFET.

The anomalous noise fluctuations in the output voltage were observed for the smaller MESFET for drain currents greater than 1 mA. This resulted in a jumping noise spectrum. The fluctuations came randomly with an intermittencity ranging form 15 to 30 seconds. In Fig. 4-7, a burst-like character of the noise fluctuation is seen clearly. Such fluctuations were also reported by Lee [5].

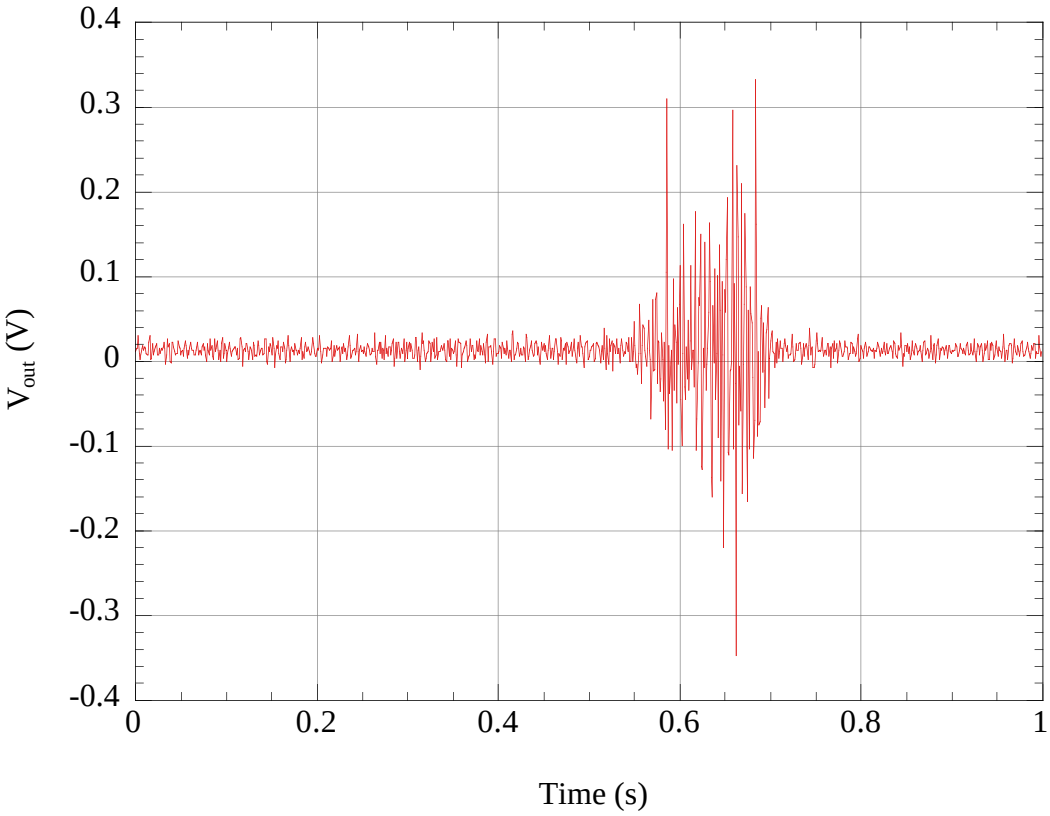

Fig 4-7. A typical noise fluctuation observed at the output for large MESFET drain currents in the small MESFET. The noise background was otherwise low as can be seen in the figure. The bursts had large low frequency components making the amplifier unusable.

5. Conclusions and Discussion

5.1 Amplifier Performance

An amplifier capable of operating at 4.2 K has been built. The best results are obtained with the largest gate FET, while the smaller FET has a limited usable bias range. The lowest noise spectrum found has a spot noise level at 100 kHz of about 1.2 nV/√(Hz) at a pass band gain of 9000. The pass band of the amplifier goes from about 400 Hz to 700 kHz. The amplifier is rather sensitive, and prone to oscillations with the RF chokes in the power supply filters.

In Fig. 5-1 our amplifiers noise is compared with data taken from ref. 5. The 1/f noise performance is superior to Lee's amplifier, while the thermal noise floor seems equal. The former was expected since the MESFETs where designed with a large gate area to lower the 1/f noise [8].

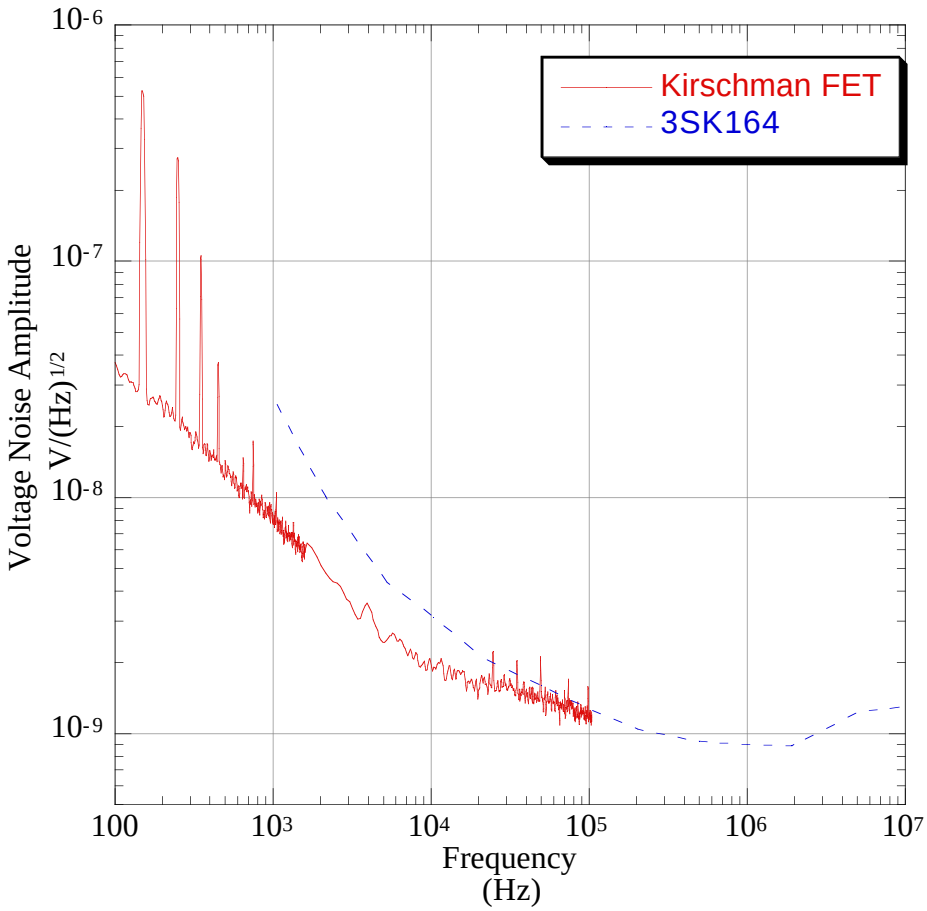

Fig. 5-1. A noise performance comparison of the custom FET and the 3SK164 FET. The 3SK164 was used in Lee's amplifier where four devices where connected in parallel to lower overall noise [5]. *The custom FET shows better 1/f noise performance, probably due to its larger gate area.*

5.2 Improving the Performance

Lee achieved a spot noise level at 1 MHz of 0.9 nV/√(Hz) at 4.2 K 0[5]. This is not directly comparable to our spot noise at 100 kHz since the noise spectrum still drops off at 100 kHz. The spot noise at 1 MHz remains to be examined.

The noise minimum is in the upper left corner of the bias map and there is a possibility that even lower noise levels can be reached at larger drain currents and lower drain source voltages. This has to be checked.

The equivalent input noise current has to be measured and plotted in a bias map. Together with the equivalent noise voltage measured in this work it will then be possible to find the optimum resistance of a signal source yielding lowest noise.

The noise contribution of the JFET Q2 has to be measured. It may be possible to lower noise levels by replacing the JFET with a low-noise bipolar transistor, although it has been shown that the input stage of the cascode is the dominant noise source [9].

The gain of the cascode is about 22.5 at the bias point with lowest noise, which is almost five times larger than in Lee's. The much larger gate area of the MESFET used in our cascode controls a wider channel and the transconductance is therefore greater than in the small gate FETs used by Lee [5]. The gain is set by the JFET drain resistor and must be lowered 5 times to about 400Ω to get a gain of five. This decreases the output impedance of the cascode and will probably raise the bandwidth (see below).

The lower frequency corner is about 400 Hz at lowest noise and is set by two RC time constants, the MESFET source AC-ground and the JFET gate AC-ground. The first one consist of the source trimmer in parallel with a capacitor. The second one consists of the gate trimmer network in parallel with a capacitor and in series with the source-gate resistance of the JFET. Both are bias dependent but can be arbitrarily low by increasing the capacitor values. The upper frequency cut-off is about 700 kHz which is 14 times lower than the 10 MHz achieved by Lee[5]. The dip in the gain at 700 kHz lowers the bandwidth and the origin of this effect is unknown. If the dip is removed and a simple high-pass filter response is extrapolated, the frequency corner will be found near 2 MHz. The main RC time constant is formed by the capacitance from the coaxial cable to ground in the dipstick, giving a total of about 100 pF, and the source to gate input resistance of the JFET of some 200-300 Ω, yielding a cut off frequency of 6 MHz. The op-amp stages also contribute due to their gain-bandwidth product. With the dip removed at 700 kHz, the amplifier would have a gain-bandwidth product of 50 MHz which is the same as Lee

found [5]. Decreasing the gain by a factor of five should increase the bandwidth to 10 MHz.

The cascode is susceptible to resonance with the power supply filters. This can be reduced by inserting a small resistor in series with the source biasing network. The resistor will provide negative feedback to the gate mirroring the fluctuations in the drain current. However, this will also decrease the gain. An alternative is to replace the entire source network with an active current source. This may however increase the noise.

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