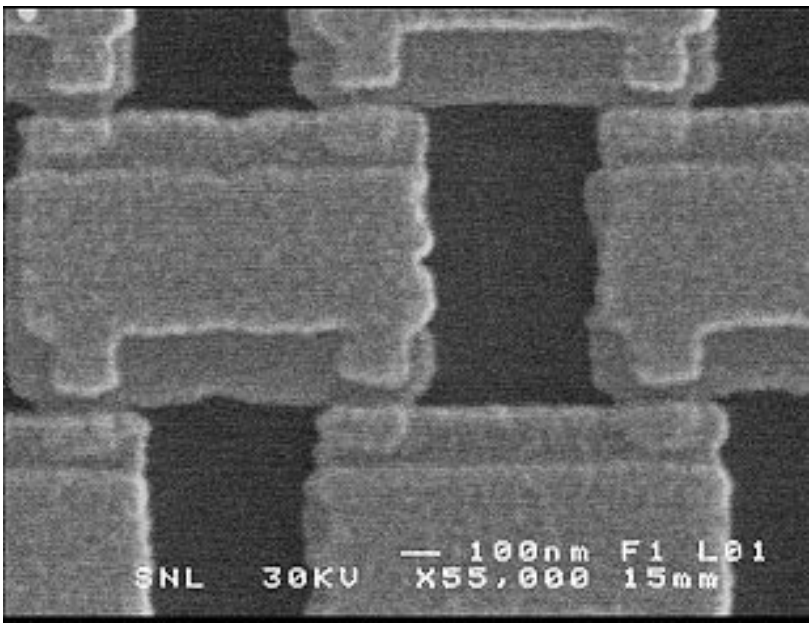
Threshold voltage and I-V characteristics measurements on two dimensional Josephson junction arrays



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Abstract

We have fabricated and measured two square two-dimensional Josephson junction arrays, each with 168x168 tunnel junctions. The junctions were made of Al-Al_2O_3-Al, fabricated with standard e-beam lithography and angle evaporation.

The first chip had a room temperature resistance of 27 kΩ per junction and showed a clear Coulomb blockade of approximately 200 μV. Several threshold voltage (V_t) measurements were made on this array, and some statistical analysis of V_t was made with histograms. The threshold voltage showed a periodic dependence on magnetic field with a period corresponding to frustration 1. Additional small peaks, which were periodic with period 0.57 in frustration were also observed, which were most likely due to some second loop size in the design of the arrays. Histograms of 10 000 V_t measurements sometimes displayed two or even three peaks, but only at low temperatures (<100 mK). The distance between those peaks was field dependent, however there was not enough data to determine weather or not it was periodic. The V_t measurements were carried out by ramping voltage over the array. The frequency of these ramps and the voltage where the ramp started, V_s, affected V_t in a complex way.

The second chip had a much lower room temperature resistance of 6.5 kΩ per junction. This sample displayed a Josephson-like behavior with a sharp critical current. There was only a very weak indication of Coulomb blockade at certain magnetic fields and no threshold voltage measurements were made on this chip. Several I vs. V_x and V_y curves were taken at different magnetic fields, where V_x is the normal voltage along the current and V_y is the Hall voltage perpendicular to the current. The zero bias resistance, $R_0 = \left.\frac{dV_x}{dI}\right|_{I=0}$, could then be calculated as a function of magnetic field. R_0 was periodic with a period corresponding to frustration 1, having dips in the resistance at frustrations 1/2, 1/3 and 2/3. There were some extra peaks as well, at the same frustrations as the peaks in the V_t measurement on the first chip, also having to do with the second loop size. At these peaks the I-V_x and I-V_y curves were discontinuous. The normal current jumped once, and the Hall voltage jumped twice with increasing current. The precise explanation of these jumps is still unknown.

Contents

1. Introduction

A Josephson junction is a structure consisting of two superconducting electrodes separated by a thin insulating layer, usually of the order of 2 nanometers in thickness. This structure is named after B.D. Josephson who predicted[1] the existence of a small current without any voltage drop. The junction is partly characterized by its Josephson coupling energy $E_J = \frac{\hbar}{2e} I_C$, where I_C is the critical current, which is the maximum zero-voltage current of the junction. If the junction is sufficiently small the charging energy $E_C = \frac{e^2}{2C}$, where C is the capacitance of the junction, becomes important. This is the energy stored in the electric field of a capacitor C with the charge ±e on its electrodes. Thus if a Cooper pair tunnels in an uncharged Josephson junction it will momentarily charge the junction with the charge ±2e, increasing the energy by $4E_C$. In a single junction this is usually not a problem because with some help from Heisenberg's uncertainty law, $\Delta E \Delta t \geq \hbar/2$, the charge slips quickly away from the junction, discharging it before the energy conservation law notices. But if there is any obstacle close after the junction, for example another junction or a resistor, the junction might stay charged long enough for the energy law to catch up. Then the tunneling will be suppressed and there will be no current without a little voltage to help. This is called the Coulomb blockade[2] of Cooper pair tunneling. In a simple model, Δt is the discharge time for the capacitor, $\Delta t = R_e C$, where R_e is the impedance of the junction environment, assumed frequency independent. The condition for Coulomb blockade is then $4E_C > \Delta E \geq \hbar/2\Delta t$, which implies $R_e > \hbar/4e^2 \approx 1\ k\Omega$.

In an array of Josephson junctions the tunneling behavior is partly determined by the ratio of E_J to E_C. If $E_J >> E_C$ there will be no Coulomb blockade and the array will be superconducting. If, on the other hand, $E_C >> E_J$, there will be a clear Coulomb blockade.

If a magnetic field is applied perpendicular to the array the behavior can usually be described in terms of frustration[3,4], provided that the array is homogeneous, i.e. the junctions, holes and superconducting "islands" are the same in the entire array, and provided that the array is considerably smaller than the Josephson penetration depth[5] (several mm in this case). Frustration is dimensionless and proportional to magnetic field. Frustration f=1 corresponds to one flux quantum, $\Phi_0 = h/2e$, in every loop in the array. Properties that depend on frustration are periodic ($f \rightarrow f+1$) for sufficiently low frustrations. At high enough fields other effects come into account, like the suppression of superconductivity.

One interesting effect is the frustration dependence of the zero-bias resistance (the resistance close to zero current), which decreases at integer as well as rational frustrations (1/2, 1/3, 2/3 etc.). The resistance can change by five orders of magnitude, just by changing the magnetic field slightly[6,7].

The threshold voltage also changes with frustration, as one measurement in this report shows. The threshold voltage is the minimum voltage required to start a current in an array with Coulomb blockade.

2. Experimental details

2.1 Fabrication

Two 2D-arrays were fabricated using standard e-beam technique. The mask layout was created with a CAD program and then transferred to an e-beam lithography machine. A two layer e-beam resist was used with a thick bottom layer and a thin, hard top layer. The bottom layer was 400 nm 10% copolymer (spin: 2000 rpm) baked on a hot plate for 5 min. in 170˚C. The top layer was 40 nm 1.8% 350k PMMA (spin: 3000 rpm) baked on a hot plate for 5 min. at 170˚C. The exposure dose was 270 $\mu C/cm^2$. After exposure the chips were developed in a mixture of isopropanol (CH_3-CHOH-CH_3) and water (H_2O) with the ratio 84:3 in an ultrasonic bath for about 1 min. The advantage of this recipe was that both layers were developed in a single stage in a non-toxic developer. However, the development time seemed to be rather sensitive to the ultrasonic bath power. While developing several chips, one at a time, the noise from the ultrasonic bath increased audibly. After that the development time was decreased by half.

A two layer resist was used to create bridges of e-beam resist over the chip surface. During development the bottom layer was developed quicker than the top layer and an undercut was created under the edge of the top layer. From an SEM image the undercut to was estimated to be approximately 130 nm at the chip surface. This undercut was enough to create bridges in the top layer where the distance between exposed areas was smallest. After development, Al was evaporated from two angles. During evaporation the pressure was about 10^{-4} Pa (10^{-6} mbar). A 200 Å layer was evaporated from an angle of 10˚ from perpendicular. Oxygen was then let into the evaporation chamber to a pressure of about 2 Pa (0.02 mbar). The first chip, H7#43, was oxidized for 5 min. and the second chip, H9#44, for 2 min. Then the oxygen was pumped out again and a second layer of Al, 350 Å, was evaporated from an angle of -10˚. This angle evaporation procedure was developed by Dolan[8] (figure 1). The resulting normal state resistance per junction was 33 kΩ and 7.6 kΩ for the two chips respectively.

2.2 Chip layout

The measured chips contained 2D tunnel junction arrays with 168x168 junctions. At the top and bottom the array was connected to a long solid bar extending along the entire side. At the sides were four Hall probes on each side at positions 1/6, 1/3, 1/2 and 5/6 of the distance from the top to the bottom bar. These Hall probes were connected through three tunnel junctions to the array. The size of the tunnel junctions were 100x200 nm. There were also tunnel junctions on the islands in series with the junctions between the islands, which were approximately 25 times larger than the small junctions and being strongly Josephson coupled they could generally be ignored. Figures 2 and 3 show SEM pictures of the entire array and close-ups of individual islands, a Hall probe and the top solid bar. Because the e-beam machine gives some stray exposure around the focus point, some unconnected islands were created near the left and right edges of the array to make sure that the exposure dose would be the same at the edge and inside the array. These are clearly seen as the bright areas at the left and right sides of the array.

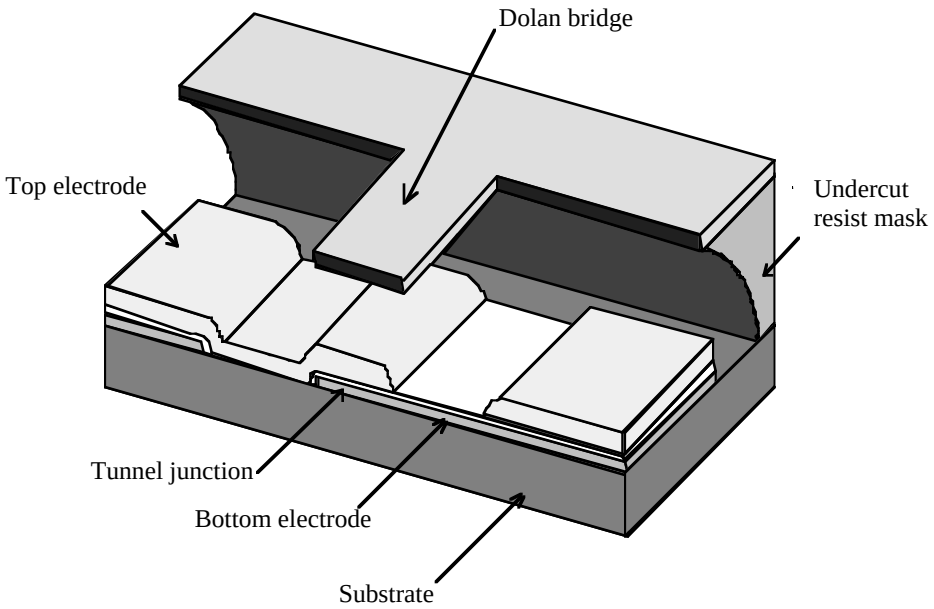
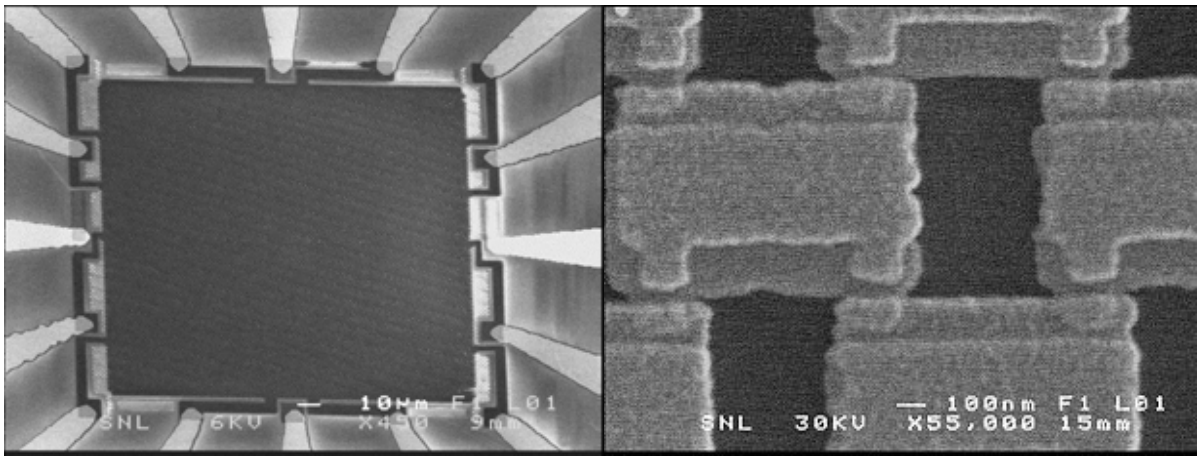


Figure 1. The Dolan bridge technique. After the first evaporation (from the right) the aluminum electrodes are oxidized to create a thin insulating Al_2O_3 layer. Then the second evaporation (from the left) will create a tunnel junction under the bridge. Picture courtesy of Peter Wahlgren©.

This table shows some parameters of the two chips reported in this thesis. They are calculated from a large scale I-V curve.

Sample	Array size	R_N (kΩ)	E_J/k_B (K)	E_C/k_B (K)
H7#43	168x168	33.0	0.215	0.693
H9#44	168x168	7.59	3.72	0.672



a *b*

Figure 2. Two SEM pictures of a 2D-array. (a) The entire array with the Hall probes on the left and right sides and two contacts on each of the solid bars at the top and bottom of the array. (b) A close-up of a few Al islands, each connected to four other islands by tunnel junctions. The size of the tunnel junctions is approximately 100x200 nm and the unit cell area, i.e. one loop (dark) and one aluminum island (gray), is 0.8x1.6 μm=1.3 μm².

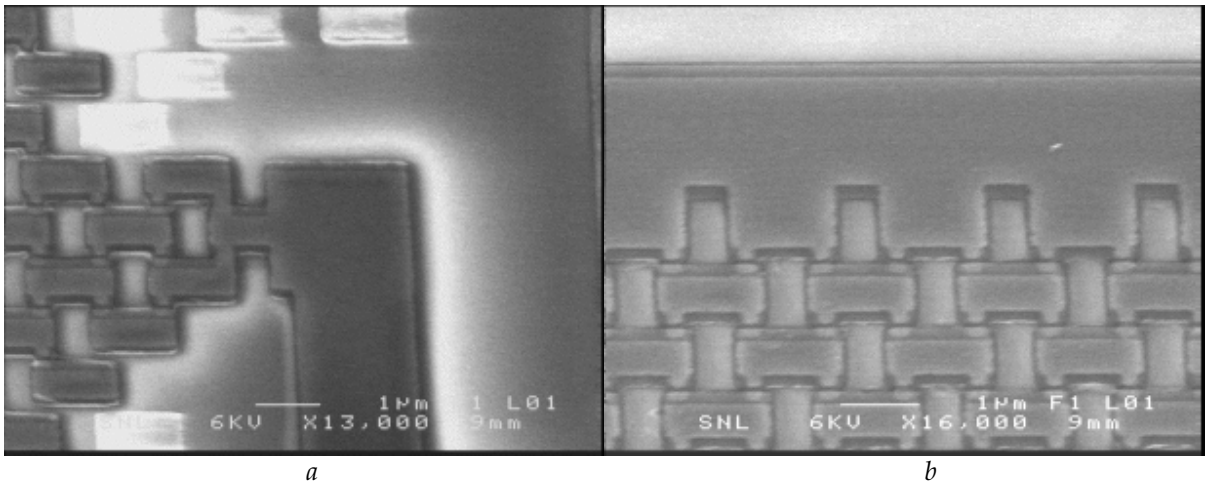


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Figure 3. Two close-up SEM pictures of a 2D-array. (a) The Hall probes are connected through three tunnel junctions to the array. The bright areas are isolated aluminum islands that get charged by the SEM. (b) The connecting bar at the top of the array. Note that the topmost loops are physically the same size as the rest of the loops. However, because the London penetration depth is of the order of the island dimensions, and the flux expelled from the bar is collected by the topmost loops, the effective loop size is actually larger, giving rise to a shorter period in magnetic field.

2.3 Measurement techniques

The measurements were carried out in a dilution refrigerator which was situated in an electrically shielded room. All digital equipment was situated outside of this room, and the digital ground was separated from the measurement ground with isolation transformers. The signals were amplified in an amplifier box located on top of the cryostat in order to minimize external pickup in the leads. The voltage across the sample was applied in one of to ways: in R-bias mode, the DC voltage was applied over two current measurement resistors in series with the sample; in V-bias mode the DC voltage over the sample was fixed by regulating the voltage with a feedback circuit.

The threshold voltage measurements were carried out using a sample-and-hold circuit specifically built for this purpose. This circuit would detect the moment when the current jumped from zero to a finite value. At that moment it would sample and hold the input voltage, giving a constant voltage to a voltmeter and sending a trig pulse to the same voltmeter. The voltage over the sample was ramped from a starting value, V_S, to 860 µV. The voltage ramp was generated by a function generator, and the frequency was varied between 2.4 Hz to 76.8 Hz (see figure 4). One V_t measurement was made in every period.

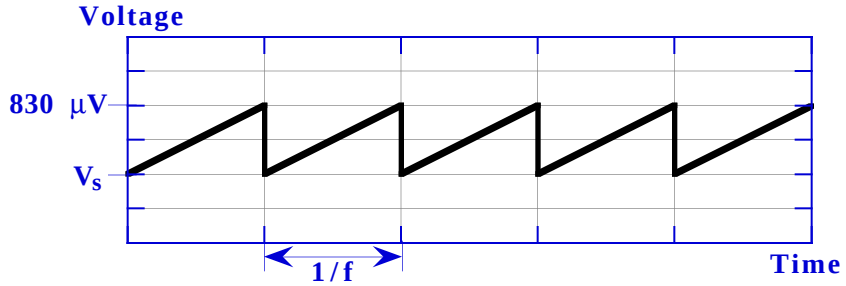

Figure 4. The voltage ramps used for the threshold voltage measurements.

3. Results

3.1 Threshold voltage

This section discusses some results from measurements of the threshold voltage V_t on chip H7#43. The array exhibits a sharp nonlinearity where the current jumps from essentially zero to a finite value (figure 5). The experimental definition of V_t is the voltage where the current rises above the noise level, which is of the order of 25 pA.

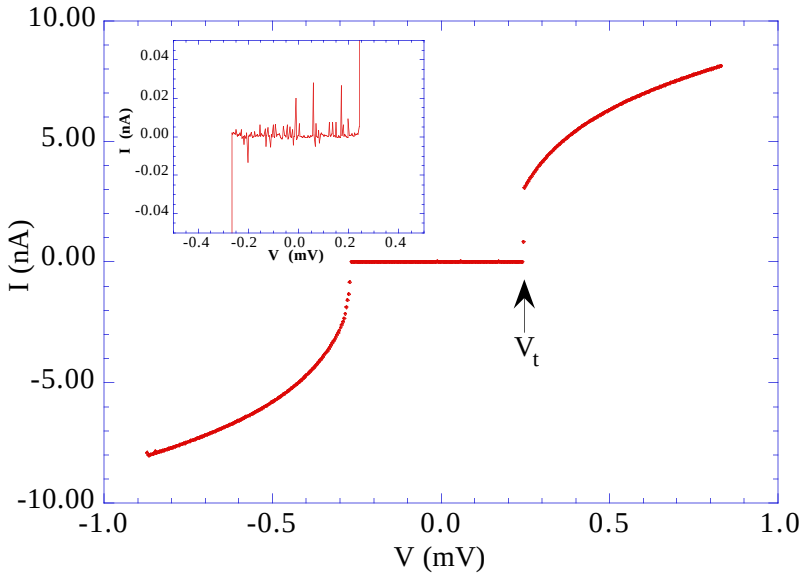

Figure 5. I-V curve for chip H7#43. V_t is the voltage where the current jumps from zero to a finite value. This curve is taken at lowest temperature (<20 mK) in zero magnetic field in V-bias mode. The curve was swept from low to high voltage. The inset is a magnification of the blockade regime to show the current noise level.

The ramp was run 10 000 times so that several Vt values could be collected and a histogram could be made. Figure 6 displays an example histogram. We discovered that sometimes two or even three peaks appeared in the histograms. The reason for this is unknown.

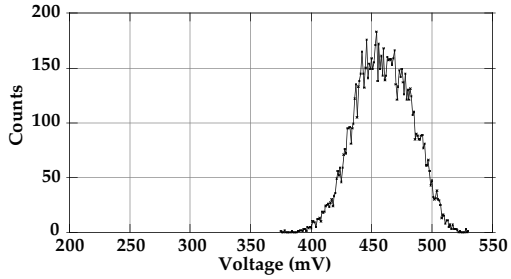

Figure 6: Example histogram from chip H7#43. This is at B=-0.94 mT, f=19.2 Hz, V_s=85.7 μV and lowest temperature. This histogram has a gaussian distribution and a mean value of about 460 μV.

Four parameters were varied during these measurements: frequency (f), magnetic field (B), starting voltage (V_s) and temperature (T).

3.1.1 Magnetic field dependence

Measurements by Delsing et al[9] on similar arrays have shown that for low magnetic field, V_t varies periodically with the field. At higher fields (25-40 mT) V_t increases and then decreases to the normal state V_t. The measurements in this report were all made at fields less than 5 mT and only the periodic behavior was observed, with a period of 1.62 mT. This period corresponds to a frustration of 1. Frustration is defined as $f=BA/\Phi_0$, where A is the area of one unit cell in the tunnel junction array and $\Phi_0=h/2e$ is the magnetic flux quantum. A unit cell is the total area of the array divided by the number of loops. The unit cell is independent of the London penetration depth, because the magnetic flux expelled from the islands in a 2D-array does not leave the array, but is collected in the loops. The effective unit cell area thus becomes the area of one loop plus the area of one island. Taking the area in the SEM picture (figure 2b), $A=1.3\ \mu m^2$, the expected period $B/f=\Phi_0/A=1.6$ mT is in excellent agreement with the measured period. The difference between high and low V_t is about 0.1 mV, which is easily measurable. Figure 7 shows several I-V curves taken at frustrations from -1.2 to 0.5. They are measured in R-bias mode and therefore there is no current jump in the graph. The curves are very noisy below 1 nA because the current actually switches rapidly between two points on the loadline determined by the two current measurement resistors. In V-bias mode there is no switching and all V_t measurements were made in V-bias mode.

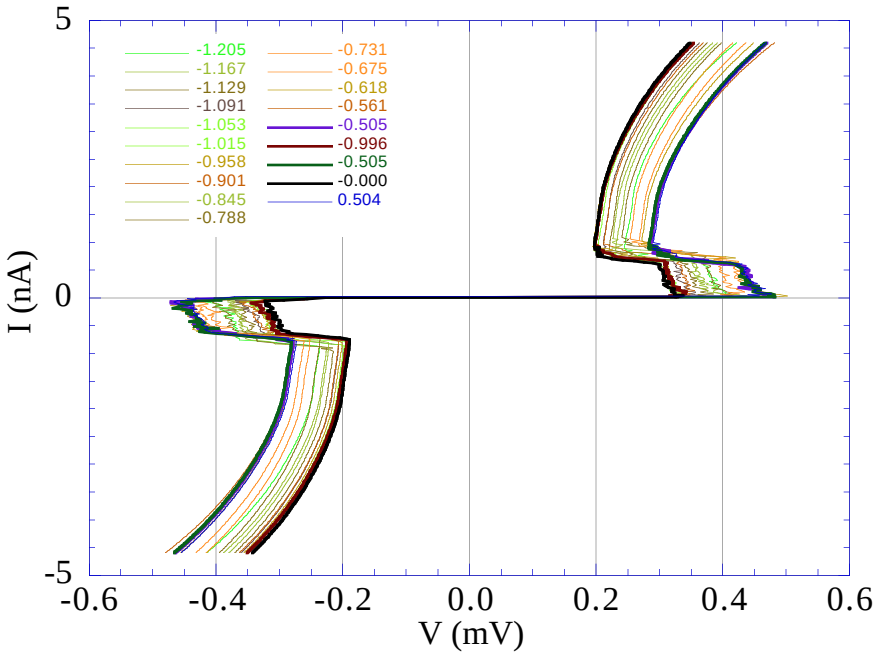

Figure 7. I-V curves for chip H7#43 at different frustrations. Frustration 1 corresponds to a magnetic field strength of 1.62 mT. These curves are taken at lowest temperature in R-bias mode.

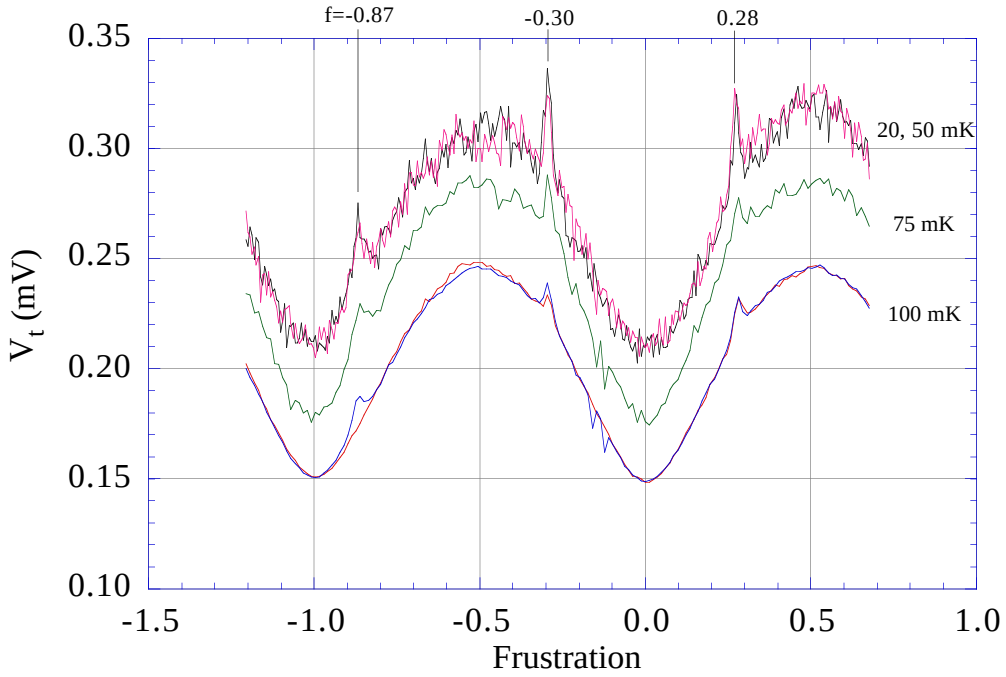

Figure 8. V_t vs. frustration for chip H7#43. The threshold voltage varies periodically with frustration. The peaks at f=-0.87, -0.3 and 0.28 are due to a second SQUID loop size. The threshold decreases with increasing temperature but the peaks are still present at 100 mK.

Figure 8 shows the periodic dependence of V_t at four different temperatures. Higher temperature gives lower V_t, but the periodic behavior is still clear at 100 mK. However, there are a few peaks that appear with a period of 0.57 frustration units. These peaks are most likely due to a second effective loop size at the top and bottom of the array, and in a zero-bias resistance (R_0) measurement on chip H9#44, extra peaks appear at the same frustration values (see figure 14). They look a little shifted to the left, and even more so in the R_0 diagram, but this could just be due to measurement errors or too few sampling points.

Some histograms show more than one peak (see figure 9). Multiple peaks appear at temperatures lower than 100 mK, but other than that there is no clear pattern. In figure 9 the second peak is always smaller than the first, but that is not a general rule. Triple peaks have even been observed. The distance between the peaks, ΔV_t, is sometimes hard to determine, but it seems that it is dependent on magnetic field. In figure 10, ΔV_t has been measured at two temperatures and seven magnetic fields, spanning a frustration slightly less than 1. It is clear that ΔV_t changes with B, but whether or not it is periodic cannot be deduced, nor if the period is the same as the mean V_t period, 1.6 mT.

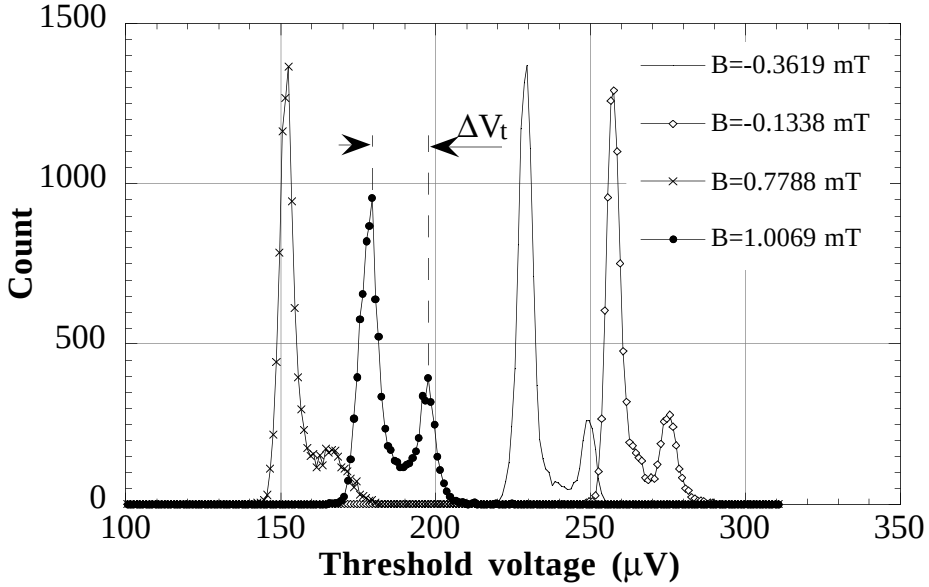

Figure 9. Histograms for chip H7#43. Sometimes double peaks appear in the threshold voltage. The distance between the peaks is defined as ΔV_t. Measurement taken at T=50 mK and f=57.6 Hz.

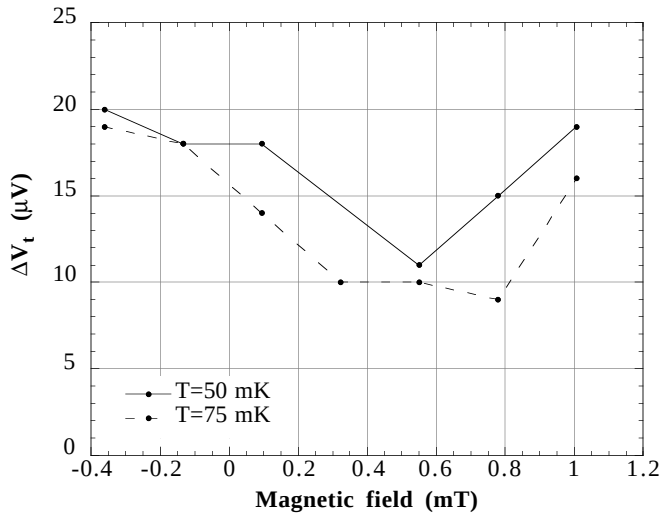

Figure 10. Chip H7#43. The distance between double peaks seems to vary with magnetic field. Even though there are only a few points it is quite clear that ΔV_t depends on B. The magnetic field spans less than one frustration and whether or not it is periodic is too early to tell. The solid line is at 50 mK and the dashed line is at 75 mK.

3.1.2 Starting voltage, V_s

The threshold voltage increases distinctly with V_s. In figure 11, which shows several histograms, V_t increases by almost a factor two as V_s is increased. The reason for this might have something to do with excess charges in the array. When the ramp starts at low V_s there is a negative current and a lot of charges are present in the array. When the voltage increases above zero there are charges already present in the array to start the current by positive and negative charge solitons[10] annihilating each other, but when the ramp starts at high V_s there are charges left from the positive current in the array and to start the current solitons must be injected in the array, which requires higher energy.

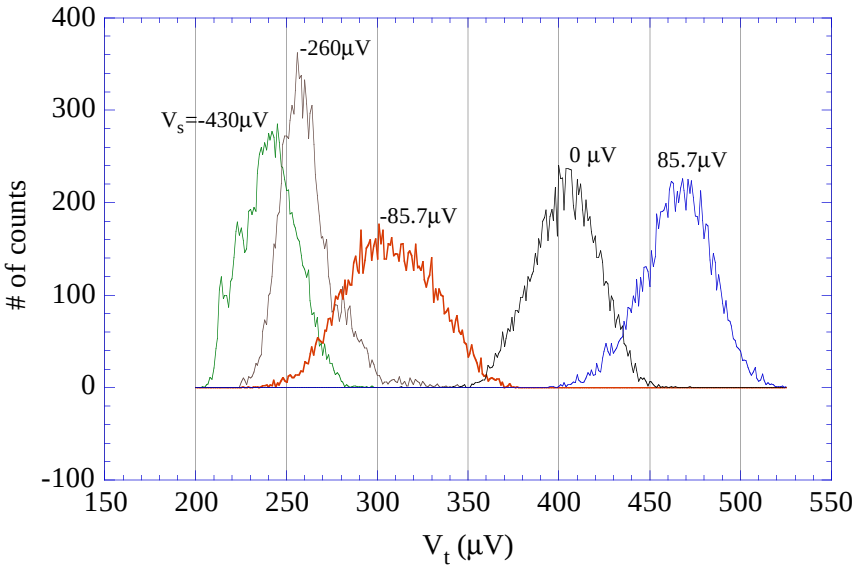

Figure 11. Histograms for chip H7#43. The threshold voltage increases with the starting voltage of the ramp, V_S. This measurement was taken at T=50 mK, B=-1.5 mT and f=76.8 Hz.

3.1.3 Temperature dependence

Generally the threshold voltage decreases with increasing temperature as shown in figure 12. Sometimes, especially when the histograms have double peaks, V_t is lower at base temperature (<20 mK) than at 50 mK. At 75 and 100 mK V_t always decreases substantially. See also figure 8.

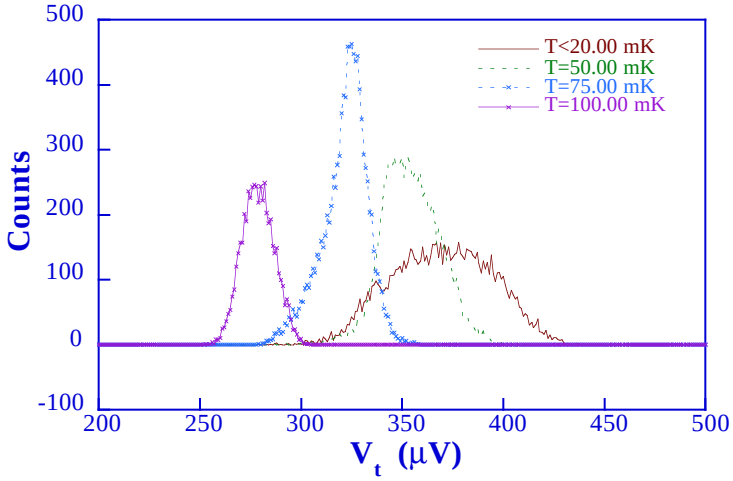

Figure 12: The threshold voltage decreases with higher temperature. Measurement parameters : B=-0.67 mT, f=76.8 Hz, V_S=-260 μV.

3.1.4 Frequency dependence

The frequency dependence is rather complicated. At low V_S the threshold voltage decreases with increasing frequency, but at high V_S it increases with higher frequency. At still higher V_S it seems that V_t is independent of frequency. This is consistent with the picture with excess charges in the array. There is a competition between the relaxation time of the charges and the time spent in the zero-current state. At low V_S there are charges left from the negative current, giving lower V_t, but at low enough frequency those charges will have time to relax by diffusing out of the array or annihilating each other before the voltage reaches the threshold voltage. At higher V_S the charges left are from the positive current, which will increase V_t unless the charges have time to relax. Figure 13 shows several histograms with different frequencies and V_S. In the third graph (V_S=-85.7 μV) the histogram for 38.4 Hz is approximately halfway relaxed. We can estimate the relaxation time ≈ the time it takes for the voltage to rise from V_S=-85.7 μV to V_t≈240 μV, knowing that the ramp stops at 860 μV: $T_R \approx \frac{240\,\mu V + 85.7\,\mu V}{38.4\,Hz \cdot (860\,\mu V + 85.7\,\mu V)} \approx 0.01\,s.$

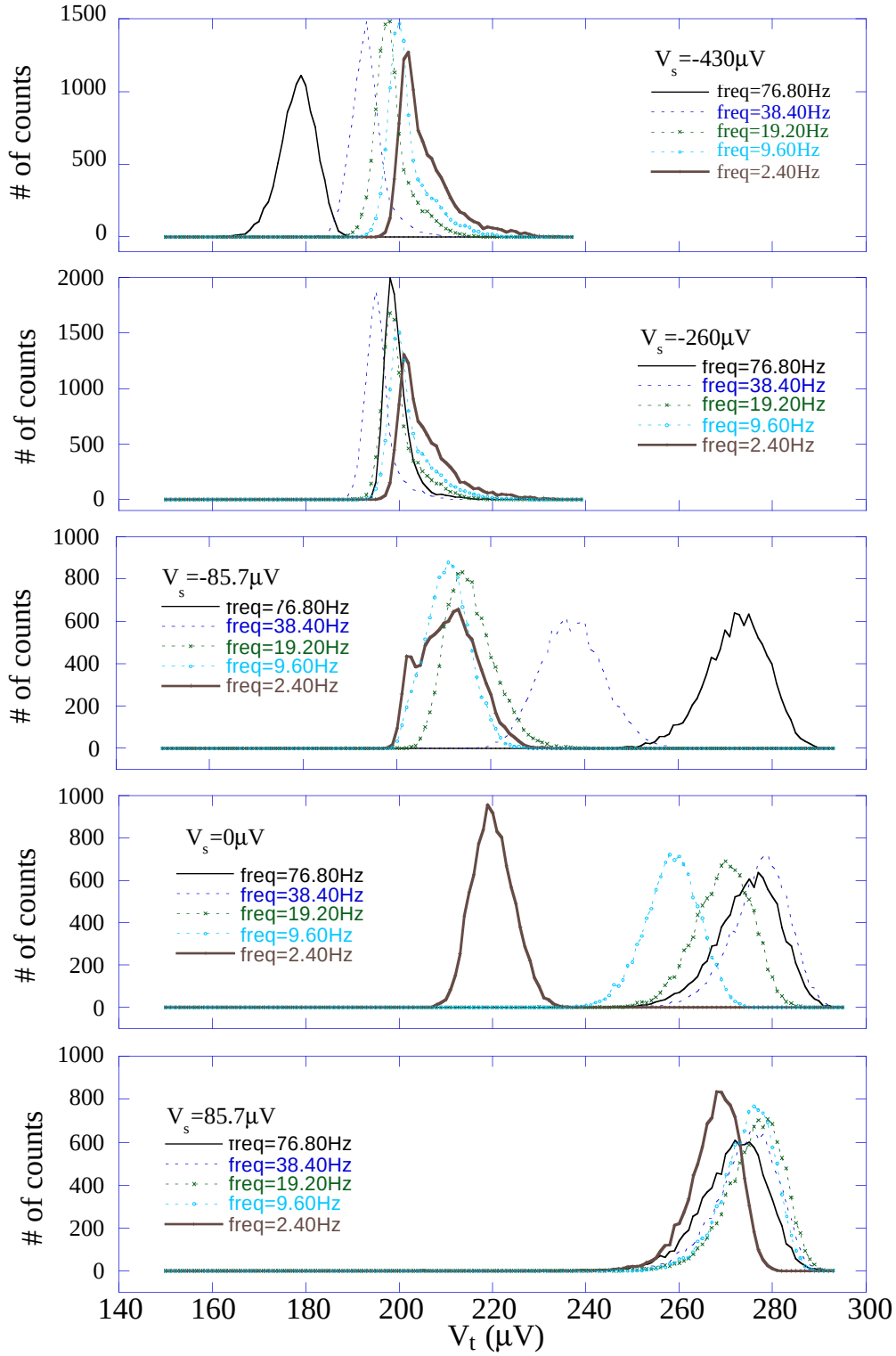

Figure 13. The threshold voltage depends on frequency in a complicated way: At low V_s the threshold is lower for higher frequency; at higher V_s the situation is reversed. It seems that at still higher V_s the threshold is the same for all frequencies. T=100 mK, B=-1.5 mT.

3.2 Zero-bias resistance

A number of I vs. V_x and V_y measurements were taken on sample H9#44, at different magnetic fields. The current, I, ran from the top to the bottom bar, the normal voltage, V_x, was measured between the same bars and the Hall voltage, V_y, was measured between the two middle Hall probes (see figure 2a). This sample showed no threshold voltage, but an applied magnetic field affected the I-V curves in a periodic manner.

By measuring the slope of an I-V_x curve at almost zero current the zero-bias resistance, R_0, can be calculated. The result is displayed in figure 14, which shows R_0 vs. frustration, where frustration 1 corresponds to magnetic field strength 1.62 mT. The resistance goes down to zero at integer frustrations and decreases at rational frustrations, 1/2, 1/3, 2/3 and so on. This is in agreement with previous measurements by van der Zant et al[7] and Chen et al[6].

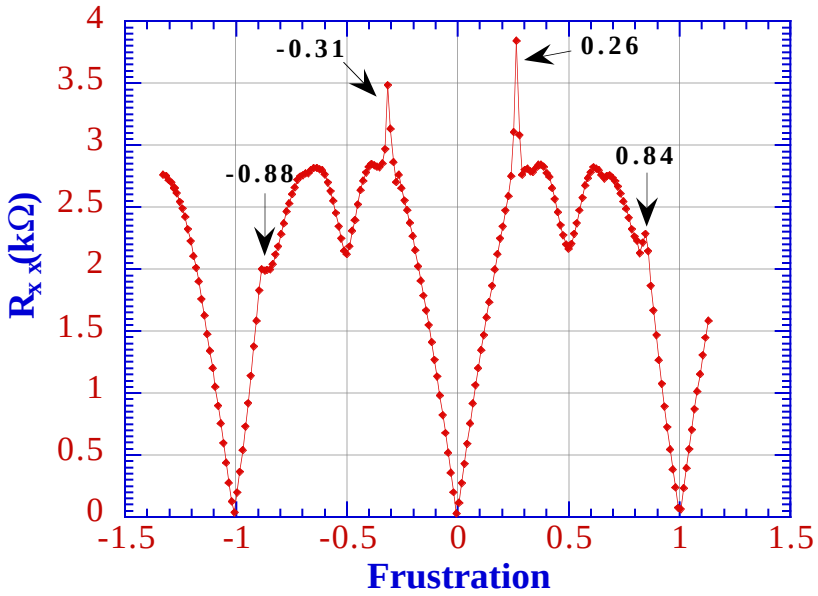

Figure 14. The zero bias resistance depends on the magnetic field with a period of 1.62 mT, corresponding to frustration 1. At f=1/2 the resistance goes down and also slightly at f=1/3 and f=2/3. The structure at f=-0.88, -0.31, 0.26, 0.84 has a different origin.

There are a few extra peaks in figure 14, at frustrations -0.88, -0.31, 0.26 and 0.84. They have a period of about 0.57 frustration units. Note that the threshold voltage measurements on chip H7#43 showed similar peaks at the same frustrations (see figure 8). The explanation has most likely to do with loops with bigger effective area than A, which would give shorter periods. At the solid bars at the top and bottom of the array are some loops with the same physical area as the loops inside the array (see figure 2b). However, those loops will collect some of the magnetic field that is expelled from the bars (Meissner effect), increasing the effective area. The London penetration depth may be bigger in the bars than in the Al islands, increasing the effective area even more. Similar phenomena has been observed in one-dimensional arrays of SQUIDs by Haviland[11].

We can make a rough estimate of the effective loop area at the bar from figure 3b. If half of the magnetic flux in the bar is expelled to the loops, the area added to the effective area will be approximately 0.5 μm x 1.6 μm = 0.8 μm^2, and the total effective area of those loops is 2.1 μm^2, compared to A=1.3 μm^2. The calculated period is then 1.3/2.1=0.62, in good agreement with the measured value of 0.57.

3.3 Current-voltage characteristics

At some magnetic fields the I-V_x and I-V_y curves became discontinuous. In figure 15 the voltage jumps by 150-200 μV, both in the I-V_x and the I-V_y diagrams. This is of the same order as the superconducting gap in aluminum, Δ_{Al}=175 μeV.

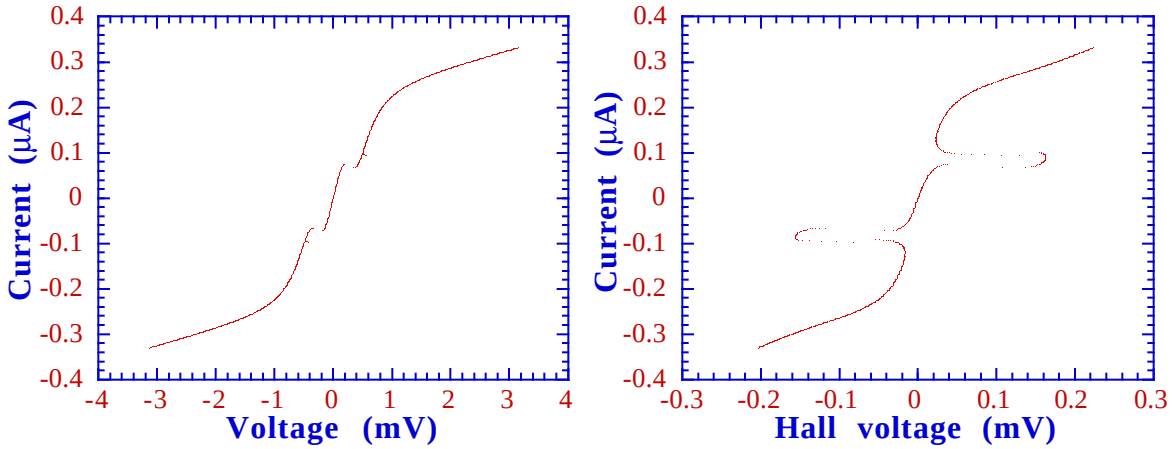

Figure 15. The I-V_x and I-V_y curves at B=-1.26 mT (f=-0.88). The origin of the discontinuity in the I-V_x and I-V_y curve at this and several other magnetic fields is still unclear. At these fields the zero bias resistance R_0 increases slightly. The curves are swept from negative to positive current and the temperature was lower than 20 mK.

The discontinuous IV curves appear only around those special peaks in the R_0 vs. frustration diagram. The current at which the discontinuity appear is smallest at these peaks, increasing at both higher and lower frustrations (figure 16). Above the critical current of the array (~0.25 μA) the discontinuity disappears. The I-V_x curve looks like there is a critical current in the loops at the bars that is almost suppressed at those magnetic fields, but that does not explain the strange discontinuities in the I-V_y curve.

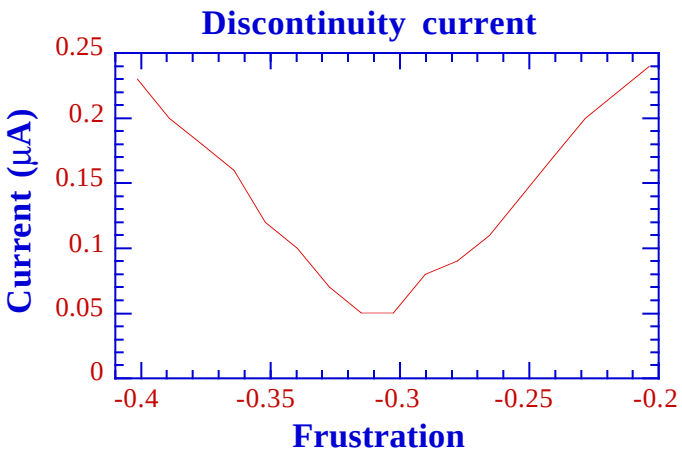

Figure 16. The current at which the IV curve is discontinuous is lowest at the peaks in the R_0 diagram. Outside of this diagram the discontinuity disappears. This is at positive current, but the negative side is approximately the same.

A close-up on the discontinuities reveal another detail: at the current where the Hall voltage makes a negative jump the bias point of the I-V_x curve jumps to a lower current. Figure 17 shows a close-up of the I-V_x and I-V_y curves at B=1.48 mT. Note that, in contrast with figure 15, at this field the Hall voltage jumps negative first and then positive. In figure 15 the first jump was positive and the second negative. A positive jump in V_y is always associated with a positive jump in V_x. A negative jump in V_y is associated with a jump in the bias point to lower current. If you look closely at figure 15 you will see the small jump, but this time at a higher current than the large one. Generally on the left side of the R_0 peaks the first jump in V_y is positive, but on the right side, at higher fields, the first jump is negative.

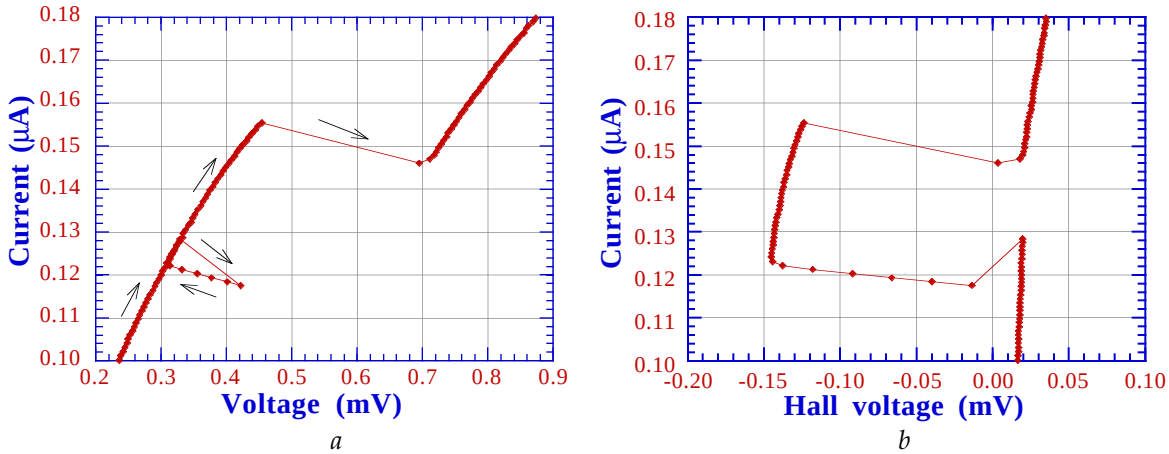

Figure 17. Magnifying the discontinuous part of the I-V_x and I-V_y curves reveals a small jump in the I-V_x curve at the current where V_y makes a negative jump. The magnetic field is 1.48 mT.

A Hall voltage, V_y, means that vortices are have a velocity component parallel to the direction of the current. The jumps in V_y means a sudden change in the Hall angle, defined as $\arctan(V_y/V_x)$. The I-V_x curve indicate a suppression of the critical current at the junctions closest to the bars. Perhaps injection of vortices at the end of the bars when this critical current is exceeded can explain the Hall voltage.

4. **Conclusions**

This report raises many questions and gives few answers. For example, why do the threshold voltage histograms sometimes have multiple peaks? And why does the distance between those peaks change with magnetic field? And does this distance depend periodically on the field? The peaks in the V_t vs. B and R_0 vs. B diagrams are most likely due to second loop sizes in the array. But how can this give rise to a sudden Hall voltage? Future experimental and theoretical work will answer these questions.

The complex frequency and starting voltage dependence of the threshold voltage can probably be explained by the relaxation of excess charges in the array. Future experiments could try to measure the relaxation time and which parameters that affect this time.

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Merry Christmas and a happy new year!