

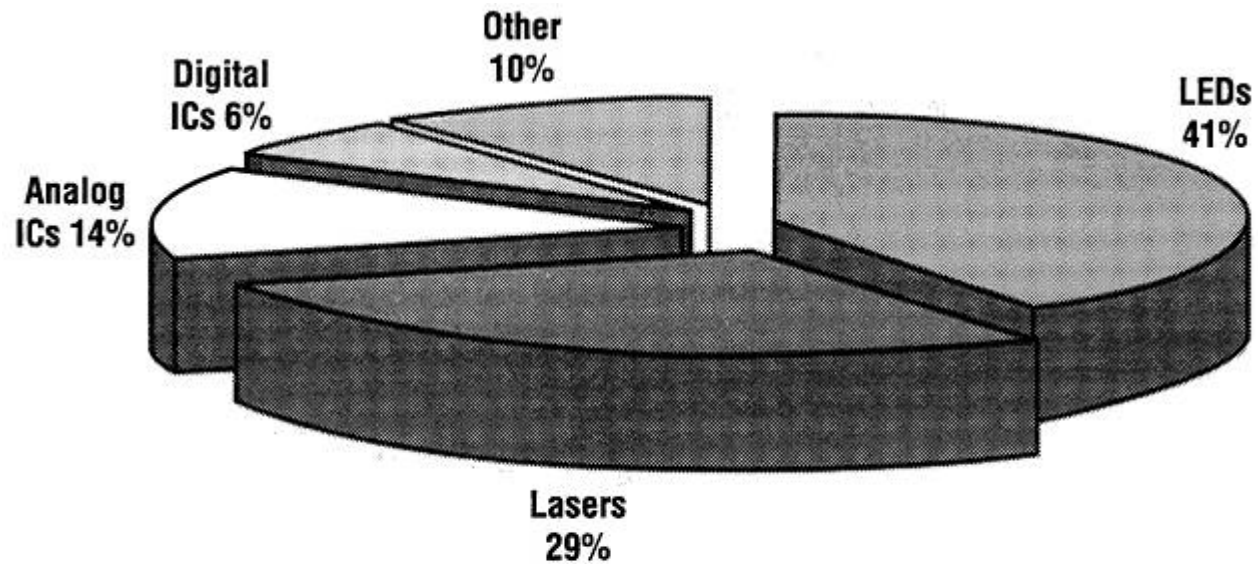
# DEVICE TECHNOLOGY & PACKAGING

Göran Alestig

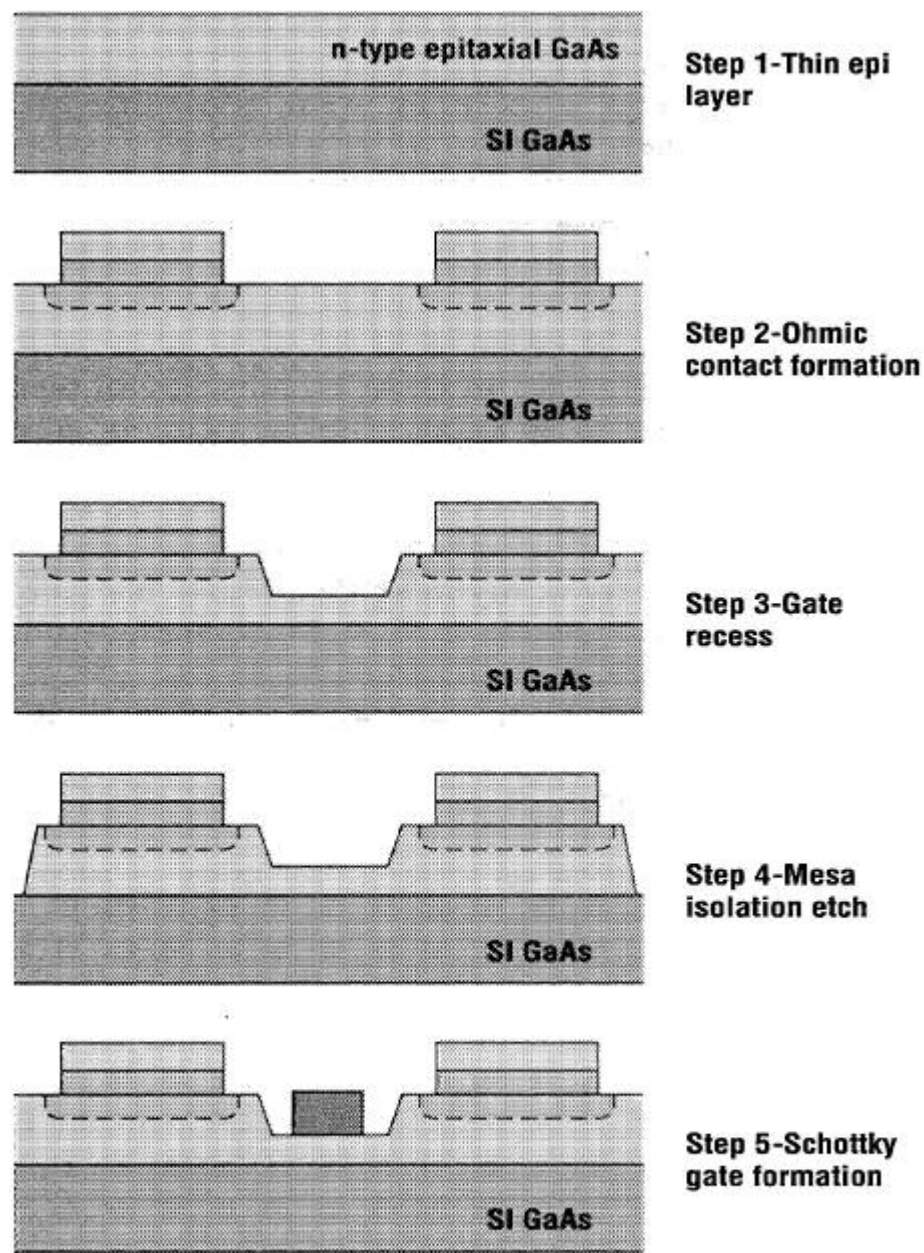
- MOS devices
- Silicon Bipolar technology
- Design and layout considerations
- **GaAs and other III-V devices**
- Packaging
- Reliability

## GaAs and other III – V technologies

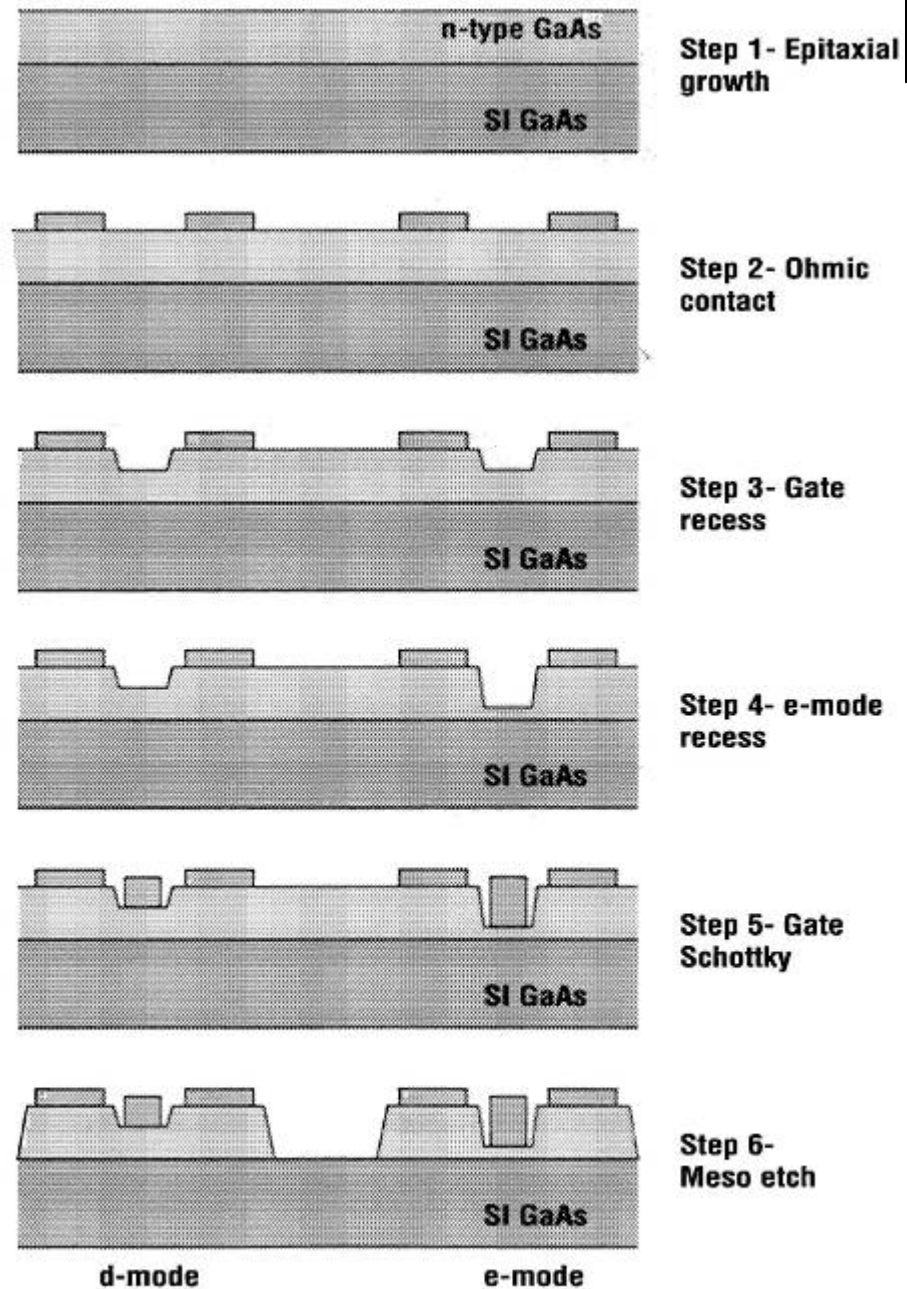
- No insulating oxide
- MESFET => Schottky contact on gate
- Can use semi-insulating high-resistivity substrate
- High electron mobility => high speed devices
- Direct bandgap => opto devices



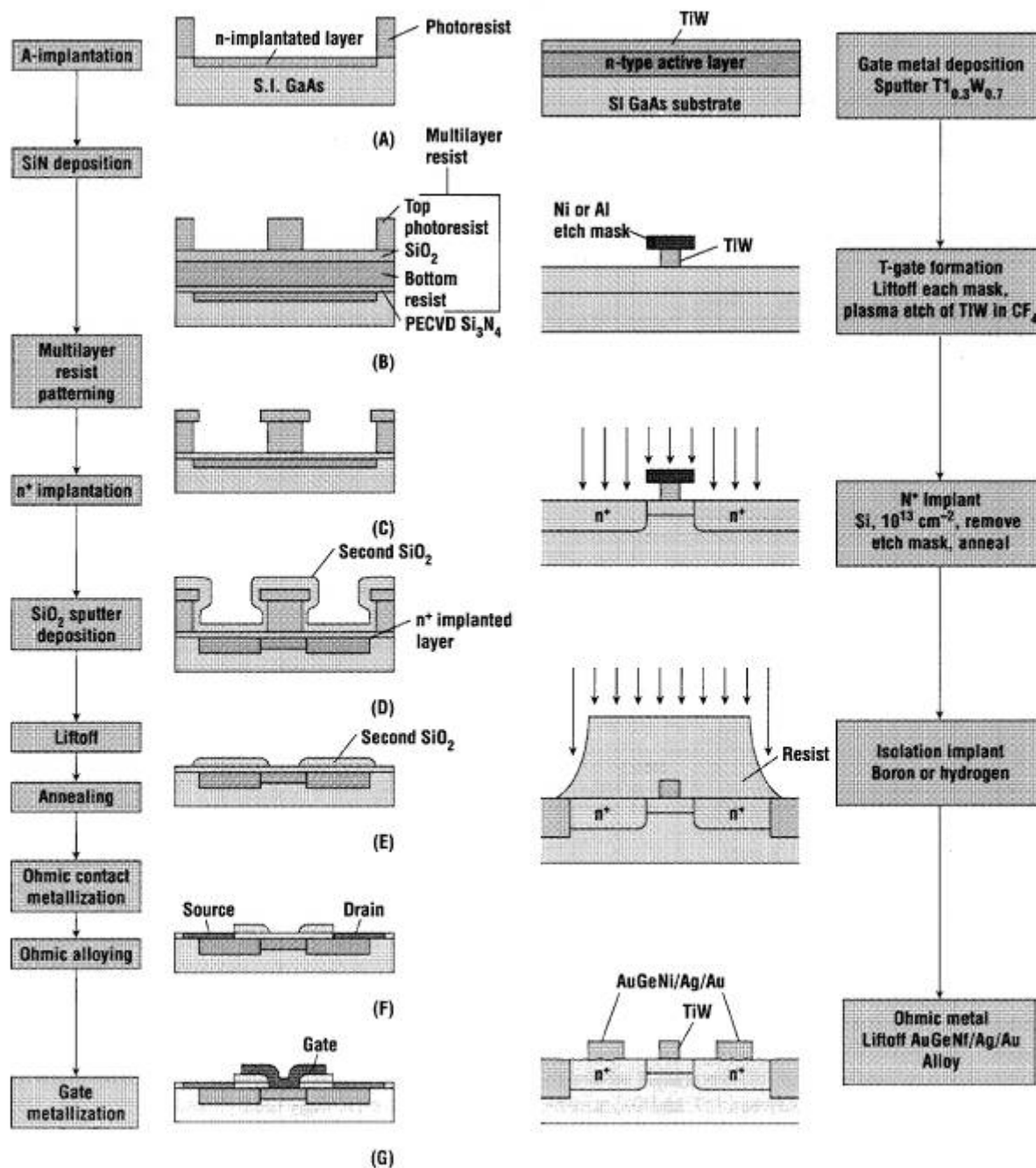
**Figure 17.1** Pie diagram of application areas for compound semiconductor devices.



**Figure 17.3** Process flow for a simple mesa-isolated MESFET. The first step can be replaced with an Si implant and anneal as discussed.

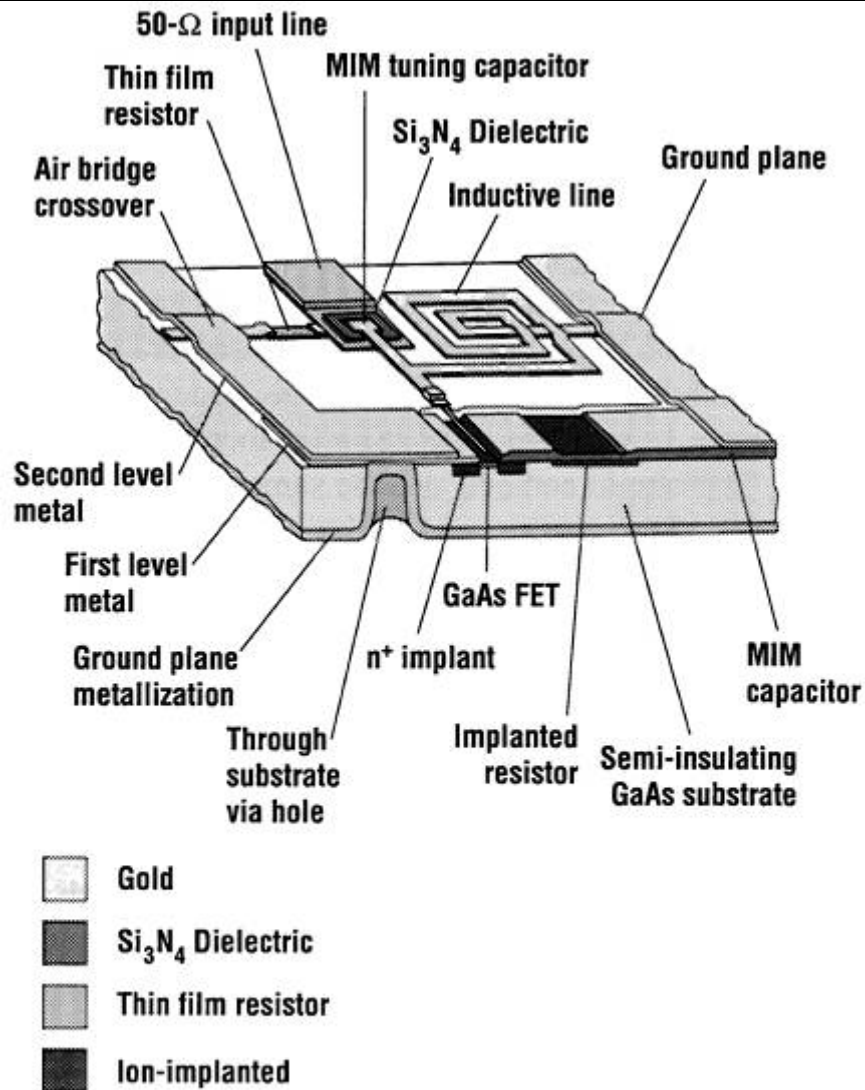


**Figure 17.5** Process flow for an etched-channel E/D technology.



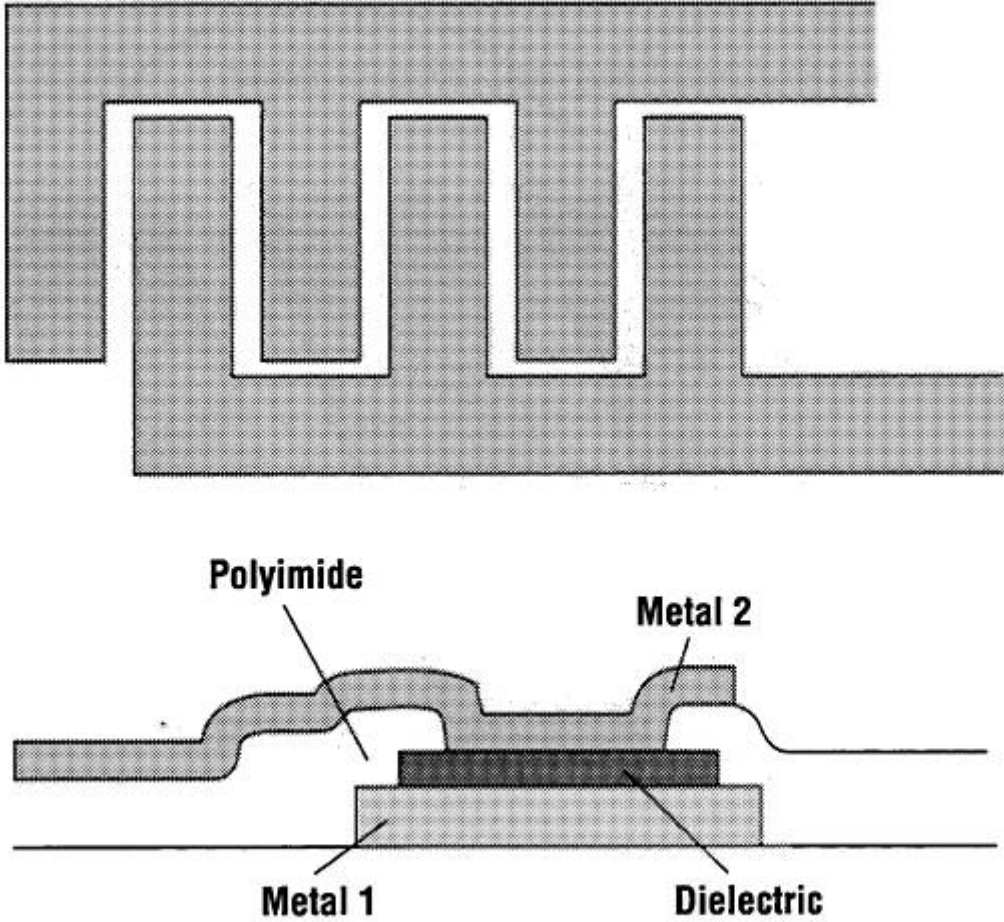
**Figure 17.6** The self-aligned gate process implantation N<sup>+</sup> technology (SAINT) (after Yamaski et al., ©1982 IEEE) and the T-gate process. The order of the last two steps of the T-gate may be reversed to reduce any isolation degradation.





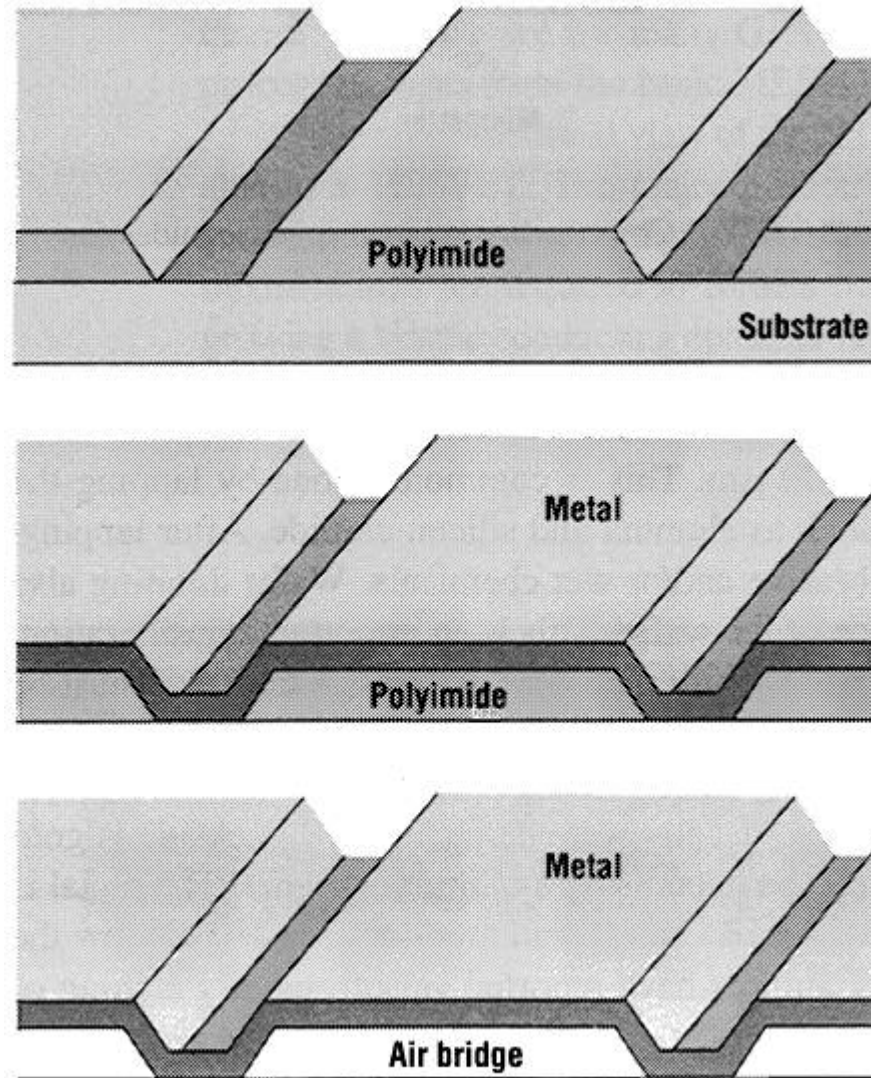
**MMIC = Monolithic Microwave Integrated Circuit**

**Figure 17.8** Cross-sectional view of a typical MMIC (after Decker).

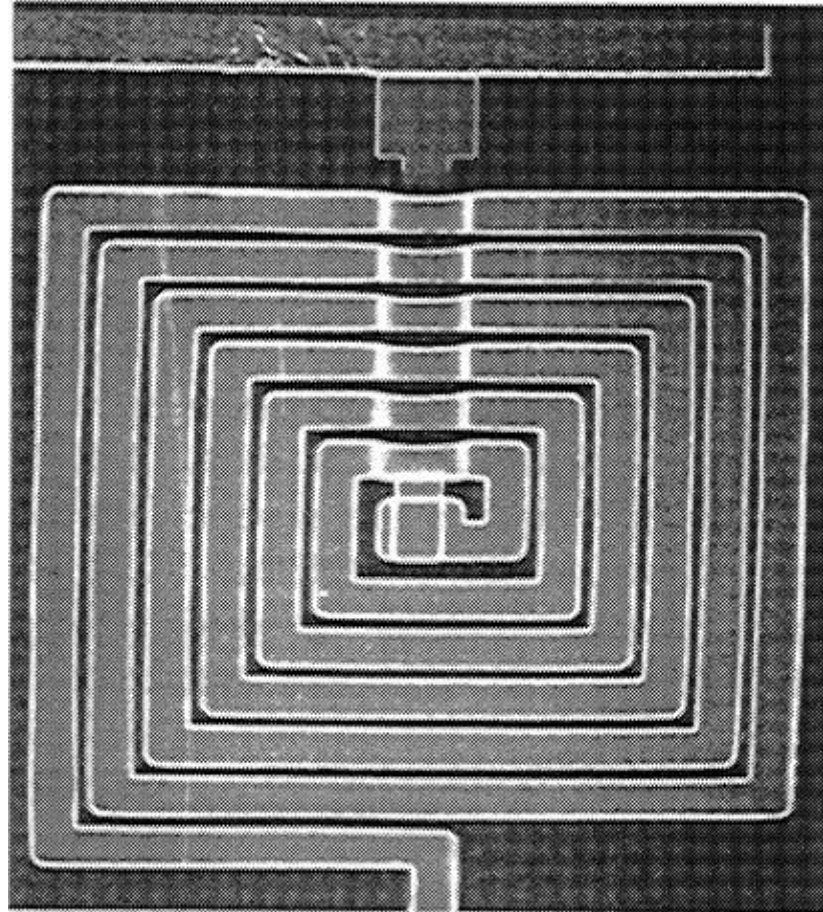


**Figure 17.9** Interdigitated and simple overlay capacitor.

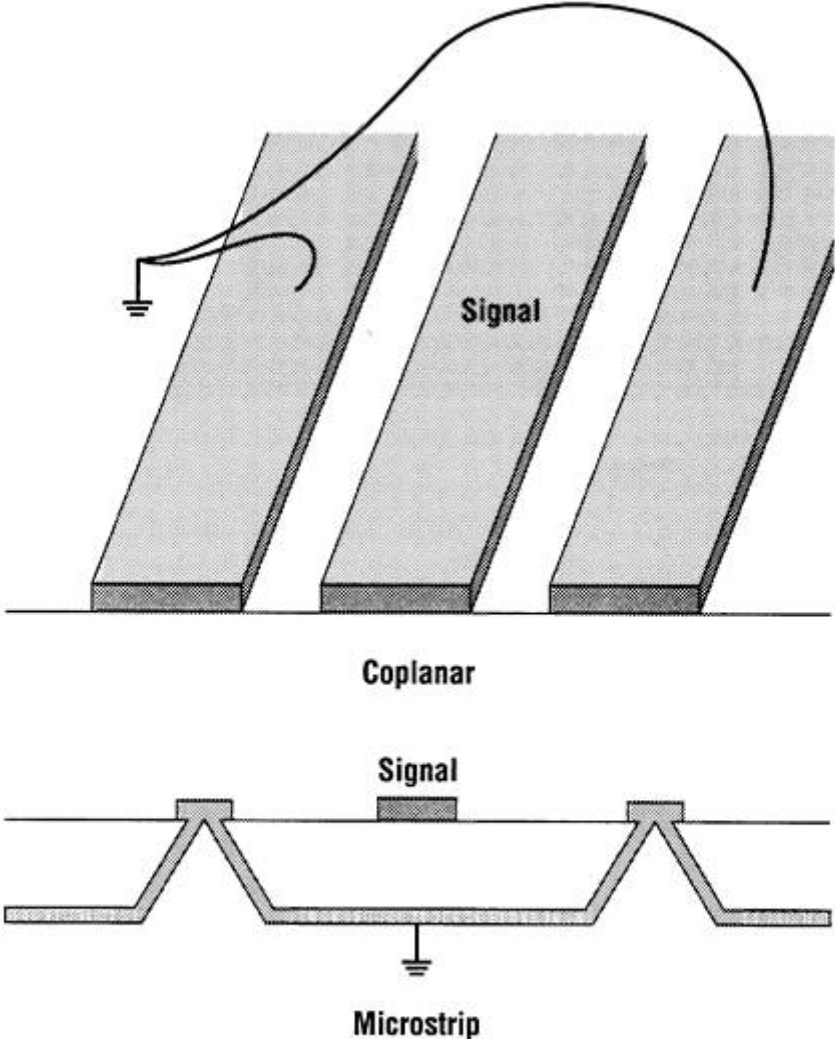




**Figure 17.10** Air bridge process flow.



**Figure 17.11** Completed spiral inductor using an air bridge crossover (after Sciater, reprinted by permission, TAB Books, Inc.).



**Figure 17.12** Coplanar and microstrip waveguides for MMIC interconnect.

Lots of interest in recent years for InP-based devices  
 => Better performance at very high frequencys ( > 100 GHz)

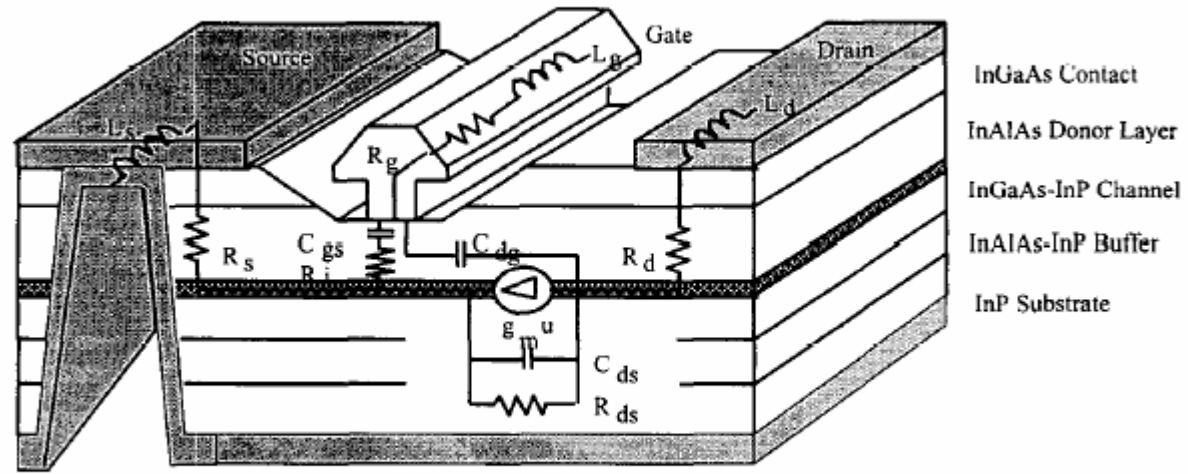
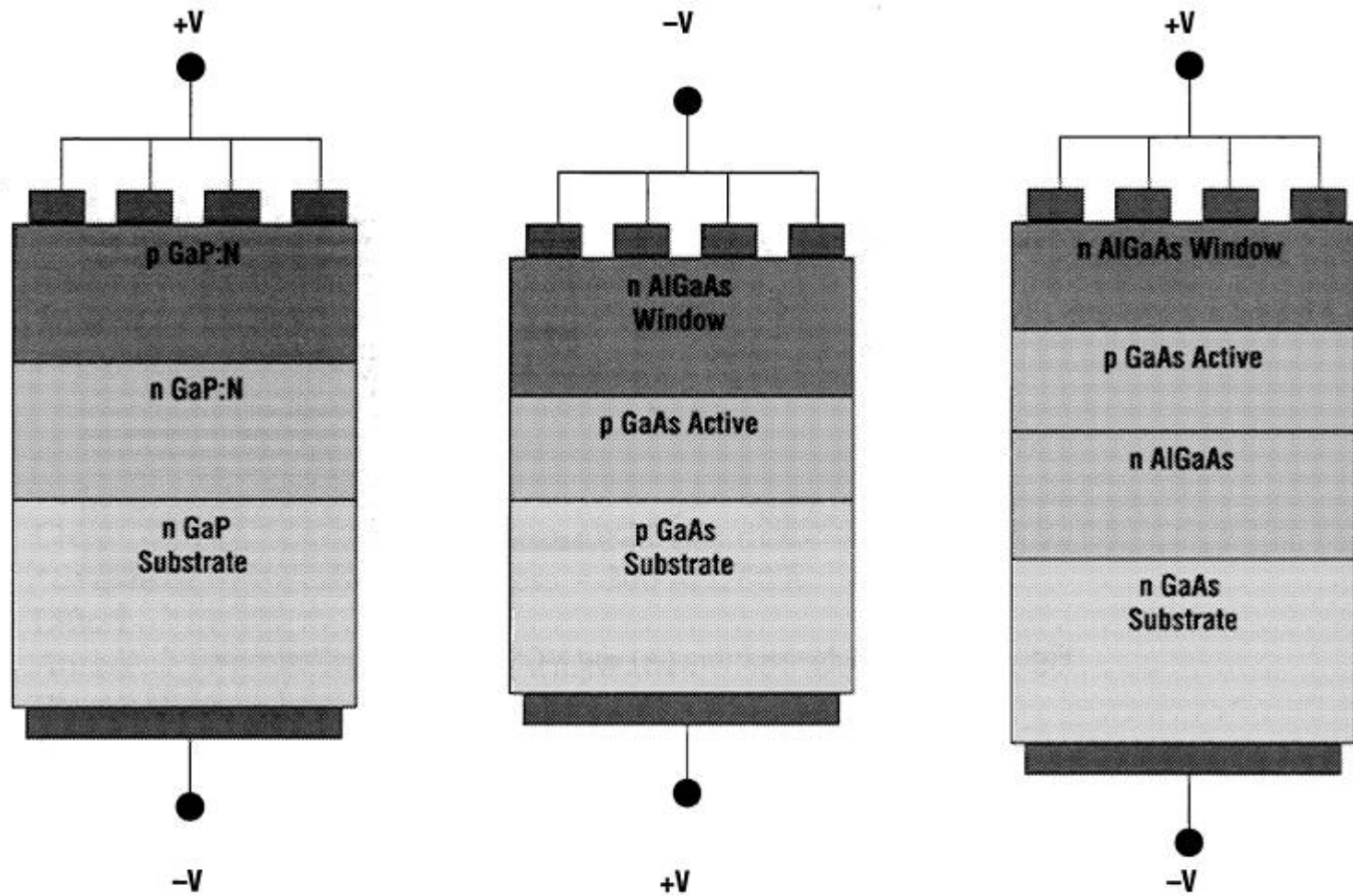


Fig. 1. Baseline pseudomorphic InP HEMT device profile.



**Figure 17.14** Typical homojunction (A), single barrier (B), and double barrier (C) LED structures. If backside contact is not desired, the stack can be etched down to the substrate and a top side substrate contact added.

