

DEVICE TECHNOLOGY & PACKAGING

Göran Alestig

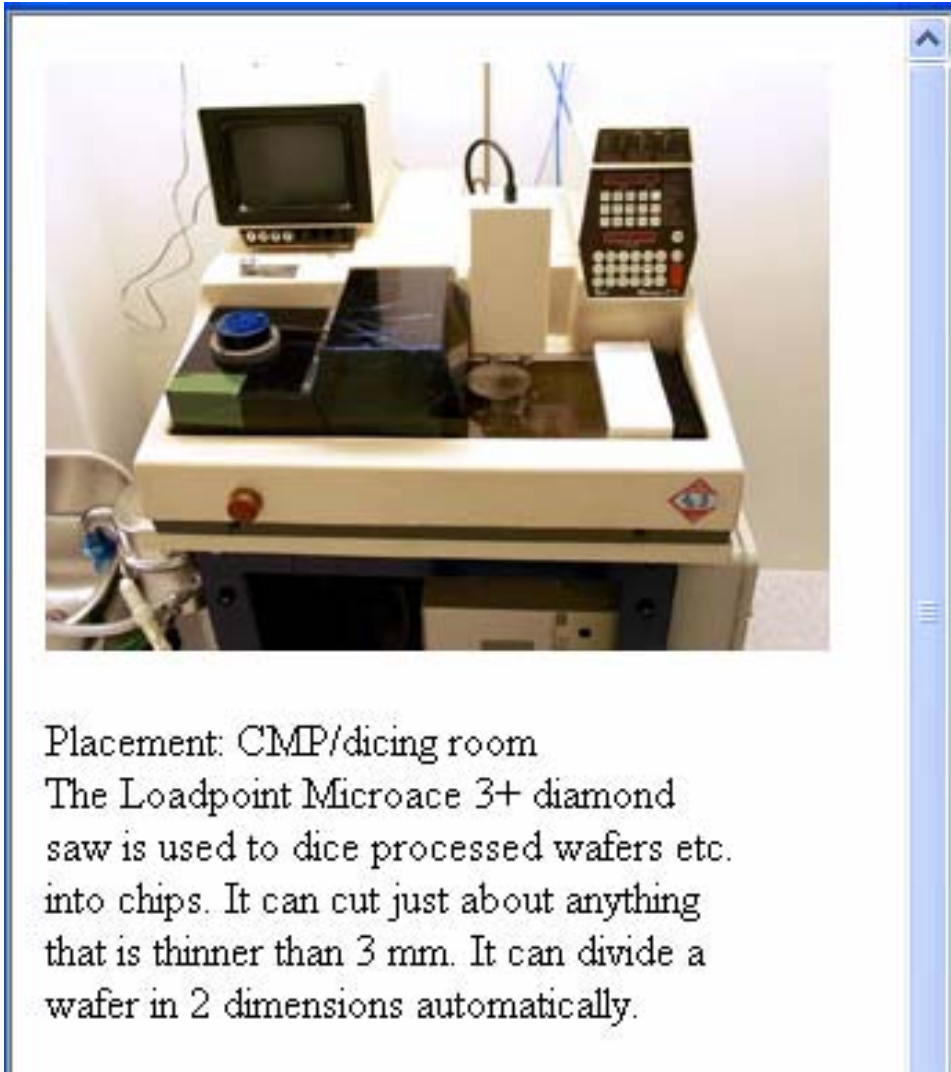
- MOS devices
- Silicon Bipolar technology
- Design and layout considerations
- GaAs and other III-V devices
- **Packaging**
- Reliability

Manufacturing steps related to packaging:

- **Testing**
 - On wafer before dicing
 - More complete test after packaging
- **Wafer thinning**
- **Die separation – Scribe or saw**
- **Die attachment – Epoxy or eutectic**
- **Wire bonding**
 - Ultrasonic or thermal
 - Ball bonding or wedge bonding
- **Flip-chip and solder bump technology**

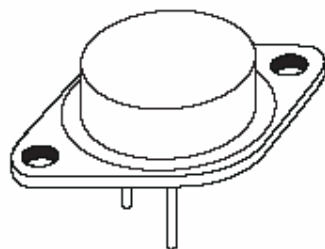


Figure 1. Example of an IC Tester (Left) and Three (3) Examples of Test Handlers (Right)



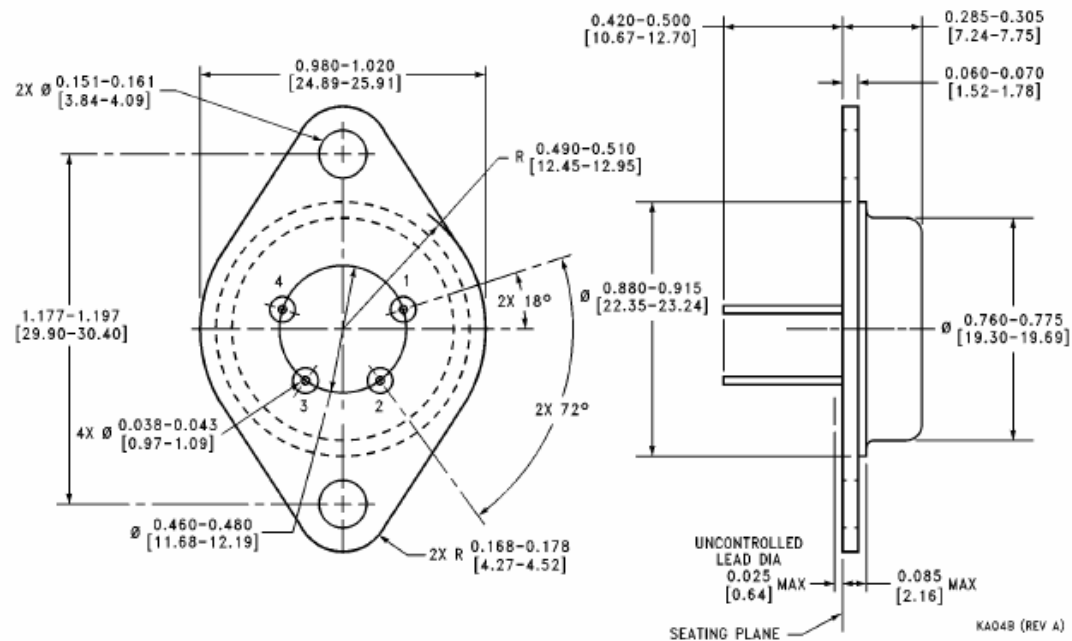


TRANSISTOR
OUTLINE PACKAGE

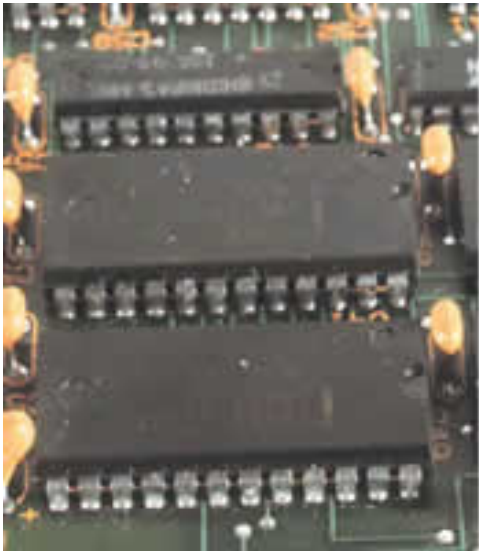
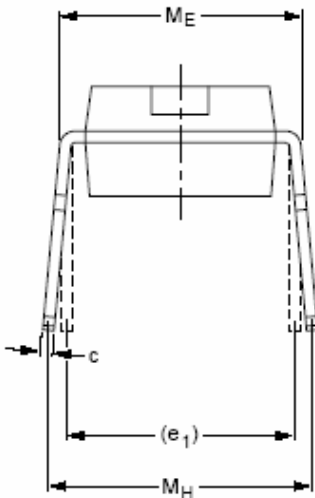
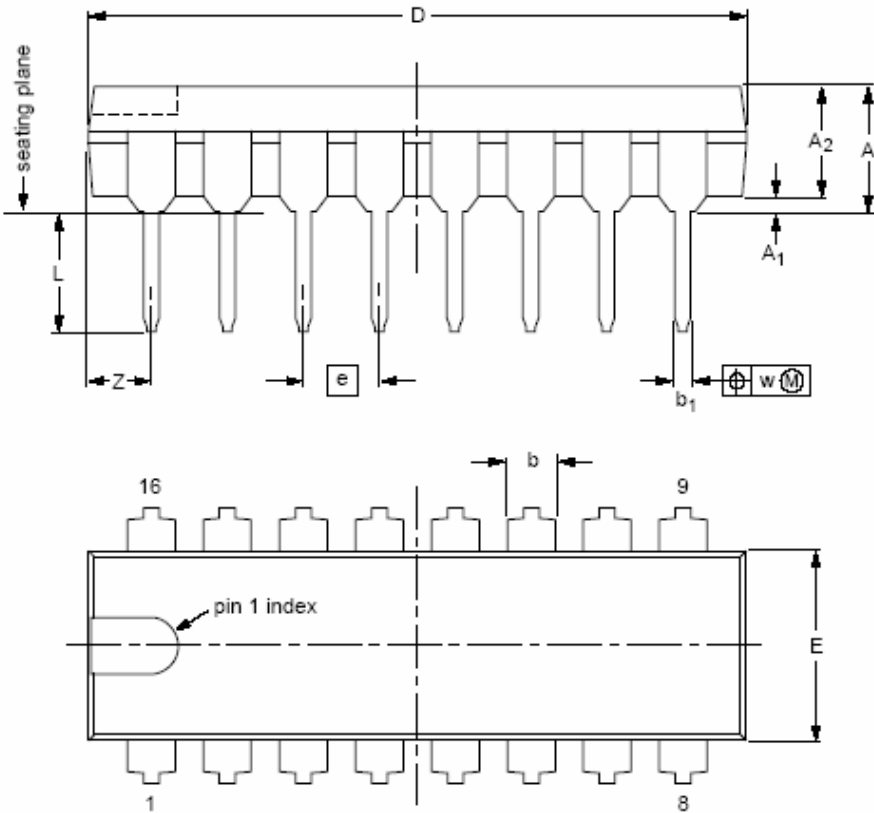


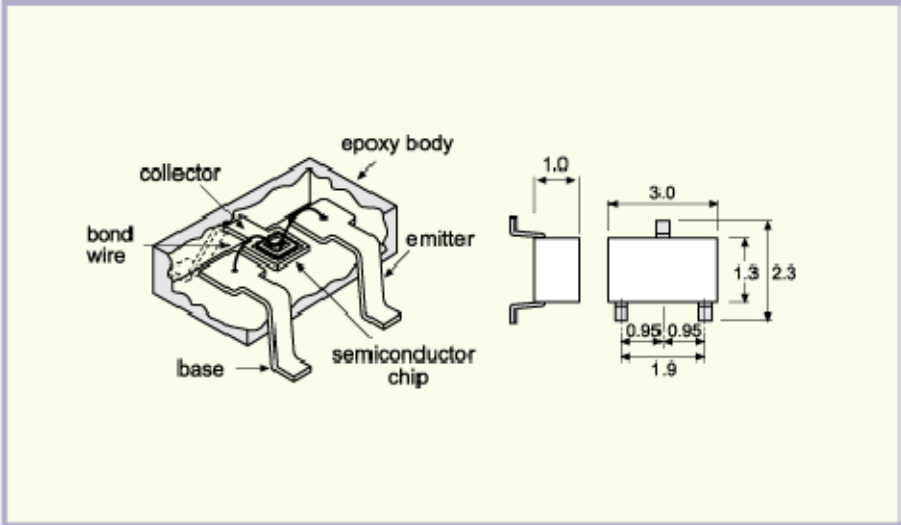
TO-3

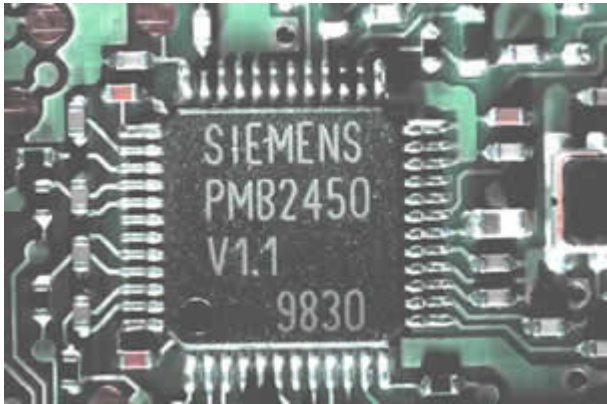
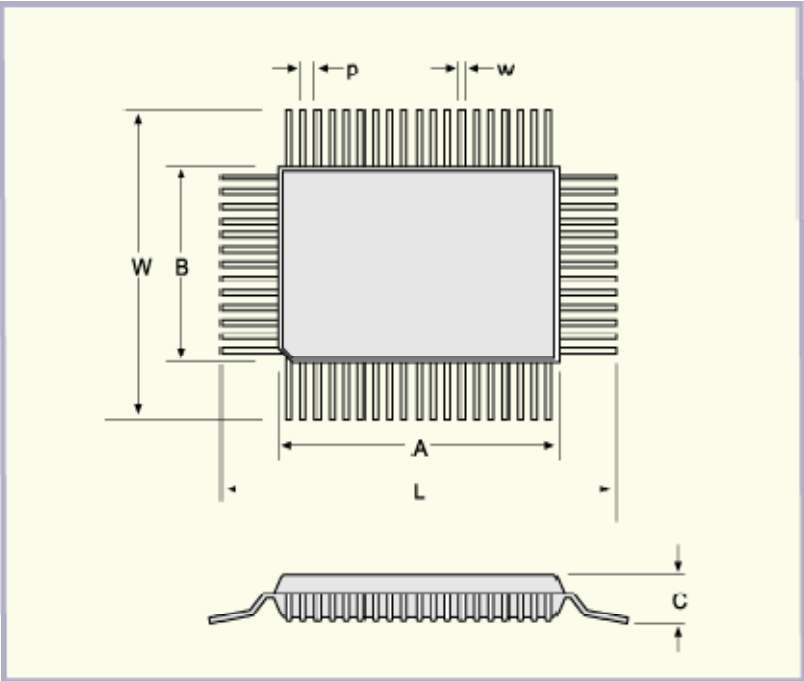
4 Lead TO-3 Metal Can Package, Low Profile
NS Package Number KA04B

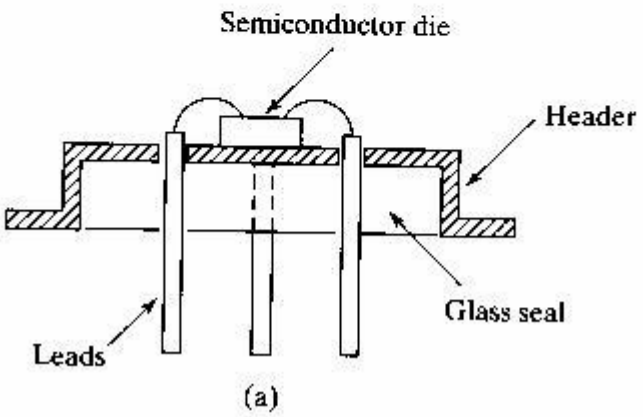
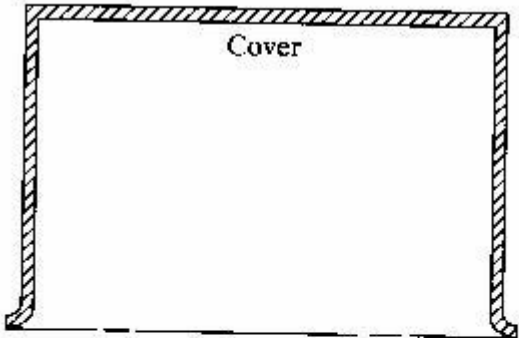
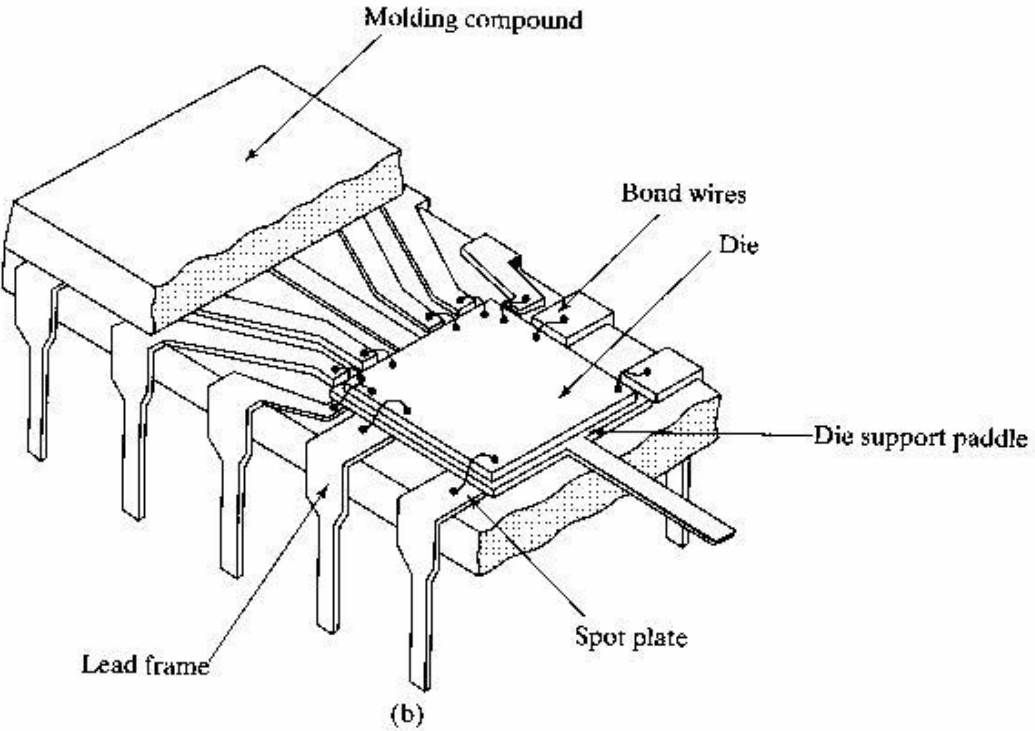


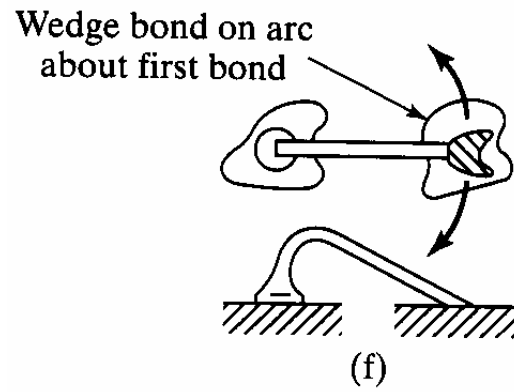
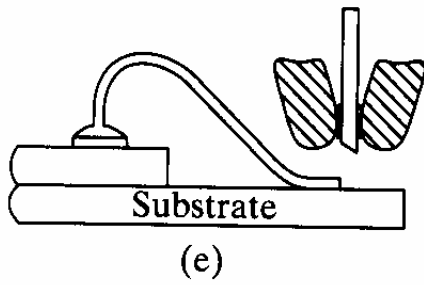
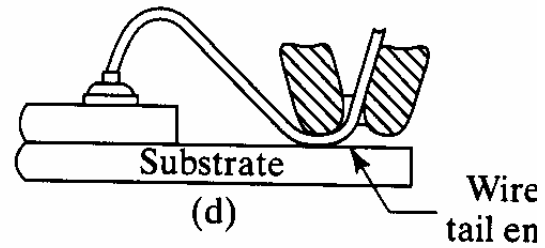
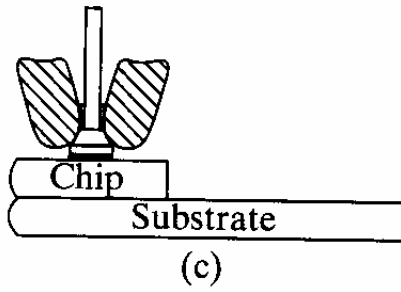
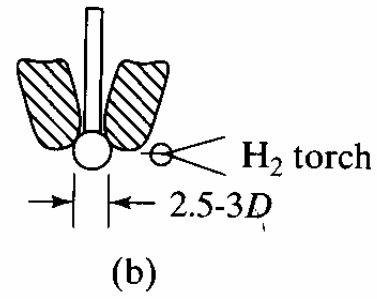
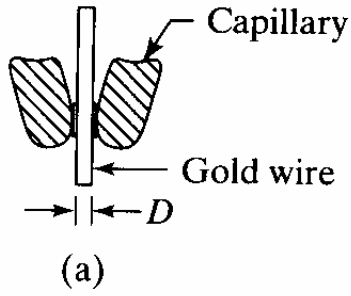
All dimensions are in inches (millimeters)

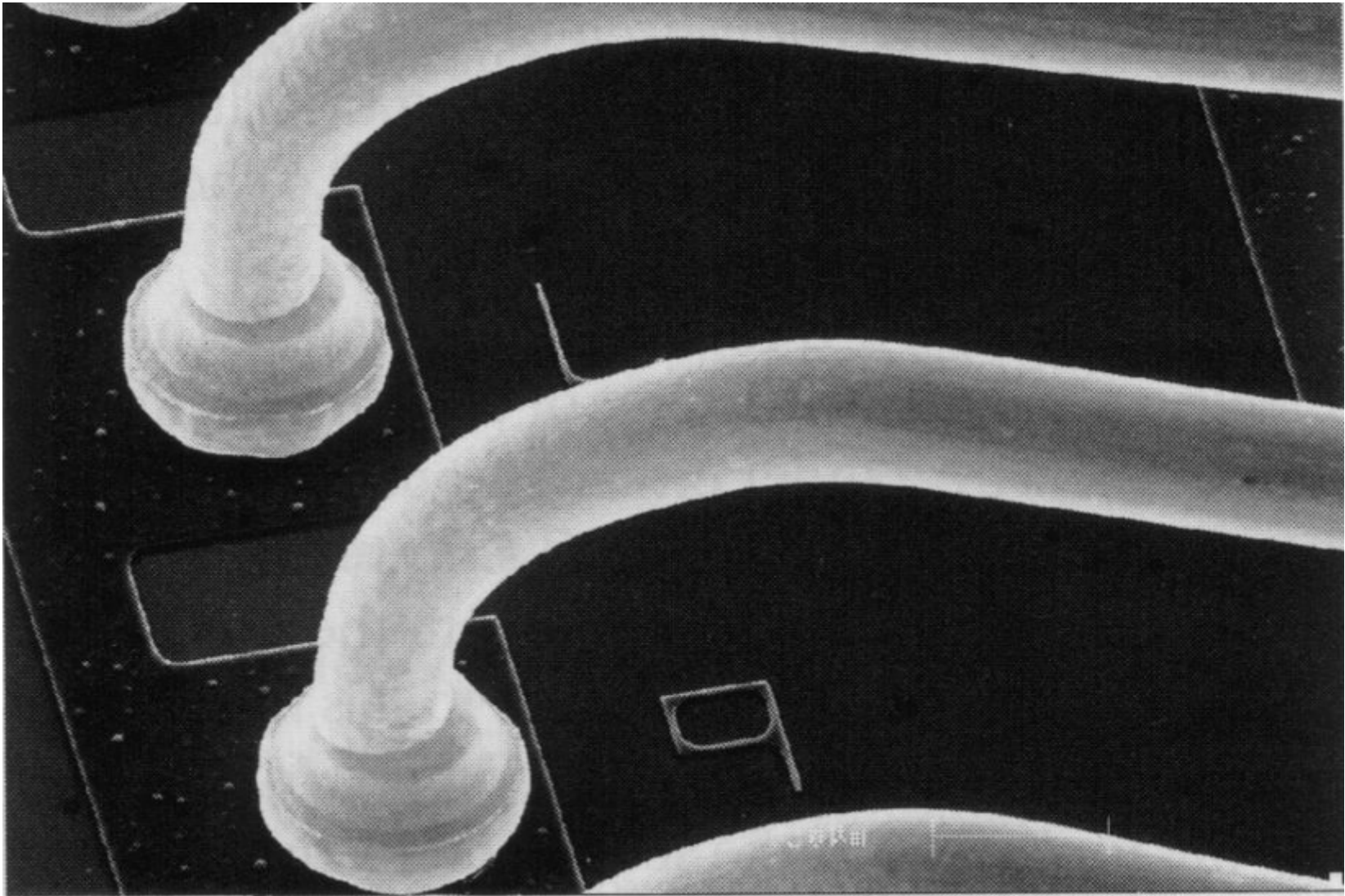


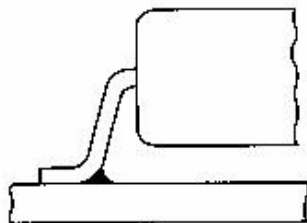




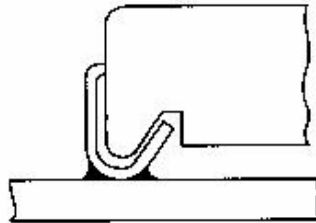








(a)

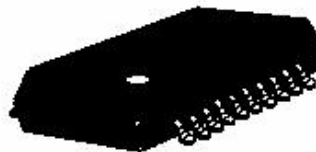


(b)



(c)

Small outline transistor (SOT)



(d)

Small outline integrated circuit (SOIC)



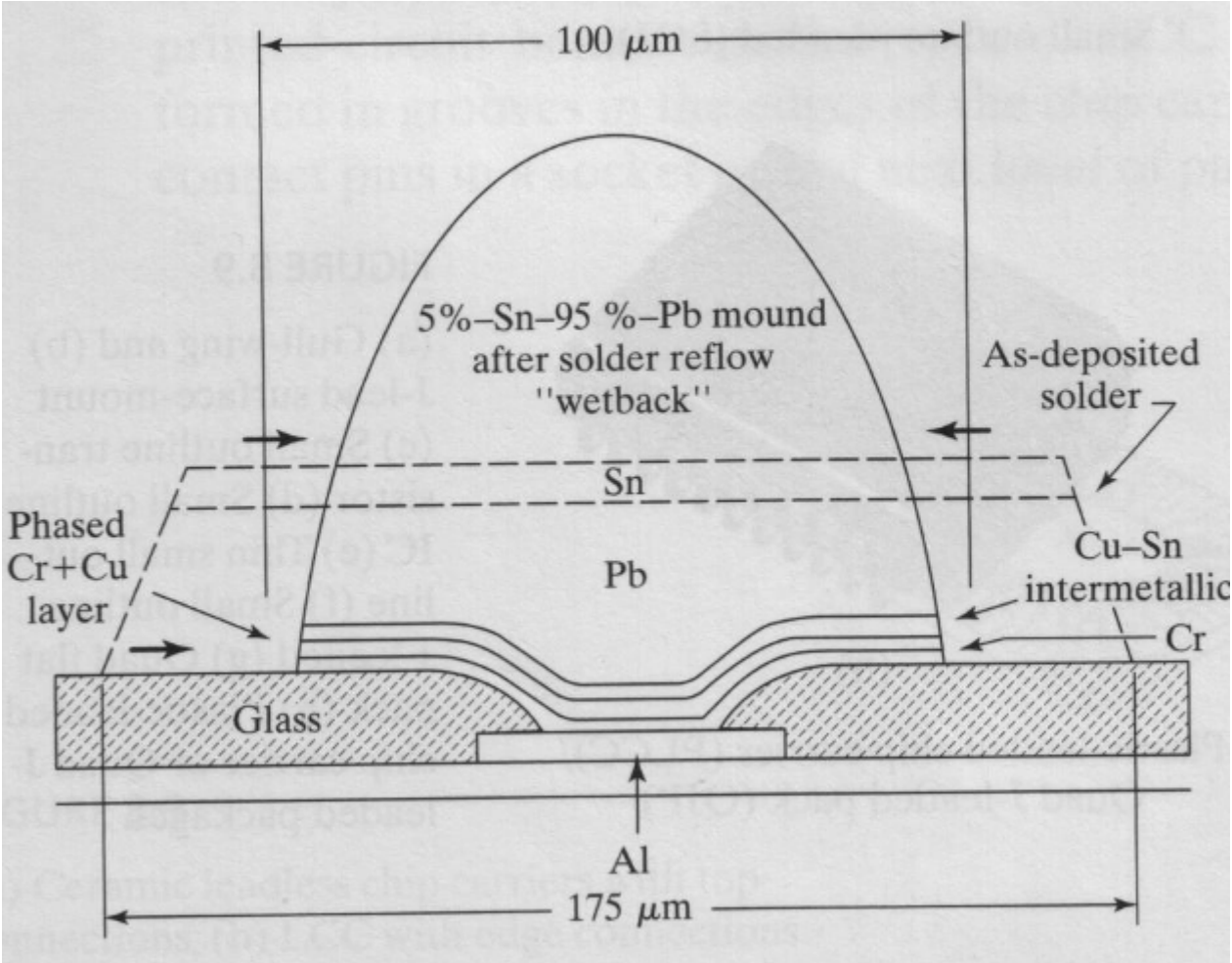
(e)

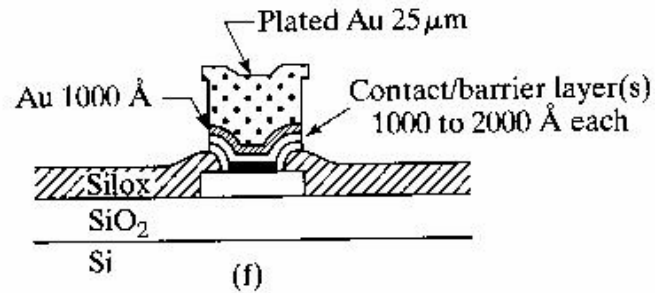
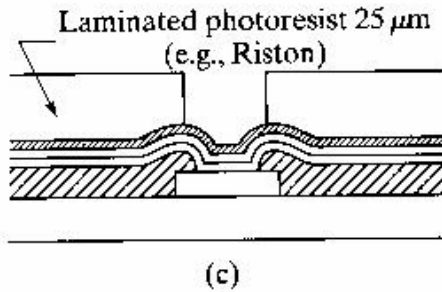
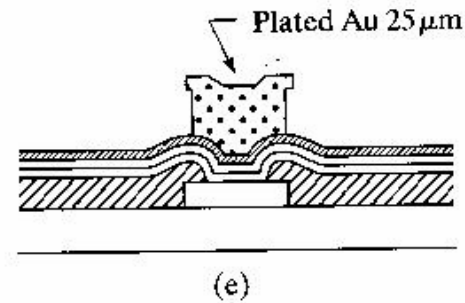
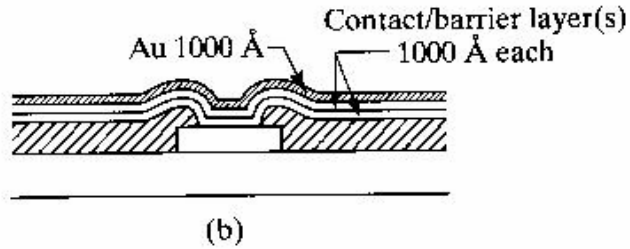
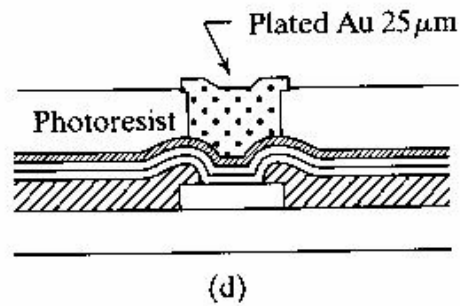
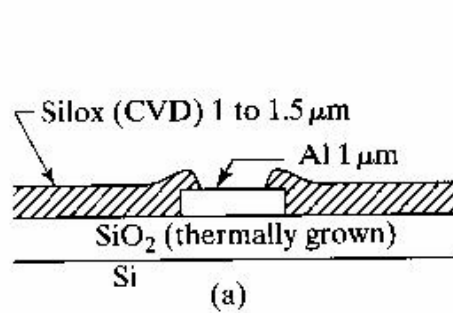
Thin small outline package (TSOP)



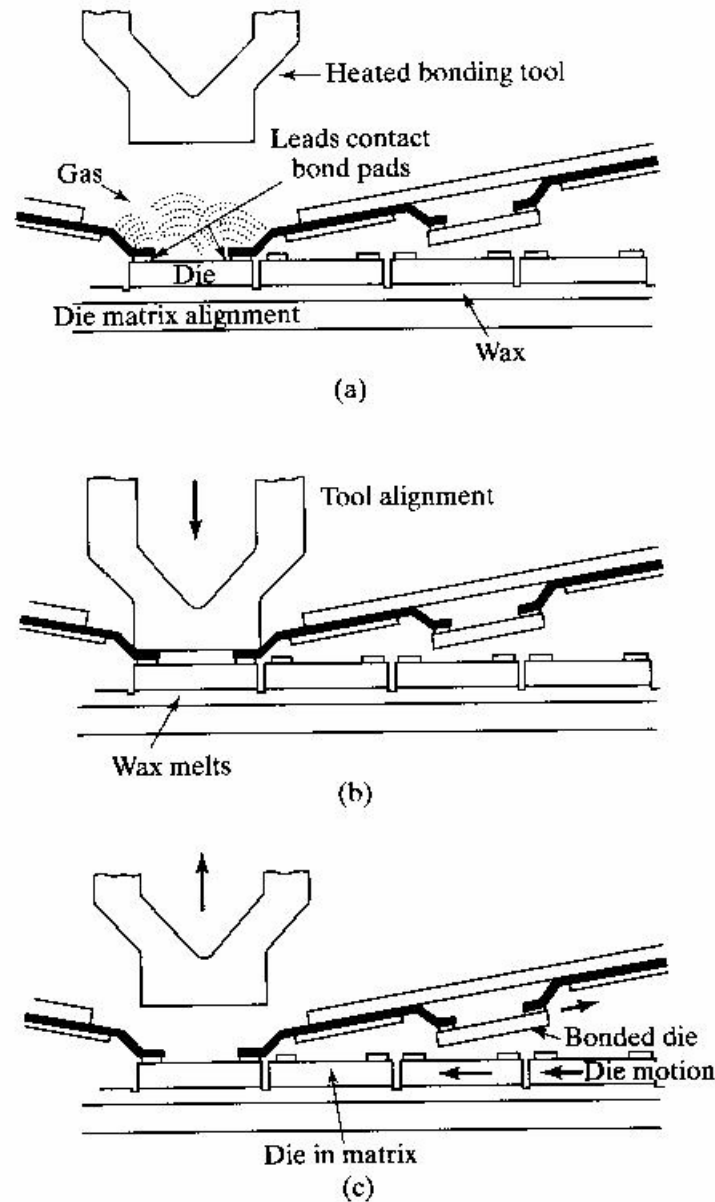
(f)

Small outline j-leaded (SOJ)





TAB = Tape Automated Bonding



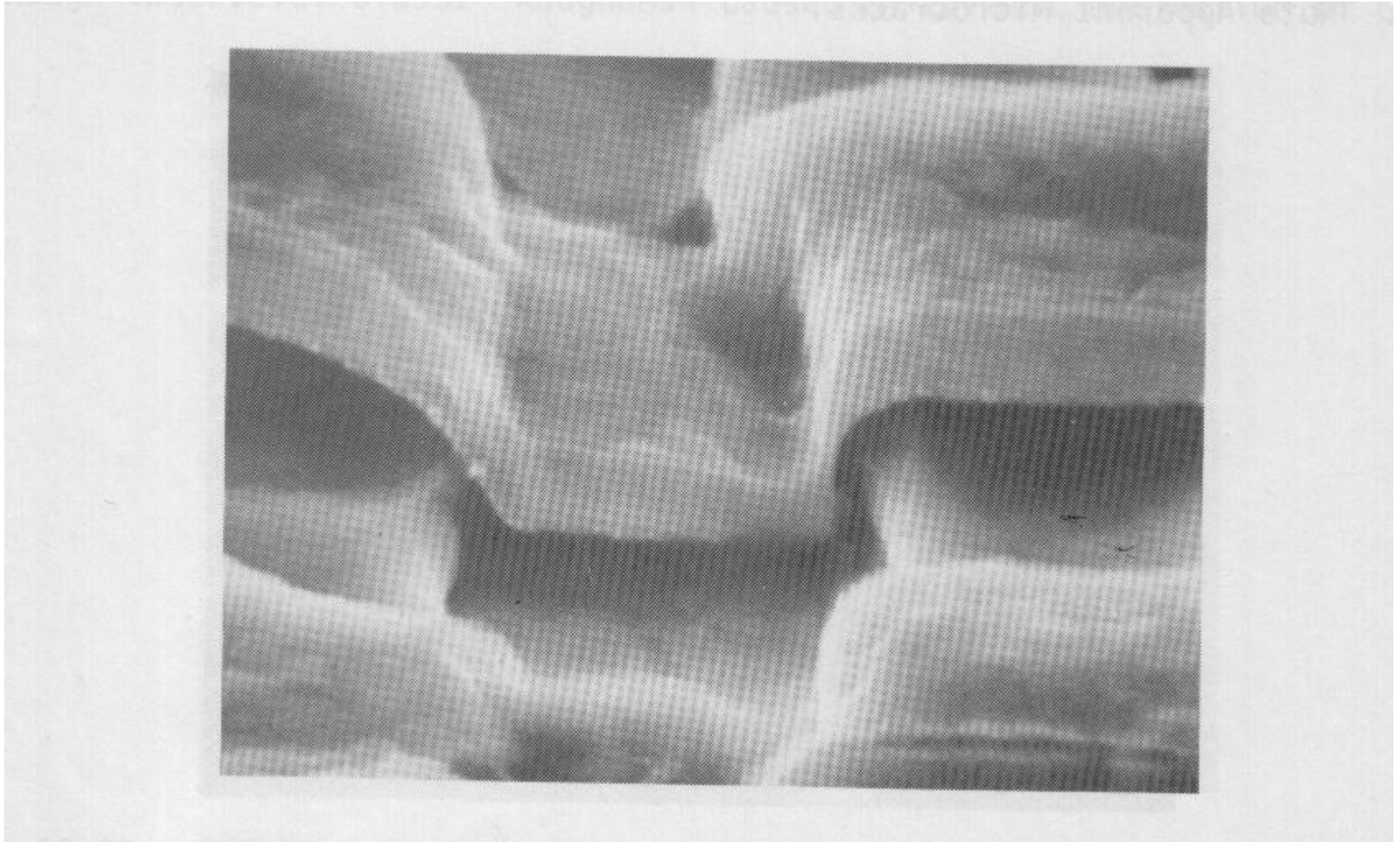
DEVICE TECHNOLOGY & PACKAGING

Göran Alestig

- MOS devices
- Silicon Bipolar technology
- Design and layout considerations
- GaAs and other III-V devices
- Packaging
- **Reliability**

Reliability

- Needs to be "designed in", cannot be added afterwards
- Need to pass tests for:
 - Current density
 - Voltage stress (dielectric breakdown, hot electrons, ...)
 - Step coverage of metal lines
 - Hot/cold temp stress
 - Passivation integrity
 - ESD (electro-static discharge)
 - etc, etc,



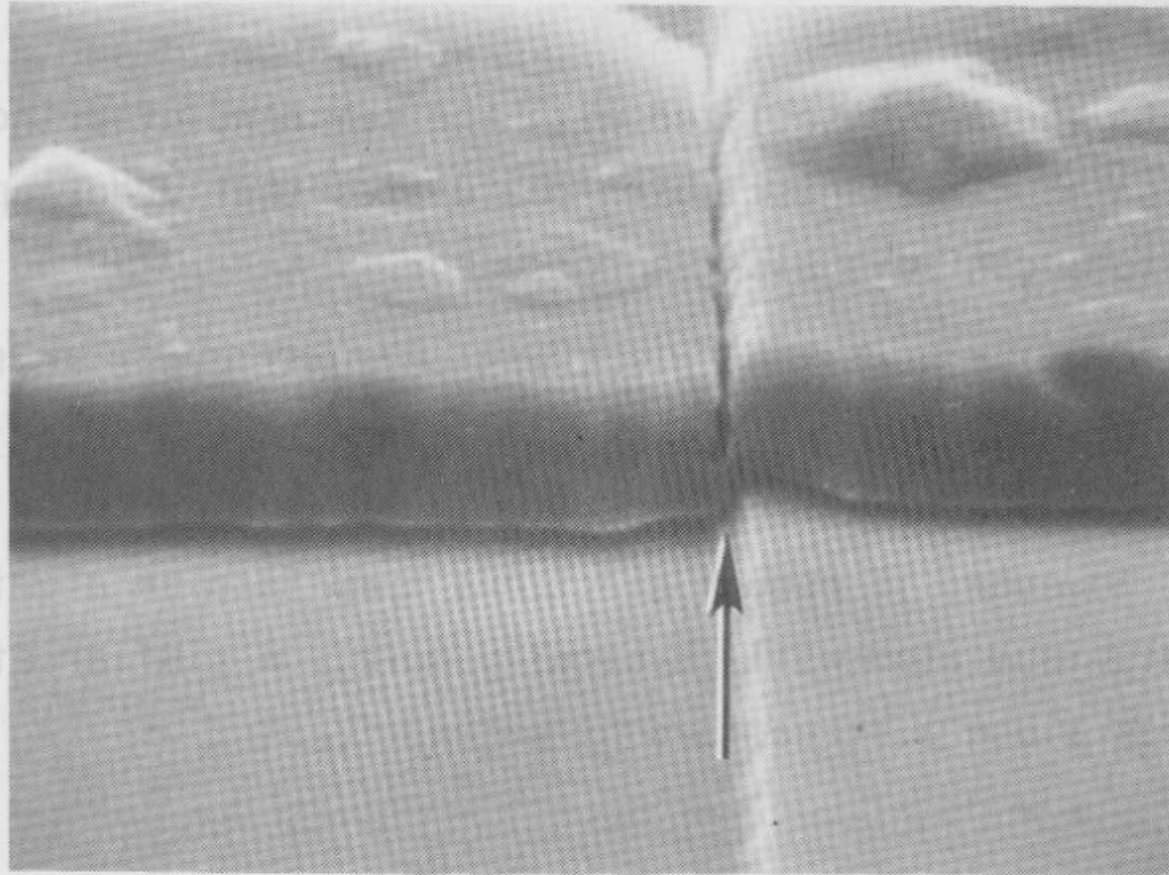
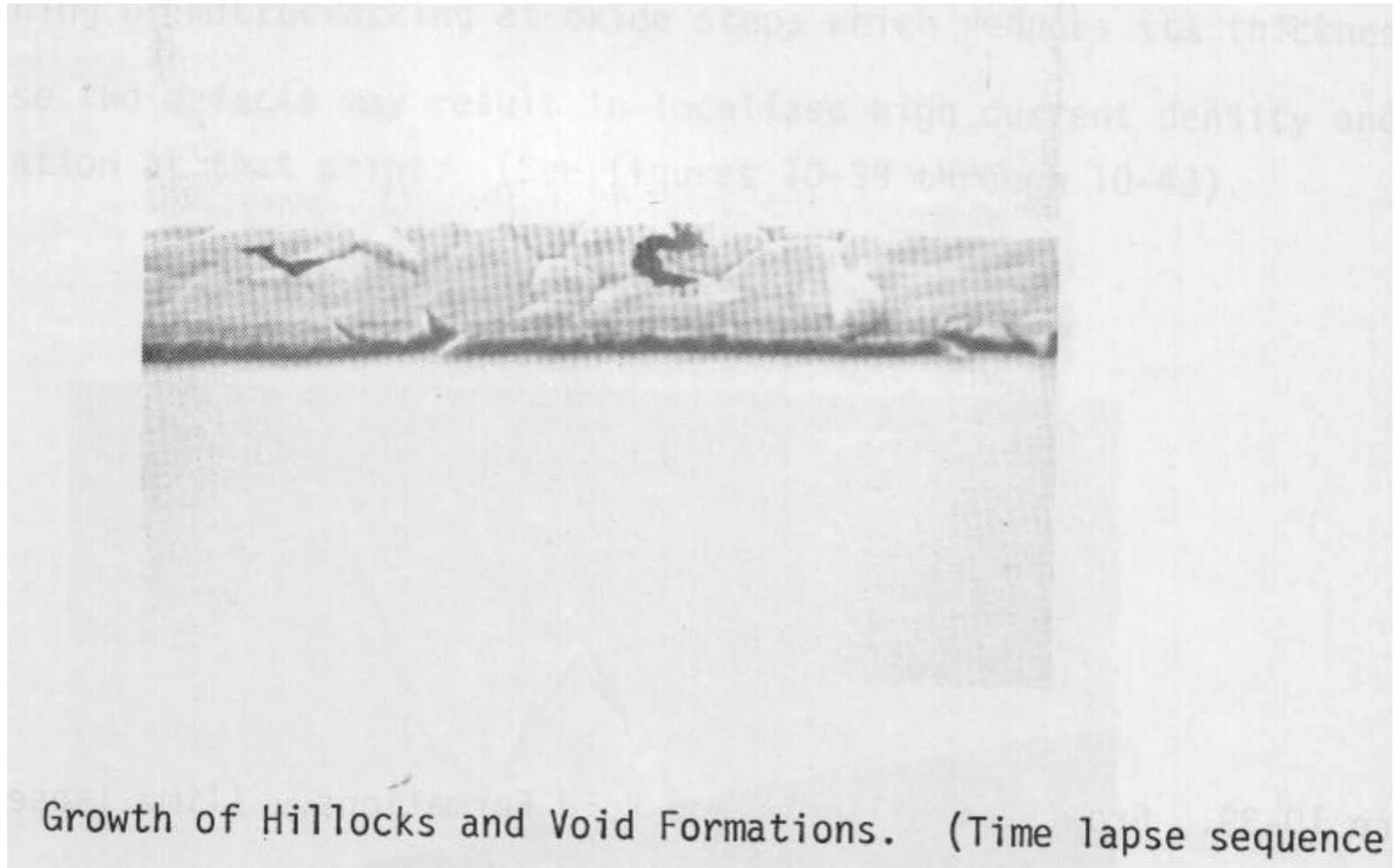
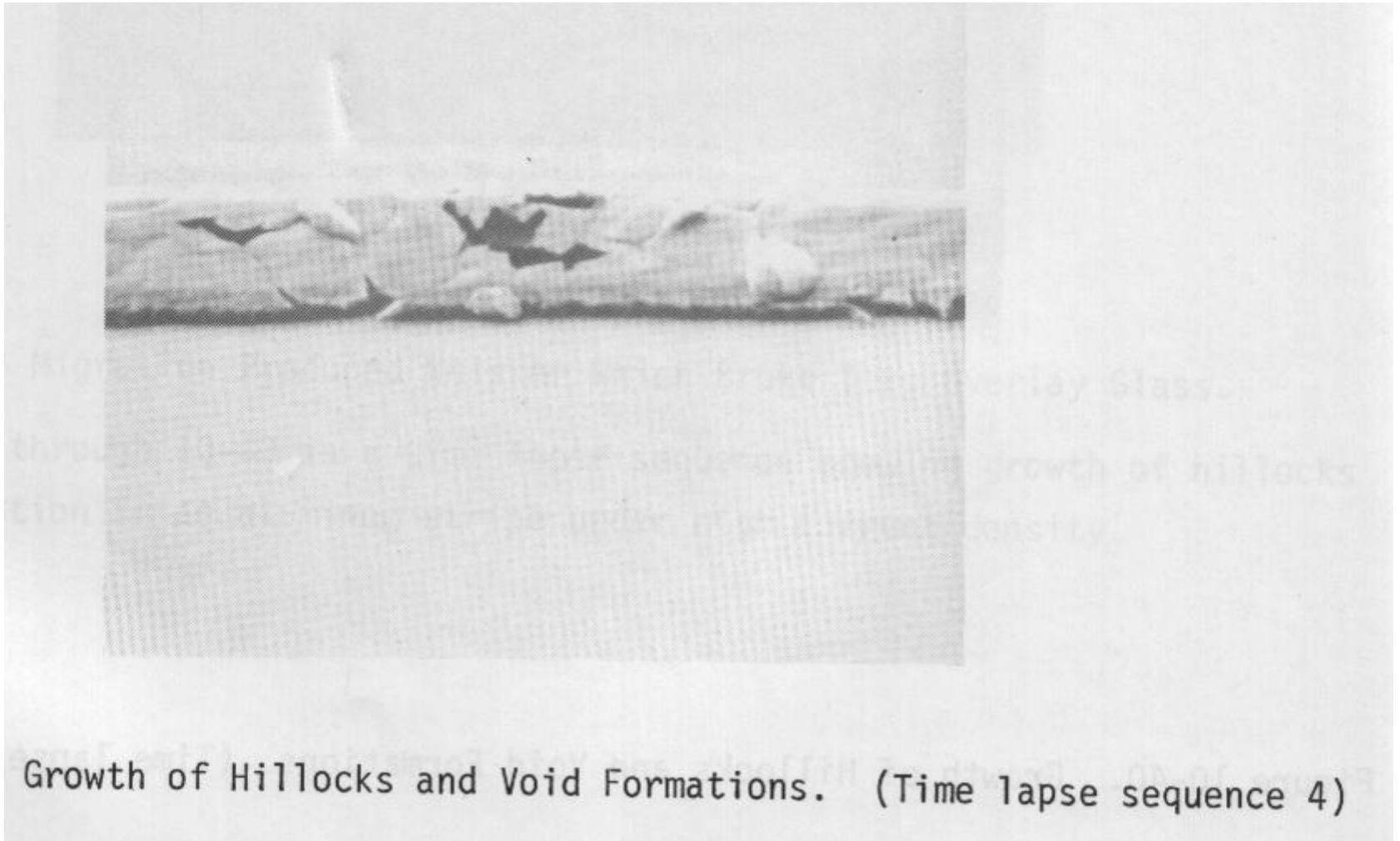
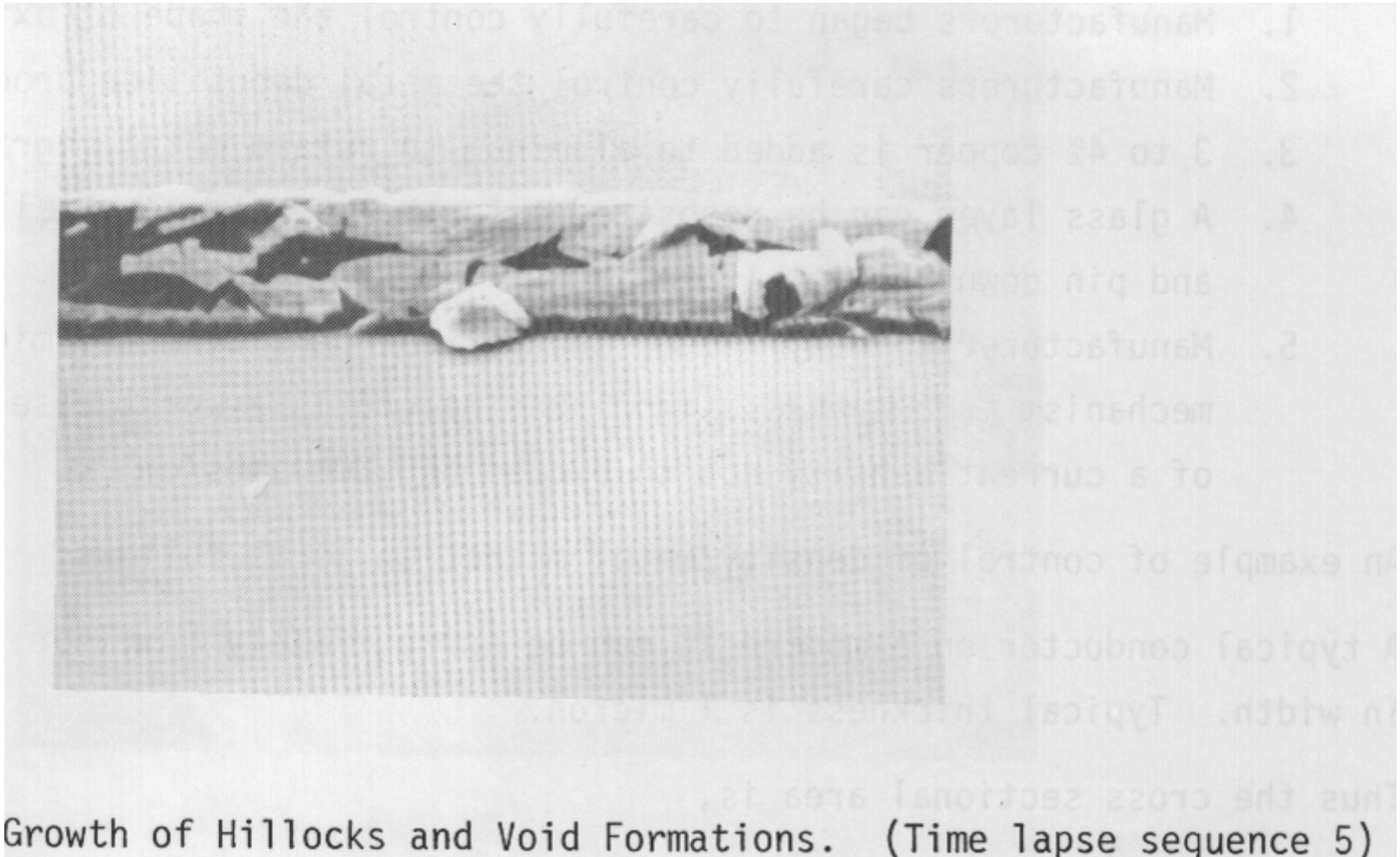


Figure 10-33. Excellent Example of Microcrack Propagation up Thru a Very Thick Metal Layer. Metal is 4 to 5 times as Thick as the Step is High.







Growth of Hillocks and Void Formations. (Time lapse sequence 5)

