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THESIS FOR THE DEGREE OF DOCTOR OF PHILOSOPHY

# Investigation of Future Nanoscaled Semiconductor Heterostructures and CMOS Devices

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Investigation of Future Nanoscaled Semiconductor  
Heterostructures and CMOS Devices

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Ente Daddykkum Mammykkum  
Snehathode

To My Mother and Father  
For Your Love, Care & Prayers

Lead, Kindly Light, amid the encircling gloom,  
Lead thou me on;  
The night is dark, and I am far from home  
Lead thou me on.  
Keep thou my feet; I do not wish to see  
The distant scene; one step enough for me.

-John Henry, Cardinal Newman (1801-90)

# PREFACE

This thesis titled "Investigation of Future Nanoscaled Semiconductor Heterostructures and CMOS Devices" is written towards getting a philosophy doctorate (Ph. D) in Physics. The research for this work was carried out roughly between the period of September 1998 and November 2002. During the first two years of my research period, (September 1998 and September 2000), I was shuffling my time between Chalmers and IVF (Swedish Institute of Production Engineering Research-Mölndal, Göteborg) to work on semiconductors and polymeric electronic packaging, respectively. After September 2000, I spent my time in Chalmers to prepare this eight publications (published, submitted and in manuscript) that are attached along with this thesis. Apart from these publications, I have also contributed to nine other articles. In a nut shell, the studies for this thesis are done in roughly 2 years. During my work in IVF, I have written a few project reports and a project proposal to Albertiska foundation, Gothenburg University, for which a grant was awarded to me. I hope that you will enjoy reading this thesis and it will contribute towards the growing technology, for a better tomorrow.

Ajey P. Jacob

Göteborg, October 28<sup>th</sup> 2002

## Abstract

Miniaturization is the key word in microelectronics. The march towards smaller solid state electronics components has given a lot of interesting results and is now maturing into nanometre regime. This is true for both conventional CMOS technology and new emerging low dimensional structure based devices. This thesis divides its contents among some issues relevant to electrical and optoelectronic devices. The first part of the thesis is devoted to nanoscaled CMOS devices and the second part to the nanoscaled semiconductor structures.

In the first part, we have investigated four different issues related to engineering a better performance of future emerging MOS technology. The first issue deals with the cryogenic operation of ultrathin oxide MOS structures with poly-Si and Poly-Si<sub>1-x</sub>Ge<sub>x</sub> gates. The main characterization tool was current-voltage (I-V) and capacitance voltage (C-V) techniques. Here, the main issue was to investigate the characteristics of flat band voltage at different temperatures and how it depends on various gate structures. We have also investigated the dependence of the accumulation capacitance for poly-Si and poly-Si<sub>1-x</sub>Ge<sub>x</sub> (x=0, 0.2 and 0.35) gates. The second issue was the structural roughness and interfacial strain properties of Si/SiO<sub>2</sub>/poly-Si<sub>1-x</sub>Ge<sub>x</sub> (x=0, 0.2 and 0.35). We have employed Transmission Electron Microscope (TEM) in both image form and convergent beam electron diffraction and High Resolution X-ray Diffraction (HR-XRD) rocking curves (HR-RC) and reciprocal space mapping (2D-RSM). We found that the Ge fraction in the gate material defines the grain size and this in turn determines the strain along the Si/SiO<sub>2</sub> lower interface. This is in fact an interesting result, since the release or introduction of strain at lower interface (conducting channel) determines defects which consequently affect the transport properties of the channel (mobility). The third part in this section deals with qualitative assessment of oxynitridation using ion implantation as nitrogen source in a poly-Si<sub>1-x</sub>Ge<sub>x</sub> gate. A time temperature study was undertaken to determine the process of nitrogen diffusion in to the silicon dioxide region. The oxynitridation takes place in the interface or in the SiO<sub>2</sub> region. It was found that a uniform nitrogen distribution takes place at a proper thermal processing. Finally, the overgrowth of tensile strain Si<sub>1-x</sub>Ge<sub>x</sub> on fully relaxed Ge/Si (001) in uninterrupted growth sequence was investigated using HR-XRD.

In the second section of the thesis, passivation and thermal processing of nanoscaled semiconductor structures is discussed. The first paper in this section shows that hydrogen can passivate dopants in a delta doped CdZn<sub>1-x</sub>Te<sub>x</sub> quantum well structures. The next paper investigates passivation of non-radiative centres like defects (dislocations) in an InAs quantum dot structure. It is shown that defect passivation can increase the radiative centres and this in turn can increase the luminescence efficiency of InAs quantum dots. The third paper gives a systematic study on the effect of thermal processing on ZnSe<sub>1-x</sub>Te<sub>x</sub> (x<0.01%) epilayers. It is shown that ZnSe<sub>1-x</sub>Te<sub>x</sub> epilayer under proper post growth thermal annealing can give room temperature emission at a wavelength range in the visible region of 5500-7000 Å. Hydrogen passivation study done on these samples confirms the previous reports that the broad band emission is related to isoelectronic defect, i.e., excitons bound to the Te clusters. For all the above papers, we have employed photoluminescence (PL) and high resolution X-ray diffraction (HR-XRD) technique for investigation. In the last paper, we have investigated CdZnTe quantum wells for their thermal stability and HR-XRD was used for their investigation.

## Abbreviation

ULSI	Ultra Large Scale Integration
CMOS	Complimentary Metal Oxide Semiconductor (Silicon)
MOSFET	Metal Oxide Semiconductor (Silicon) Field Effect Transistor
MBE	Molecular Beam Epitaxy
CVD	Chemical Vapour Deposition
RTP	Rapid Thermal Processing
RTO	Rapid Thermal Oxidation
I-V	Current Voltage
C-V	Capacitance Voltage
PL	Photoluminescence
PLE	Photoluminescence Excitation
FE	Free Exciton
FB Transition	Free-to-Bound Transition
DAP Transition	Donor-Acceptor Pair Transition
XRD	X-ray Diffraction
TEM	Transmission Electron Microscope
SIMS	Secondary Ion Mass Spectrometry

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## APPENDED PAPERS

This thesis is based on the work contained in the following papers:

1. A. P. Jacob, T. Myrberg, O. Nur, M. Willander, P. Lundgren, E. Ö. Sveinbjörnsson, L. L. Ye, A. Thölen and M. Caymax “Cryogenic performance of ultrathin oxide MOS capacitors with in situ doped  $p^+$  poly-Si<sub>1-x</sub>Ge<sub>x</sub> and poly-Si gate materials” in *Semiconductor Science and Technology* **17**, 942 (2002).
2. L. L. Ye, A. P. Jacob, T. Myrberg, O. Nur, M. Willander and A. Thölen, “Structural roughness and interface strain properties in Si/SiO<sub>2</sub>/poly-Si<sub>1-x</sub>Ge<sub>x</sub> tri-layer system with ultra thin oxide. (Submitted to *Journal of Material Science: Materials in Electronics*).
3. A. P. Jacob, T. Myrberg, O. Nur, M. Friesel, M. Willander, U. Serincan, and R. Turan, “Ultrathin Oxynitridation Process through ion implantation in a Poly-Si<sub>1-x</sub>Ge<sub>x</sub> Gate MOS capacitor” (Submitted to *Journal of Material Science in Material Processing*).
4. A. P. Jacob, T. Myrberg, O. Nur, M. Willander, C. J. Patel, Y. Campidelli, C. Hernandez, O. Kermarrec, D. Bensahel and R. N. Kyutt, “Relaxation properties of Si<sub>1-x</sub>Ge<sub>x</sub> uninterrupted over growth on fully relaxed Ge/Si 001” (Manuscript).
5. A. P. Jacob, Q. X. Zhao, M. Willander, T. Baron and N. Magnea, “Hydrogen passivation of nitrogen-acceptors confined in CdZnTe quantum well structures” in *Journal of Applied Physics*, **90**, 2329 (2001).
6. A. P. Jacob, Q. X. Zhao, M. Willander, F. Ferdos, M. Sadeghi and S. M. Wang, “Hydrogen passivation of self assembled InAs Quantum dots” in *Journal of Applied Physics* **92**, No. 11 (2002).
7. A. P. Jacob, Q. X. Zhao and M. Willander, “Room temperature luminescence from ZnSe<sub>1-x</sub>Te<sub>x</sub> ( $x < 1\%$ ) epilayers grown on (001) GaAs” (Submitted to *Journal of Applied Physics*).
8. A. P. Jacob, T. Myrberg, O. Nur, M. Willander and R. N. Kyutt, “Post-growth process relaxation properties and interlayer diffusion of strained Cd<sub>0.92</sub>Zn<sub>0.08</sub>Te/ Cd<sub>0.83</sub>Zn<sub>0.17</sub>Te quantum well heterostructure grown by molecular beam epitaxy” (submitted to *Journal of Vacuum Science and Technology-B*).



In addition, the following papers have been published, (submitted for publications, or as manuscripts) but are not included in the thesis. Their content either strongly overlaps with the papers above or is outside the scope of this thesis.

9. A. P. Jacob, T. Myrberg, O. Nur, G. Aygun, R. Turan, M. Willander, "Bias dependence and post metallization annealing of interfacial states in ultrathin oxide p<sup>+</sup> poly-Si (Si<sub>1-x</sub>Ge<sub>x</sub>) gated MOS structures" (Tentative Manuscript).
10. A. P. Jacob, Q. X. Zhao and M. Willander, "Thermal annealing of self assembled Ge quantum dots grown by MBE and CVD" (Manuscript).
11. A. P. Jacob, T. Myrberg, M. Friesel, O. Nur, M. Willander, U. Serincan, R. Turan, "Nitridation of ultrathin oxide MOS poly-Si<sub>1-x</sub>Ge<sub>x</sub> capacitor through ion implantation" in Challenges in Predictive Process Simulation (ChiPPS-2002), Prague, Czech Republic, 13-17 Oct 2002.
12. A. P. Jacob, Q. X. Zhao, T. Myrberg and M. Willander, "Post growth processing of quantum dots in hydrogen atmosphere" Poster presentation and Gunshot oral presentation in the "Frontiers in Nano-Science and Nanotechnology" Værløse, Denmark, June 18 - 23, 2002.
13. A. P. Jacob, T. Myrberg, M. Y. A. Yousif, O. Nur, M. Willander, P. Lundgren and E. Ö. Sveinbjörnsson, "Low temperature electrical performance of ultrathin oxide MOS capacitors with p<sup>+</sup> poly-Si<sub>1-x</sub>Ge<sub>x</sub> and poly-Si gate materials" in IWPSD, Delhi, India, December 2001.
14. A. P. Jacob, T. Myrberg, O. Nur, Q. X. Zhao, M. Willander, T. Baron and N. Magnea, "Post-Growth structural stability and optical properties of strained CdZnTe single quantum well grown by MBE" in IWPSD, Delhi, India – December 2001.
15. Q. X. Zhao, A. P. Jacob, M. Willander, F. Ferdos, M. Sadeghi and S. M. Wang, "Nonradiative centres in InAs dots grown on GaAs substrates for 1.3 μm emission"(Submitted to, Physical Review B).
16. T. Myrberg, A. P. Jacob, O. Nur, M. Friesel, M. Willander, C. J. Patel, Y. Campidelli and D. Bensahel, "Effect of layer thickness on the structural properties of relaxed Ge buffer layers on Si (001) in Challenges in Predictive Process Simulation (ChiPPS-2002), Prague, Czech Republic, 13-17 Oct 2002.
17. M. Willander, Q. X. Zhao, A. P. Jacob, "Optical Properties of low dimensional semiconductor structures" in XXXI International school on the physics of semiconducting compounds Jaszowiec 2002, Poland, June (2002) (Invited talk).

18. T. Myrberg, A. P. Jacob, O. Nur, Q. X. Zhao, M. Willander and W. B. DeBoer, "Relaxation and Photoluminescence of different post-processed Si/Si<sub>1-x</sub>Ge<sub>x</sub> quantum well structures grown by CVD" in Solid-State Electronics, **45**, 1915 (2001).
19. A. P. Jacob, J. Liu, M. Willander, Quality assessment of conductive adhesives bonded Electronic Packaging, -Project Proposal submitted to Albertiska foundation in Göteborg University, Göteborg for fundamental research in "environmentally compatible electronics" (July, 1999).

Science knows no country, because knowledge belongs to humanity, and is the torch which illuminates the world.

Pasteur, Louis  
(1822-1892) b. Dôle, France

René Dubos, *Pasteur and Modern Science*, Doubleday, Garden City, NY, 1960, p. 145. (1)

# 1

## General Introduction

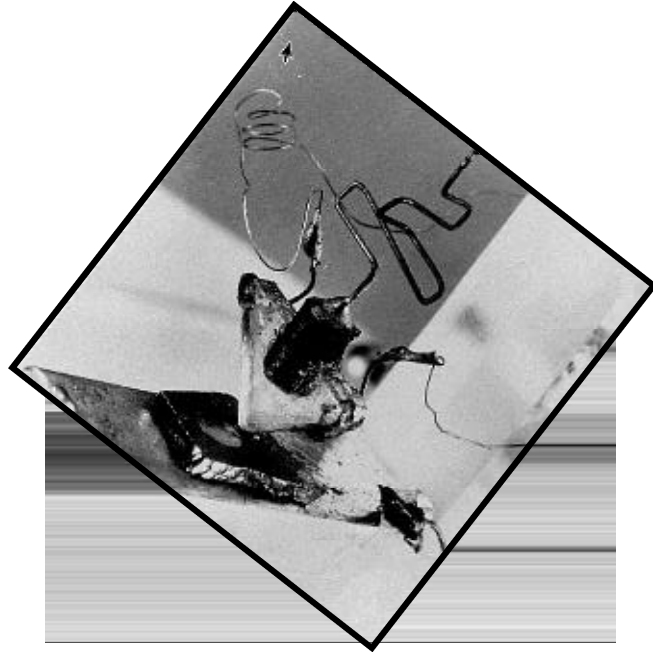
The communication revolution and the present information age date back some 500 years, when the first printing press originated. Today, we can store and rapidly move enormous amounts of information across the globe through computers (via internet). What happens when you switch on the computer? We find that the operating system; UNIX, Linux, DOS or MAC; of the computer pops up with in few seconds. So what transpires in the computer during these few seconds? During this little time, we find that the system is checking for various components like key board, mouse, various hard disks etc. For a computer to do all these jobs, we need to configure the system. The information to configure the system as and when you switch it on is stored in “memory” made of CMOS devices. CMOS stands for Complimentary Metal Oxide Semiconductor.

The credit for today’s technological progress goes to semiconductors. It is obvious from the name itself that a semiconductor has its conducting characteristics between a conductor and an insulator. The history of semiconductors can be traced back to early nineteenth century when *Michael Faraday* observed decrease in resistance of silver sulphide with increasing temperature (1833). In 1873, *W. Smith* found out the photo-conducting property of selenium. *F. Braun* is credited for observing the rectifying property of lead sulphide in 1874.

The present day communication revolution started with an entirely new research field that was brought in by *Sir J. C. Bose* for his "millimeter wave propagation measurements through certain polarizing crystals" in 1895. This led to the discovery of solid-state diode detector of wireless waves for which *Bose* was given the world's first patent. During the Second World War, silicon found its application as a rectifier in radar systems. Silicon is an element produced from silica. Silica (sand) is one of the most abundantly available materials in the earth, actually the second most abundant material on earth after oxygen. Silicon has been an incredible material for the mankind since its existence. Human civilization has exploited silicon in one form or other; for example, sand and clay are key components for making bricks, sand is the raw material in making glass, sand is used in making steel harder

since centuries and today the multi billion information industries is guided mainly by the same sand.

The intensive development in this industry started since December 16, 1947 when the Nobel laureates *J. Bardeen* and *W. H. Brattain* invented the junction transistor (*Figure 1.1*). On January 23, 1948, Nobel laureate *Shockley* made the revolutionary theoretical invention for this transistor. Keep in mind that this transistor was made of germanium, a much explored material in those days. In the pursuit of development, germanium had to give way for silicon not because of its superior quality but for its formation of oxide on silicon. Unlike any other semiconductor material, silicon forms



**Fig. 1.1:** Worlds First Solid State Transistor

superior interface with its oxide. This oxide, generally known as silicon dioxide is a dielectric. Thus the credit should go to silicon dioxide. In fact it was the search for field effect mechanism that paved the path to the finding of a transistor with bipolar action. The concept of field effect was that an electric field applied through the surface of a semiconductor could modify the density of mobile charge in the body of the material and thereby change its conductivity. By 1960, *John Atalla* from Bell Labs made new design on the basis of the original field effect theories developed by Shockley paving way to industrial production of field effect transistors by late 1960's. MOSFET (Metal Oxide Semiconductor Field Effect Transistor) is the most used transistors today. CMOS and Bi-CMOS (Complimentary MOS-Bipolar Transistor system) transistors follow the suit in the later developing face.

The invention of the transistor led to quick commercialization efforts, fuelling ever-increasing demands for better and increasingly complex circuits and systems. Integration of transistors, resistors and capacitors on to a single chip leaped the growth of this technology and *Jack Kilby* from Texas Instruments was leading this work. Another name to be mentioned for the integrated circuits is *Robert Noyce* from Fairchild industries. The major invention during this period was the epitaxial growth technique by which one can grow single crystal layer of a material on another crystalline material. *Zhores I. Alferov* of Ioffe Physico-Technical Institute in St-Petersburg and *Herbert Kroemer* of University of California at Santa Barbara used the epitaxial growth technique to grow semiconductor heterostructures used in high-speed and opto-electronic devices. In the year 2000, *Jack Kilby*, *Zhores I. Alferov* and

*Herbert Kroemer* were awarded Nobel Prize for their great contribution to physics and Technology.

The epitaxial growth technique not only revolutionised the semiconductor world, but particular development in fundamental physics could be highlighted. For example, *Esaki* and *Tsu* discovered the low dimensional semiconductor structures with the name semiconductor superlattices in 1969 and they proposed to create artificial potential in a semiconductor crystal using periodically doped layers in 1970. Basically, they observed that an electron moving through the potential of a quantum well (One dimensional periodic lattice structure whose geometrical thickness is less than that of the electron mean free path) exhibits quantum phenomena. Subsequent experimental observations of these predictions (for e.g. negative resistance by *Chang* in 1974 and exciton resonance by *Dingle* in 1975) gave a booming impact on the production and design of semiconductor multilayers with desirable electrical and optical properties. Quantum wires and quantum dots (one and zero dimensional quantum system) are the latest among the low dimensional quantum technologies which have opened new research areas in fundamental science resulting in advanced devices with high resolution and precise performance.

In a nutshell, the semiconductor research has developed in to the field of microelectronics that has leaped multiples of times, thus contributing to all walks of life. One point to be noted here is that this is one of the few research fields where industries and fundamental scientific research goes hand in hand.

This thesis deals with various aspects of this technological innovation with respect to giving a physical understanding on various designs and materials used. The first chapter in this thesis gives a fundamental understanding towards *CMOS devices*. The second chapter is focussed towards *low dimensional heterostructures* and some of the *relevant post processing issues*. Subsequently, the main *characterization tools and the technology* used for various experiments in this thesis are explained. The last chapter gives a *brief conclusion* along with a *short summery about the published scientific articles*. Finally the scientific articles are added along this thesis.

## General Reference

- Proceedings of the IEEE January 1998 Volume 86, No 1, Special Issue on the Fiftieth Anniversary of the Transistor, Edited by P. B. Bondyopadhyay, P. K. Chatterjee and U. Chakrabarti.
- <http://www.nobel.se>
- Figure 1.1- Photo of worlds first point contact transistor, S. M. Sze, Physics of Semiconductor devices, Second edition, Wiley International, New York (1981).

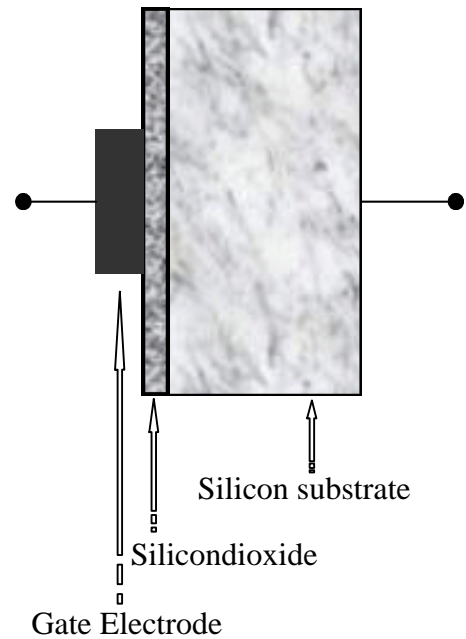
"Computers in the future may weigh no more than 1.5 tons."

- *Popular Mechanics*, 1949

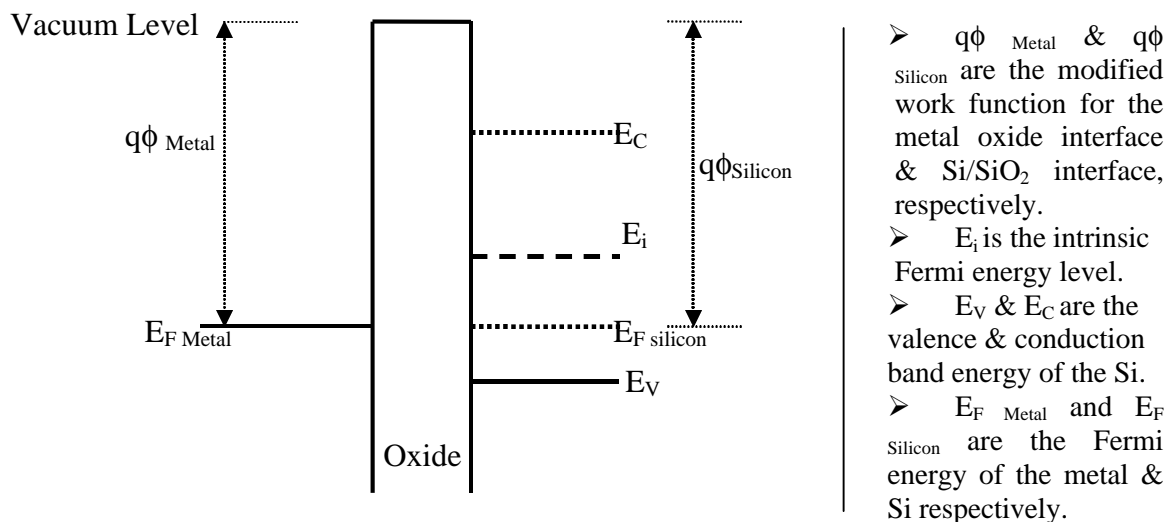
# Future Nanoscaled CMOS Devices

The fundamental building block of a CMOS device or a MOSFET is the Metal Oxide Silicon capacitor configuration and this is as shown in figure 2.1 (a). This parallel plate capacitor configuration is the most demanding test structure for a MOSFET and is called so because the first successful MOS transistor was made of a metal gate, silicon dioxide insulator and silicon. Even today the basic configuration remains the same [Figure 2.1.a]. It is this capacitor that controls the conducting channel region on the silicon surface. The equilibrium energy band diagram for an ideal MOS is given in Figure 2.1.b.

**Fig. 2.1 a**



**Figure 2.1 b**



**Fig. 2.1.a-b:** Schematic picture and the energy band diagram of an MOS system, respectively.



When no bias voltage is applied and when the work function of the metal and Si is equal, an ideal device will align its Fermi levels as shown in *figure 1.b* and this phenomenon is called flat band condition. When a bias voltage is applied, depending on the amount of bias voltage and the surface potential generated on silicon, the regions can be differentiated as accumulation, depletion or inversion. A detailed description of the MOS device technology and its performance can be followed in “Nicollian and Brews” and S. M. Sze [1,2]

The present leap in this technological advancement follows the article published by Gordon Moore, of Fairchild Semiconductor in the journal “Electronics”. The paper titled “Cramming more components onto integrated circuits” observed that “the complexity for minimum component cost has increased at a rate of roughly a factor of two per year [3]. This was in the year 1965, and became known as Moore’s law, “the number of components per IC double every year”. This “law” was later amended to, the number of components per IC doubles every 18 months. In order to satisfy Moore’s law, miniaturization of components on a chip is the only option. One of the first reference to miniaturization, code named as scaling was a classic paper published by R. H. Dennard et. al. [4] and provides the guiding principle for scaling [5]. According to this paper, if a constant electric field is maintained while reducing the device dimension, all other parameters involved in its performance also improves and the circuit becomes faster. It should be noted while scaling; all the properties that a long channel device has must be reproducible for a short channel device also. In order to attain this, the aspect ratio between each component, i.e., the channel length dimension, the gate dielectric dimension and the gate electrode dimension should be maintained. This is easily said but is not simple because as we reach deep-sub micron regime, short channel effects are enhanced.

This chapter gives an overview of the current developments in CMOS devices, especially, gate, channel and temperature engineering. Here, the physical, electrical and temperature effects on the various parameters are discussed.

## [2.1] Engineering the Gate Dielectric & Gate Electrode

The dominance of silicon among other semiconductor materials in the microelectronic industry owes mainly to silicon dioxide. The main characteristic of silicon dioxide is the superior interface quality that it maintains with silicon. But as we reduce the gate dielectric dimension this no longer remains the case. Some of the basic problems of ultrathin oxides are the interface roughness [6], the interface strain [6], dopant diffusion [7,8,9,10] etc. Apart from all these, the unacceptable increase in leakage current proves hazardous to the normal functioning of the device [8,11,12,13].

To overcome some of these problems like reducing dopant diffusion, reducing leakage current, nitridation of the oxide is an immediate solution. Another alternative is to use silicon nitride and high-k materials as gate dielectrics. It is well known that a small amount of nitrogen in the Si/SiO<sub>2</sub> interface reduces the boron penetration [14,15,16,17,18,19,20,21,22,23]. When compared to standard oxides, oxynitrides has higher dielectric permittivity ( $\epsilon$ ) and increased mechanical strength (dielectric constant of SiO<sub>2</sub>=3.9 and for SiN<sub>2</sub>=7, therefore, oxynitrides can have a dielectric constant between 4 and 6.9; Table-1) [15,20]. They are less reactive to gate electrodes and are more resistant to ionizing radiation [20,24]. They also show improved electrical characteristics concerning reduction in interface state density and hot carrier generation, higher immunity towards leakage currents, improvement in breakdown characteristics etc. [22,23,25,26,27,28,29].

The physical structure, distribution, quality and integrity of an oxynitride depend on how it is grown. Some of the common growth techniques that are employed to incorporate nitrogen in oxides are furnace [30,31,32], rapid thermal oxidation (RTO) [30,33,34,35,36,37,38] and downstream plasmas [23,39,40,41]. These growth methods either use nitrous oxide (N<sub>2</sub>O) [30,34,35,38] or nitric oxide (NO) [31,32,37,42] or mixtures of nitrogen and oxygen [37,43,44] gas to incorporate nitrogen. The use of NH<sub>3</sub> for nitridation of gate oxides is also studied extensively [22,45]. A relatively new process of nitrogen incorporation is by implanting N<sup>+</sup> or N<sub>2</sub><sup>+</sup> either into the silicon wafer prior to oxidation [46] or directly into the grown oxides [47,48]. Regarding distribution of nitrogen, thermal oxides are seen to have a roughly uniform nitrogen distribution through out the film and RTO accumulates the nitrogen at the SiO<sub>2</sub>/Si interface or at the surface [30]. While NH<sub>3</sub> gas mixture incorporates maximum amount of nitrogen, the rest of the gaseous mixtures (N<sub>2</sub>O or NO) incorporates fewer amount of nitrogen [49,50]. An advantage of NO over N<sub>2</sub>O is that higher drain current is observed for NO oxynitridated transistors [51]. The drawback of using NH<sub>3</sub> is that the hydrogen is also incorporated along nitrogen and upon biasing the hydrogen migrates to the interface and act as trapping centres paving way to its breakdown [52]. Nitrogen implantation studies carried out in our lab show that depending on the ion implantation dose, the nitrogen concentration can be varied. It is also seen to have uniform nitrogen distribution throughout the film. The amount of nitrogen and its distribution in the SiO<sub>2</sub> region is seen to be a function of post growth implantation annealing temperature. The stoichiometry of oxynitrides processed by this method is similar to that of Si<sub>3</sub>N<sub>4</sub>. Oxidation kinetics is found to depend on nitrogen implantation dose and therefore, oxynitrides grown on nitrogen ion implanted silicon has a lot of potential application for industrial production [53]. Along with these advantages, nitridation also carries some disadvantages like reduction in channel mobility in the transistor [54], which is in general unique to all dielectrics other than silicon dioxide.

Apart from electrical characterization techniques like current-voltage and capacitance-voltage spectroscopy, some of the commonly employed characterization techniques to investigate the polygate/SiO<sub>2</sub>/Si interface are Electron Spin Resonance (ESR) [55,56,57,58,59], Transmission Electron Microscopy (TEM) [60,61], Atomic Force Microscopy (AFM) [62], High resolution X-ray Diffraction (HR-XRD) [63], Infrared Spectroscopy [64], Rutherford Back Scattering (RBS) and Medium Ion Energy Scattering (MEIS) [65,66], X-ray Photoelectron Spectroscopy (XPS) [67,68,69] etc. Though there are a lot of characterization techniques, correlating the structural evaluation with electrical properties gives prompt results, e.g., correlating interface roughness with the interface state density gives an in depth understanding on the performance of the device [57,58,70]; this is because the reliability of the device depends very much on the interface state density and interface roughness.

The MOS devices studied as a part of this thesis consists of thermally grown ultrathin oxides, oxynitrides and nitrogen implanted oxynitrides. In part of this thesis, nitridation of SiO<sub>2</sub> using ion implantation was investigated for ultrathin oxide MOS devices.

## [2.2] Si/SiO<sub>2</sub> Interface Roughness & Interface Strain

According to the semiconductor industry road map [71] the thickness of the SiO<sub>2</sub> will soon reduce to 1 nanometre or about 5 silicon atoms across. Among these 5 silicon atoms at least 2 of them will be at the silicon dioxide interface and their irregularity can change the desired electrical characteristics of the device. Therefore, the roughness of the oxide (surface and interface roughness) should be in an atomic scale if such an ultra thin oxide is to prove a success [6,72]. The roughness of the device influences the scattering parameter and this influences the carrier mobility [73]. This is because the scattering at the interface increases proportionally to the interface roughness. Thus, the roughness increases the interface defects, trap densities, threshold voltage and subsequently decreasing the reliability and changing the function of the device [6,8,74,75,76].

Another parameter of importance is the strain. SiO<sub>2</sub> has an O-Si-O bonding configuration. The bond angle upon total relaxation is about 144°. When this bond angle is distorted, the SiO<sub>2</sub> is under strain. The strain in the system can be differentiated into macroscopic strain and interfacial strain. Macroscopic strain is in the bulk body of the SiO<sub>2</sub> while the interfacial strain extends to a few monolayers into the silicon substrate as well. The strain can be due to various reasons. It can be due to volumetric expansion, thermal expansion or due to external sources like the compressive stress imparted by the gate material on the SiO<sub>2</sub> [6,77,78,79,80]. The volumetric expansion happens because of the large difference in volume between the Si and SiO<sub>2</sub>. Due to volumetric expansion, there can be compressive

stress in the bulk  $\text{SiO}_2$  and tensile strain in the silicon. The thermal stress is due to the large difference between the thermal coefficient of Si and  $\text{SiO}_2$  when the sample is cooled after  $\text{SiO}_2$  growth. The amount of strain in the system depends on the  $\text{SiO}_2$  growth temperature. For oxides grown at higher temperature ( $>950^\circ\text{C}$ ), the stress in the bulk oxide is found to be less and the strain is concentrated in the interface itself [6] while those grown below this temperature, has a high bulk stress and a large interfacial strain. Various models have been proposed to study the growth mechanism and the behaviour of the oxides with respect to the temperature of growth. According to the viscoelastic model, oxide films grown above  $950^\circ\text{C}$  relaxes itself by relieving the stress in them and those grown below this temperature has higher density, high refractive index, large strain and large interface roughness. Similar behaviour is seen in oxynitrides [81,82].

Ultrathin oxides and oxynitrides by thermal oxidation are grown at a lower temperature of around  $800^\circ\text{C}$ . These oxides are dense and are very much stressed. When a voltage bias is applied to these stressed oxides, it is more vulnerable to degradation. This is explained by Yang and Saraswat [83]. They reported a direct correlation between oxide reliability and physical stress at the interface. The mechanical stress of the oxides distorts the bond angle of Si-O-Si, the stress increases the potential energy of the Si-O-Si bond state and forms weaker bonds, energetic electrons ejected during electrical stress break the strained Si-O-Si bonds, resulting in the formation of weak Si-Si bonds. The Si-Si bonds easily trap charges and form a path way for the breakdown on the oxide [83]. Some alternative way to grow better oxides at higher temperature could be by rapid thermal oxidation [6] or to grow these oxides on tilted substrates [66]. Oxides grown on tilted Si substrates have shown higher reliability under stress biasing. This is explained by the negligible strain on the Si-O-Si bonds at the Si/ $\text{SiO}_2$  interface. Presence of nitrogen in low concentration at the interface has shown improvement in hot electron stability and radiation hardness and this is probably due to the relaxation of the  $\text{SiO}_2/\text{Si}$  interfacial strain [82,84]. The mechanism can be explained as follows: the nitrogen atoms bonded to the dangling bonds present in the interface releases the interfacial strain. This could subsequently reduce the trap density, suppressing the breakdown of the oxide and increase the immunity of the trap generation under the current stress. To have a reliable sample, uniform distribution of nitrogen in the bulk film or an equilibrium concentration of nitrogen at the interface is desirable [84].

In part of this thesis, I have employed transmission electron microscopy (TEM) and high resolution X-ray diffraction (HRXRD) to study the strain and interface roughness of oxidized and oxynitridated poly-Si gate and poly- $\text{Si}_{1-x}\text{Ge}_x$  gate MOS devices.

## [2.3] Thoughts for the Future:-High-k Dielectric

High-k dielectrics are those with a dielectric constant above that of silicon nitride i.e., above 7 Farad/centimetre (F/cm). The equivalent oxide thickness (the thickness that SiO<sub>2</sub> would have for a given capacitance) of a high-k dielectric is higher than that of silicon dioxide and this is one of its primary advantage. Since high-k dielectrics have higher thickness, there will be less leakage current and boron penetration (boron penetration if polysilicon is used as the gate electrode). For example, for an equivalent oxide thickness of 1.2 nm, a high-k dielectric like Ta<sub>2</sub>O<sub>5</sub> with a dielectric constant of 25 can have a thickness of around 7.5 nm. These values follow the equation developed for the equivalent oxide thickness,

$$EOT = (k_{SiO_2} / k_x) t_x$$

where,  $k_x$  is the  $k$  value for the film of interest,  $t_x$  is the physical thickness of the film of interest and  $k_{SiO_2}$  is the  $k$  value of silicon dioxide. The selection of a high- $k$  dielectric not only depends on the value of its dielectric constant (dielectric property) but also on the band gap energy and the electronic property of the semiconductor-dielectric interface [85].

The most basic issues for the selection of a high-k dielectric are (1) the chemical compatibility of the dielectric material with the silicon channel (2) the chemical compatibility of the dielectric with the gate electrode. These in turn depend on the process condition to which high-k dielectrics are exposed under the current MOS technology [85]. Therefore, the material must have thermodynamical stability and good adhesion with silicon. They should be process compatible (like ability to be patterned easily) and should have low deposition temperature. They should have high breakdown voltage, low defect density, and low charge states on silicon. The likely transport property of the dielectric should also be taken into consideration [85]. Another condition is that the switching frequency should also be high [86]. The characteristics of these dielectrics also depend on the method with which they are grown like epitaxy (molecular beam epitaxy and chemical vapour deposition), sputtering etc. So it is also a necessity to find out a cheaper growth method. Some of the problems that are necessary to be solved with the existing MOS technology are that they should also be compatible with the gate electrode (as mentioned earlier). The present CMOS technology uses poly-silicon as the gate electrode. Though the compatibility of the high-k dielectric with the polysilicon gate is envisaged, it is a difficult problem to be solved. A metal gate electrode is a good solution for high- $k$  dielectric materials. So a compatible metal gate should be introduced. Until these basic issues are solved, it is a long way for these materials to be implemented in CMOS devices.

Some of the alternate dielectrics discussed in the literature are Al<sub>2</sub>O<sub>3</sub> [87], Y<sub>2</sub>O<sub>3</sub> [88,89], La<sub>2</sub>O<sub>3</sub> [89], Ta<sub>2</sub>O<sub>5</sub> [90,91], TiO<sub>2</sub> [92,93], ZrO<sub>2</sub> [94,95], HfO<sub>2</sub> [94,96,97] etc. Table-1 gives their dielectric constant, band gap and crystal structure and a comparison with SiO<sub>2</sub>

[85,98]. Most of the dielectrics shown in the table are thermodynamically stable with Silicon. In order to have a better compatibility with silicon, some of these dielectrics have also been grown on SiO<sub>2</sub> [95]. There are also several other dielectrics that are not given in the table but have been investigated at least once. Worth mentioning would be perovskites (e.g., BaSrTiO<sub>3</sub>, PbZrTiO<sub>3</sub> etc) that are suitable for using in dynamic random access memories [99].

**Table-1:- Dielectric constant, energy band gap and crystal structure of various high-k dielectric materials.**

Material	Dielectric Constant	Bandgap E <sub>G</sub> (eV)	Crystal Structure
SiO <sub>2</sub>	3.9	8.9	Amorphous
Si <sub>3</sub> N <sub>4</sub>	7	5.1	Amorphous
Si <sub>x</sub> N <sub>y</sub> O <sub>z</sub>	4-6.9	---	Amorphous
Al <sub>2</sub> O <sub>3</sub>	9	8.7	Amorphous
Y <sub>2</sub> O <sub>3</sub>	15	5.6	Cubic
La <sub>2</sub> O <sub>3</sub>	30	4.3	Hexagonal, Cubic
Ta <sub>2</sub> O <sub>3</sub>	25	4.5	Orthorhombic
TiO <sub>2</sub>	80	3.5	Tetragonal
ZrO <sub>2</sub>	25	7.8	Monoclinic, Tetragonal, cubic
HfO <sub>2</sub>	25	5.7	Monoclinic, Tetragonal, cubic
ZrO <sub>2</sub> .SiO <sub>2</sub>	~12	---	---
HfO <sub>2</sub> .SiO <sub>2</sub>	~11	---	---
BST (BaSrTiO <sub>3</sub> )	300	---	---

## [2.4] Gate Electrodes

Poly-Si has been used as the gate electrode since the 80s due to its compatibility in silicon processing, superior “all weather” interface quality with gate dielectric. Ideally, the work function difference between the poly-gate and the silicon substrate is zero, which gives it the primary advantage in usage. But, in deep sub-micron regime, the compatibility of poly-Si is questionable due to several problems like poly-depletion, dopant diffusion (problems are acute when doping is higher), high leakage current etc. Also, the series resistance is seen to increase with scaling. Series resistance should be less otherwise, the RC (resistance-capacitance) delay in a circuit becomes large and this will limit the speed of the device. Due to the low work function, they are suitable to be used as a buried channel device, but as the

scaling is applied, punch through effects and drain induced barrier lowering in the silicon channel deter them from this model.

In order to solve the above mentioned problems in poly-Si, alternate gate electrodes are proposed. When a gate electrode material is chosen, the compatibility with the gate dielectric and to the existing microelectronic processing must be taken care of. They should also have a suitable work function. With high-K dielectric materials being inevitable for the future CMOS device, future gate electrodes can be substituted by the metal electrodes. As long as the silicon dioxide dielectric remains in the CMOS devices, poly-silicon will also try to remain as the most compatible gate material. But, due to the increase in poly-depletion effect in short channel CMOS, compatible metal gate electrodes are recommended for further investigation. One more important technology to be mentioned here is the IBM's "dual gates" that can further reduce the size of CMOS to the 0.1  $\mu\text{m}$  range. This double gate FET technology frees device characteristics from dependence on the bulk properties of doped semiconductors and instead defines the FET channel by the physical shape of the undoped silicon. Basically this is an important step towards miniaturization and this architecture can solve the problems related to channel doping [100]. In this device model, a reduction in the direct tunnelling current is also observed in the ultrathin oxide regime [101]. But even for this device design, problems related to poly depletion are still present [102].

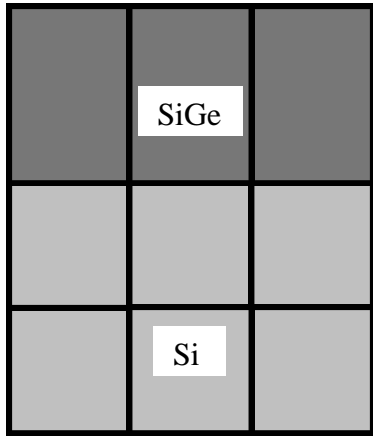
An immediate solution to substitute poly-Si gate electrodes is to use poly-Si<sub>1-x</sub>Ge<sub>x</sub> alloys. Advantages in using poly-Si<sub>1-x</sub>Ge<sub>x</sub> gate electrodes are that their work function can be tuned depending on the Ge fraction used. In addition, they also provide lower resistivity, reduced gate depletion and reduced boron penetration [103,104]. Poly-Si<sub>1-x</sub>Ge<sub>x</sub> has also been used in dual gate technology and reduced gate depletion was observed [102]. In this thesis, we have used poly-Si<sub>1-x</sub>Ge<sub>x</sub> gates with two different Ge concentration, 20 and 35%. The electrical and structural characterization presented in thesis is based on these structures.

## [2.5] Channel Engineering:-Virtual Substrates

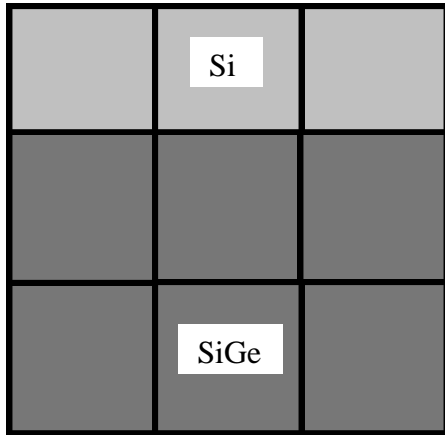
In the deep sub micron regime, control of mobility by channel engineering has become a popular option. Channel engineering is nothing but the epitaxial growth of "virtual substrates" on Si, and the manipulation of strain (strain between two layers develops during the growth) for improving the performance of the device, or by using buried channels, e.g., quantum wells. The former option has been investigated in this thesis. The publication by IBM in the Kyoto VLSI symposium, 2001, shows that when strain is introduced into a fairly standard CMOS process, carrier mobilities can improve by as much as 70 % and the current drive by 35% [105,106]. Apart from the contribution to the CMOS technology, the path to channel engineering also gives an option to integrate the silicon technology with the existing

optical devices belonging to both III-V and II-VI elements in the periodic table [107,108]. The advantage is that this can provide ultrawide bandwidth optical interconnects for high speed information processing [109]. By such integration, not only the cost of the material but the weight of the total component is reduced dramatically, while increasing the mechanical reliability. This is very much advantageous for components used in space applications. Energy sources like space photovoltaic cells will then become a light weight commodity. Silicon integration is also advantageous for Ge based devices such as infrared photo detectors.

Virtual substrates grown epitaxially on silicon are relaxed Ge or relaxed  $\text{Si}_{1-x}\text{Ge}_x$  alloys. The lattice mismatch between Si and Ge is around 4.17%. When Ge is grown on Si, the lattice



**Fig. 2.2a:** Compression; Strained  $\text{Si}_{1-x}\text{Ge}_x$  on relaxed Si



**Fig. 2.2b:** Tension; Strained Si on relaxed  $\text{Si}_{1-x}\text{Ge}_x$

difference induces strain in the epitaxially grown layer. This layer is highly strained if their growth is below a critical thickness. The lattice mismatch is measured by the misfit parameter  $f_m(X)$  defined below.

$$f_m(X) = \frac{a_l(X) - a_{sub}}{a_{sub}}$$

Here  $a_l(X)$  is the lattice constant of the alloy,  $a_{sub}$  is the lattice constant of the substrate, and  $X$  is the concentration of the Ge in the  $\text{Si}_{1-x}\text{Ge}_x$  epilayer. If both the misfit parameter  $f_m(X)$  and the thickness  $h$  of the epilayer are small, the misfit between the two semiconductors is accommodated by a tetragonal strain. The strain is compressive if  $a_l(X) > a_{sub}$ , and it is tensile if  $a_l(X) < a_{sub}$  [110]. Figure-2.2a-b show when the layer is under compressive or tensile strain.

The strain can be varied by changing the composition of Si and Ge in the grown layer. For most of the applications thicker virtual substrates are necessary. The growth of high quality defect free substrates is difficult because of the difference in atomic spacing between the substrate and the grown layer which can cause elastic distortion. A lot of research input is needed to mature this technique.

If the internal energy exceeds the elastic strain regime, plastic deformation occurs. Plastic deformations are followed by misfit dislocations. Misfit dislocations arising at the  $\text{Si}/\text{Si}_{1-x}\text{Ge}_x$  (substrate-layer) interface can nucleate dislocation loops that propagate to the surface of the layer and finally to the active region of the device. Misfit dislocations are formed either by nucleation and expansion of surface half



loops or through the propagation of existing threading dislocations. Along with misfit dislocations, the strain field creates a cross hatch pattern on the surface of the grown epilayer [111,112]. The cross hatch pattern occurs in the form of trenches and ridges. The variation in surface morphology makes the patterning of the device difficult. In a nutshell, in relaxed buffer layers strain relaxation takes place by the creation of misfit dislocations. A Fundamental understanding on the formation of misfit dislocation and their propagation can be referred to the Force Balance Theory by Mathews and Blackeslee [113] and Principle of Energy Minimization by Ball and Van der Merwe [114,115].

The primary function of buffer layers is to relieve misfit strain in such a way as to produce a surface which is suitable for the subsequent growth of a device structure. In other words a buffer layer should be an effective substitute for a substrate that can provide a suitable lattice parameter. This means that the surface of the buffer layer must be lattice matched to the material used to grow the device, the surface must be flat and the threading dislocation density must be sufficiently low. Some devices may have more requirements for the buffer layer, like the buffer layer may be a part of a conducting pathway between the device and the back of the substrate, or it may have to be semi-insulating to give device isolation. It may have to possess a particular doping level or conductivity if a depletion region is to be formed, and it may even form part of the device structure itself. In a nutshell, the primary requirements of a buffer layer are strain relief, flatness and reduced threading dislocation density. These norms are regardless of the specific requirements for individual devices.

All these factors are dependent on the type of growth method that is used for the growth of the epilayer. These structures can be grown by various growth techniques with different growth parameters. The methodology by which these are grown determines the quality of the layer.

There are mainly four different routes of obtaining relaxed buffer layers, 1) the post processing of strained  $\text{Si}_{1-x}\text{Ge}_x$  [116,117,118], 2) the approach of using graded layer [119,120], 3) single and direct Ge epitaxy on Si with or without surfactant [121,122,123], 4) to use a compliant Si based substrate [124,125,126]. More recently relaxed buffer layers are grown by a new technique called epitaxial necking [127].

In part of this thesis, we have investigated the properties of overgrown  $\text{Si}_{1-x}\text{Ge}_x$  layers on relaxed pure Ge buffer layers using high resolution X-ray diffractometer.

## [2.6] Temperature Engineering

As the CMOS scaling in all dimensions is seeking new solutions for better performance, researchers now look forward to exploit the cryogenic performance of these devices. Compared to room temperature performance, there are substantial improvements in the device function at low temperature. Fundamental study can improve not only the performance at low temperature but can substantially promote the understanding of the device at room temperature. When designing a low temperature CMOS device, more emphasis must be given to study the change in material properties with decreasing temperature [128]. Some of the advantages of the device at low temperatures are;

- 1) Higher mobility can be obtained at low temperature. This will increase the transistor switching speeds because it is proportional to the mean carrier velocity in the device and mobility is the ratio of electron or hole velocities to electric field. We know that mobility increases as temperature decreases due to a reduction of carrier scattering from thermal vibrations of the semiconductor crystal lattice.
- 2) Another major improvement of the device at cryo-temperature is the reduction in leakage currents. As the leakage current is reduced there is also a reduction in noise ratio. The combination of these, together with the lower noise of CMOS circuits at low temperatures, yields both faster signals and higher signal-to-noise ratio.
- 3) Apart from the improvements in the performance of the device at low temperature, reliability of the device is also seen to improve. The reliability of a CMOS device is a strong function of operating voltage and temperature. According to Clark et. al., the mean-time-to-fail (MTTF) is proportional to temperature and is expressed by an Arrhenius relation;  $MTTF \propto e^{[(\Delta H/k)(1/T_0 - 1/T_R)]}$  where  $k$  is the Boltzmann constant,  $T_0$  and  $T_R$  are the operating temperature and reference temperature, respectively, and  $\Delta H$ , is a parameter related to the activation energy of a given thermal process.  $\Delta H$  is typically in the range of 0.3 to 1.2 eV. The improvement in reliability is due to the increase in gate oxide reliability at low temperature. The integrity in gate oxide is due to the negligible ionic mobility through the interface at low temperature that causes degradation [129]. The degradation due to electromigration is also reduced at low temperature. Some other problems that can be faced are degradation due to hot carriers (at low temperature hot carriers degradation is higher) [130].
- 4) Another reason for using the cryo cooled devices is to keep the temperature below the operational temperature limit. The heat dissipated by the device is detrimental both to the device and to the package. Instead of air cooling, it is more advantages to use cryo cooled devices.

However, cryo cooled devices have disadvantages of high cost, extra energy necessary for refrigeration and the packaging space required for the refrigeration. Apart from this,

fundamental studies have shown that there are some defects and problems which are unique to low temperature [131,132]. Some other reliability issues that can appear due to the thermal cycling, i.e. thermal excursion from room temperature to low temperature and vice versa can cause potential damage to the device and device packaging systems.

In part of this thesis, we have studied the cryogenic (low temperature) performance of ultrathin oxide and oxynitridated MOS devices having poly-Si<sub>1-x</sub>Ge<sub>x</sub> ( $x = 0.2$  and  $0.35$ ) and poly-Si gate electrodes.

It is also worth mentioning about the silicon MOS devices that are presently used for high temperature applications. High temperature generally means those temperatures above 125 °C because normally silicon devices are designed to work only till this temperature range [133]. But majority of high temperature applications are normally below 300 °C. High temperature devices are used for automotive applications, aircraft industry, and for petrochemical well-logging (oil well drilling). Though silicon bipolar transistors were used extensively to meet these requirements, CMOS devices are now being targeted due to their simplicity [133].

## [2.7] Sample Preparation

### [2.7.1] Virtual Substrates

For channel engineering, strained Si<sub>1-x</sub>Ge<sub>x</sub> was grown on Ge epilayer which is indeed grown on Si. The growth of these epilayers was performed by Chemical Vapour Deposition (CVD). These samples are grown in “STMicronics”.

### [2.7.2] CMOS Structures

The samples used for the low temperature electrical measurements, oxynitridation study and the structural investigation are PMOS capacitors. The PMOS capacitors were fabricated on 0.142 ohm cm (100) n type Si wafer. These wafers are from Wacker Siltronic. The n-type doping concentration measured from CV measurement technique is of the order of  $5-6 \times 10^{16} \text{ cm}^{-3}$ . This is consistent with the manufactures data. Ultrathin Silicon dioxide SiO<sub>2</sub> and Silicon oxynitrides (SiON) are grown on them through thermal oxidation technique. The thickness of these oxides according to the optical measurements (Ellipsometry) and Transmission Electron Microscopy (TEM) was in the range 2 to 3 nm. These oxides are grown at a temperature of around 750 to 800 °C, using ASM A400 vertical furnace. Poly-Si and poly-Si<sub>1-x</sub>Ge<sub>x</sub> with various Ge concentrations were deposited on these oxides with an LPCVD ASM system. The gases used for their deposition are SiH<sub>4</sub> (Silane) and GeH<sub>4</sub>

(Germane) at a pressure of 40 torr and temperature of 615 °C and 640 °C, respectively. Some of these samples were insitu doped using diborane ( $B_2H_6$ ) gas. Prior to the deposition of poly Si/poly- $Si_{1-x}Ge_x$ , an undoped Si seed layer with a nominal thickness of 1 nm was deposited at 615 °C. This helps in the nucleation of poly-silicon. The thickness of the gate layers was 200 nm according to optical tencor spectramap measurements.

Some of the samples with pure oxides, and undoped poly- $Si_{1-x}Ge_x$  gate electrodes were oxynitridated by nitrogen ion implantation. Atomic nitrogen ions were implanted by using a Varian DF4 ion implanter. The implantation energy was 50 keV which places the peak of the N distribution in the middle of the  $Si_{1-x}Ge_x$  gate. The N distribution was estimated by simulation program TRIM prior to the implantation and confirmed by the SIMS measurement after the implantation. The dose of the implanted N ions was  $5 \times 10^{14} \text{ cm}^{-2}$ ,  $2 \times 10^{15} \text{ cm}^{-2}$  and  $5 \times 10^{15} \text{ cm}^{-2}$ . After nitrogen implantation rapid thermal annealing was carried out to find the optimal temperature and time for the oxynitridation formation. Boron implantation on these samples was later performed through ion implantation. Boron implanted N-ion oxynitridated samples are now under investigation with emphasis on their electrical performance.

For electrical measurements, mesa structures were fabricated on them using photolithography. These mesa structures are of the size of 500 to 200  $\mu\text{m}$ . For contacts to these structures, aluminium metallization of an average thickness of 500 nm was done both on these mesa structure, i.e. on poly part and also for back side contact on the silicon.

I recognize that many physicists are smarter than I am--most of them theoretical physicists. A lot of smart people have gone into theoretical physics; therefore the field is extremely competitive. I console myself with the thought that although they may be smarter and may be deeper thinkers than I am, I have broader interests than they have.

**Pauling, Linus**  
(1901-1994) b. Portland, Oregon

Linus Pauling, *The Meaning of Life*, Edited by David Friend and the editors of *Life*, Little Brown, New York, 1990, p. 69. (6)

# 3

## Nanoscaled Semiconductor Structures and Relevant Processing Problems

In this chapter, a brief introduction about heterostructures and low dimensional structures is given. The later part deals with thermal processing and hydrogen passivation effects relevant to semiconductor heterostructures. The description on the samples used for these studies is also given at the end of the chapter.

### [3.1] Heterostructures

The credit for the present day communication revolution goes to novel semiconductor heterostructure device designs. For example, the possibility of optically transmitting electrical signals through fibre optics cables (i.e., converting electrical signals into optical signals and vice versa is done using a semiconductor) would not have been possible without combining different elemental materials together, to form novel designs of compound semiconductors and then growing them epitaxially on another wafer (for example,  $\text{In}_x\text{Ga}_{1-x}\text{As}$  grown on GaAs). Heterostructures are formed when two or more different semiconductor layers grown epitaxially on top of each other. These semiconductor layers will be in intimate contact. An ideal heterostructure should have an abrupt heterojunction. A heterojunction is the junction between two different semiconductors.

An abrupt heterojunction is too difficult to achieve and there can be an interface roughness between the two layers. If there is a lattice mismatch between the substrate and the layer that is to be deposited, first few layers will be highly strained (the maximum thickness up to which it can be highly strained and defect free is its critical thickness). If the growth is continued, strain release between the layers can create dislocation. Depending on the dislocation density, creep formation can take place in the grown structure. Such defects make the structure impossible to be used as an active part of a device because defects create

interface trap centres. When a bias is applied, trap centres act as charge trapping centres. An ideal heterostructure should have a minimum defect density and interface roughness. So, the research in the growth of heterostructures revolves around creating a defect free sample. In order to reduce defect formation, an epitaxial layer is grown on a lattice matched substrate. But it is also found that highly strained epitaxial layers such as  $\text{Si}_{1-x}\text{Ge}_x$  can be designed as a high mobility transistors and its performance is much higher than unstrained silicon. [134, 135, 136]. This is because of the strain induced reduction in bandgap and this phenomenon is commonly referred as “bandgap engineering”.

For a long time, the research on growing epitaxial layers had been concentrated on chemically similar structures; for example, when InAs is grown on GaAs (both are chemically similar materials as they belong to the III-V column in the periodic table), or when  $\text{Cd}_{1-x}\text{Zn}_x\text{Te}$  is grown on  $\text{Cd}_{1-x}\text{Zn}_x\text{Te}$  (both belong to group II-VI column in the periodic table) or when  $\text{Si}_{1-x}\text{Ge}_x$  is grown on Si or Ge layer (both belong to the group IV). As the demand for the integration of all other materials with the silicon technology increased, there have been attempts to grow chemically dissimilar materials on silicon; for example, attempts are being made to grow defect free GaAs on Si or on Ge.

## [3.2] Low Dimensional Semiconductor Heterostructures

Low dimensional semiconductor structures are of importance as they generate new ideas in band structure engineering. By low dimension, we mean that the structure is reduced in its size. Thus in a low dimensional structure the geometrical characteristics of the structure dominates the physical property of the material. When the size of the heterostructure is reduced, quantum phenomena start appearing. By properly designing the geometrical dimensionality of the material, one can obtain the desired property which is impossible with the bulk form (homostucture of the material). This technology is called band gap engineering. A good example is the fabrication of double heterostructure lasers [137].

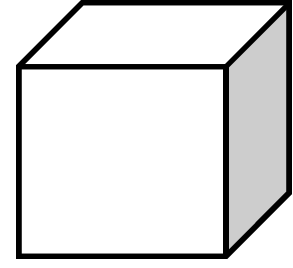
### [3.2.1] Quantum Well

When a material of lower bandgap is sandwiched between two materials of higher bandgap and if the geometrical dimension of this interlayer is so small that electrons can freely move only along two directions while motion is restricted along the third direction, we define such a system as the so called quantum well. The degree of freedom for an electron is only along x and y directions and not along the z direction. The confinement of electrons is preferably in the growth direction of the structure and it results in quantization of the electron energy.

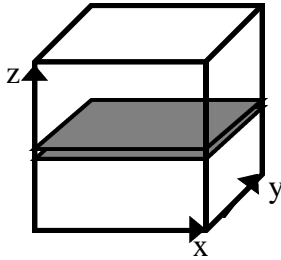
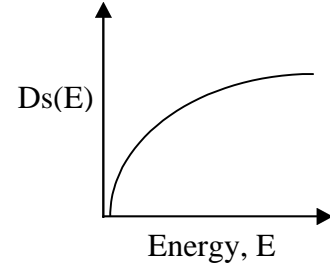
The kinetic energy of electrons in a bulk material [138] is given as

$$E = \frac{\hbar^2}{2m^*} (k_x^2 + k_y^2 + k_z^2).$$

Here,  $m^*$  is the effective mass,  $k_{x,y,z}$  are the wavevectors in all three directions. Density of states of a bulk system is  $Ds(E) \propto E^{1/2}$ . A schematic diagram of a bulk system and its energy spectrum is given in Figure 3.1. The continuous form of density of states starts disappearing as the low dimensional system march from quantum well to quantum dots.



Bulk material; 3D



Quantum well; 2D

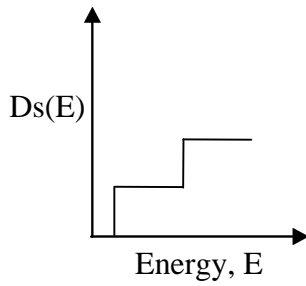


Fig. 3.2

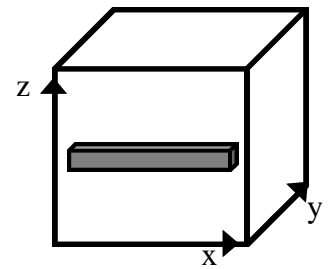
When it comes to the kinetic energy of electron in a quantum well, it can be written as [138];

$$E = \frac{\hbar^2}{2m^*} (k_x^2 + k_y^2) + E_z^i$$

where  $i=1,2,3,\dots$   $\hbar$  is the Planck's constant and  $m^*$  is the carrier effective mass.  $k_{x,y}$  are the wave vectors along the respective directions. Density of states is highly modified near the quantization energies, showing step like behaviour. A schematic diagram of a quantum well and its energy spectrum is given in Figure 3.2.

### [3.2.2] Quantum Wire

In a quantum wire, this dimensional limit is maintained along two dimensions and the electrons are allowed to move freely only along one direction. A schematic diagram of the quantum wire and its energy spectrum is given in Figure 3.3. As shown in the figure, the degree of freedom for an electron is only along x direction while the electrons are not allowed to move along the y and z direction. So the quantization of charge takes place in the y and z direction.



Quantum wire; 1D

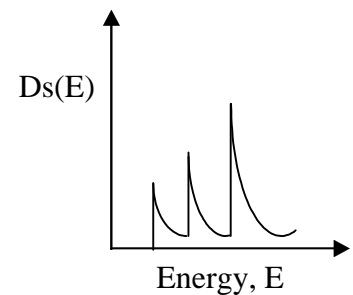


Fig. 3.3



The energy of electron in a quantum wire is written as [138];

$$E = \frac{\hbar^2}{2m^*} (k_x^2) + E_y^i + E_z^j$$

where  $j=1,2,3,\dots,h$  is the Planks constant and  $m^*$  is the carrier effective mass.  $k_x$  is the wave vectors along the x directions. Density of states is highly peaked and its modification from the quantum well-DOS takes place at all relevant energies [138] (figure 3.3).

### [3.2.3] Quantum Dot

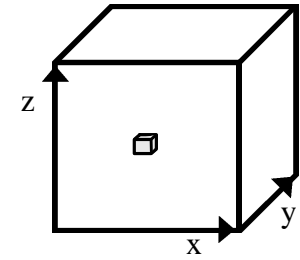
Among all these quantum structures, quantum dots are the most fascinating designs in the quantum regime. They are nanometre sized and are three dimensionally confined system. Figure 3.4 gives the schematic diagram of the quantum dot and its energy spectrum. As is shown in the figure 3.4, the quantum dot resembles a particle in a box. Since the electrons are confined in this system, the electron energy is quantized. Discrete lines are thus observed.

Energy of electron in a quantum dot is written as [138];

$$E = E_y^i + E_x^j + E_z^k$$

where  $i,j,k=1,2,3,\dots$ . Density of states is a series of  $\delta$  function peaks as shown in the figure 3.4.

Some of the characteristics of a quantum dot is similar to that of an atom, and therefore, they are also called as “artificial atoms” (by Maksym and Chakraborty) [138,139,140] and “designer atoms” (by Reed) [138,141]. Though they are called so, it has differences from real atoms, as they are much larger than atoms (since more than one atom is present) [138]. In general, quantum dots combine both single atomic property and the bulk property of a semiconductor [142,143] Apart from this, since the electrons are confined inside the dot, they have reduced electron-phonon interaction and therefore result in slow intersubband relaxation [144,145,146]. Though discrete spectral lines are possible in ideal case, in reality it has not yet been possible to obtain discrete lines for an ensemble of dots and the reasons are the interface roughness and the fluctuation in size between individual dots. Size fluctuations between single dots will lead to a statistical distribution of the eigen energies, characterized by a spectral width. However, micro-photoluminescence study has shown that ultranarrow luminescence can be observed which directly prove their  $\delta$ -function-like density of states [147,148].



Quantum Dot; 0D

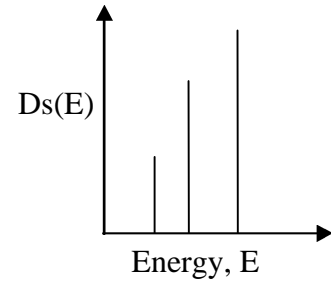
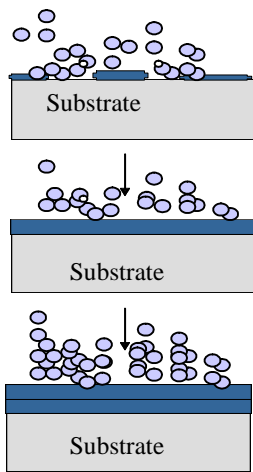


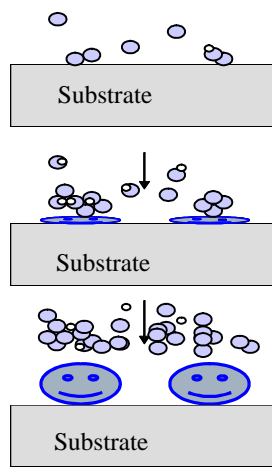
Fig. 3.4

### [3.3] Growth Methods

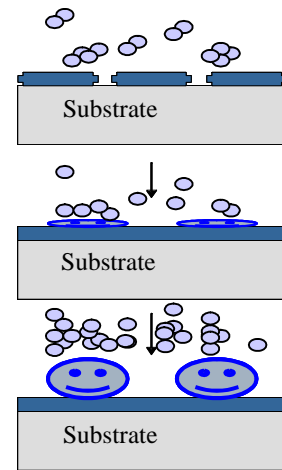
The two most successful methods of epitaxially growing heterostructures are by *Molecular Beam Epitaxy* (MBE) [149] and *Chemical Vapour Deposition* (CVD) [150]. These growth techniques have precise control over the growth structures in atomic scales. Liquid Phase Epitaxy growth method has also been used for the growth of heterostructure fabrication. There are basically three growth modes for epitaxial films. They are Frank-van der Merwe (F-M) [143,151], Volmer-Weber (V-W) [143,152] and Stranski-Krastanov (S-K) [143,153] and are as shown in figures 3.5a-c.



**Fig. 3.5a:** Frank-Van der Merwe Growth



**Fig. 3.5b:** Volmer-Weber Growth



**Fig. 3.5c:** Stranski-Krastanov Growth

F-M mode is useful in growing atomically smooth layers and is generally useful for homoepitaxy. Quantum wells are grown using this method. V-W and S-K modes can be used for growing quantum dots. In V-W growth mode, atoms nucleate at random positions but it does not have necessary control over the growth process for quantum dots.

S-K growth combines the properties of both F-M and V-W process. In S-K method, growth begins with the F-M mode (i.e., a wetting layer is formed first) and ends with the V-W mode (i.e., quantum dots are formed in random positions). S-K growth process occurs when there is a large lattice mismatch between the two heterostructure constituent materials. For example, there is a lattice mismatch of around 7% when InAs quantum dots are grown on GaAs substrate. Due to this lattice mismatch, elastic strain energy is accumulated in the epilayers which helps the layer to grow. These above said epitaxial growth methods are all self assembled growth process. For a quantum dot, self assembly means they are formed automatically. This term was indeed defined by Kuhn and Ulman as “a process in which

supermolecular hierarchical organization is established in a complex system of interlocking components” [154].

Semiconductor quantum dots can also be fabricated on patterned substrates through lithography. In fact, this was the mode of growth in the beginning of quantum dot development. But the processing induced damages outlived the real efficiency that the quantum dots could give and is now rarely used. The advantage of fabricating QD by lithography is that they can be processed in a predefined pattern.

### [3.4] Thermal Processing

In ultra large scale integration (ULSI) technology, fabrication of a microelectronic device from a semiconductor wafer involves a lot of unavoidable thermal processing steps. The annealing temperature depends on the particular processing step involved and the kind of semiconductor material used. For example, to activate the ion implanted dopant, high temperature annealing (~900-1100 °C) is performed in silicon. High temperature is a relative term and for an epitaxially grown semiconductor wafer, this temperature could be above its growth temperature. This also depends on the method of thermal processing.

The two most basic and widely used thermal processing methods are furnace annealing and rapid thermal annealing. Among these two, furnace annealing is the traditional and the most dominating processing step and this is what we have employed in this part of our investigations. Since thermal processing has to be done at these critical temperatures, stability of the semiconductor is an issue of importance to be studied in details.

What is stability for a semiconductor structure? This could be better explained with an example. To fabricate a high performance transistor with a  $\text{Si}_{1-x}\text{Ge}_x$  low dimensional heterostructure, high temperature annealing is necessary for dopant activation. If the growth temperature of this sample is not known, the specific temperature used can cause strain relaxation and alloy intermixing i.e. Ge can inter diffuse. This can damage the  $\text{Si}_{1-x}\text{Ge}_x/\text{Si}$  interface resulting in a change of the device characteristics. The temperature used for dopant activation is also critical as dopants can diffuse through heterostructures causing unwanted device characteristics. Therefore, thorough knowledge about a range of temperatures that can be used for a particular device fabrication step is necessary to be known prior to begin a processing sequence. Apart from considering post processing temperature, it is also necessary to know the thermal characteristics of alloy mixtures before growing a stable structure. This is particularly needed to grow stable multilayer structures and super lattices as the electrical and optical characteristics depend on the interface.

Though interdiffusion can be considered as a thermal instability problem in semiconductor heterostructures, sometimes it can also be useful. For example, post growth

thermal treatment of self assembled InAs quantum dots is found to modify its structural and optical properties. Rapid thermal annealing of InAs dots increases their lateral sizes. Large blue shift in the emission energy, significant linewidth narrowing and decrease in the luminescence peaks have been observed for the annealed samples [155,156]. Some researchers have also observed increase in the luminescence peaks after annealing [157].

The thermal stability studies done in our lab on  $\text{Si}_{1-x}\text{Ge}_x$  single and double quantum wells grown by CVD show that they are much stable compared to MBE samples. Our results show that interlayer diffusion depends on the design of the quantum well. We have also found that the local relaxation of high temperature grown samples was higher compared to low temperature grown samples [158]. The appended paper-VIII is about the thermal stability studies done on  $\text{CdZn}_{1-x}\text{Te}_x$  quantum wells grown by MBE. In this article, we employed high resolution X-ray diffraction to investigate the stability and alloy interdiffusion characteristics on these structures.

In general, we have chosen a variety of samples (ranging from semiconductor epilayers to quantum dots) to study their post process thermal stability for a particular growth method. The different semiconductors that are studied have interesting electronics and optoelectronics applications. Major characterization tools used for these studies were photoluminescence spectroscopy and high resolution X-ray diffraction.

### [3.5] Hydrogen and Deuterium in Semiconductors

Hydrogen has played an important role in the development of semiconductors and semiconductor devices. It has also fascinated fundamental semiconductor researchers for the past two decades. The vast majority of questions pondering the role of hydrogen in elemental, alloyed and compound semiconductors have been extensively dealt with both theoretically and experimentally. The incorporation of hydrogen into a semiconductor changes the properties of surfaces, interfaces, impurities and defects, apart from its change in the total bulk property of a semiconductor. The change in these properties effectively changes its electrical and optical property. It could also be said that atomic hydrogen passivates both shallow donors and acceptors in a semiconductor: the passivation efficiency depends on the kind of impurity involved. In semiconductor heterostructures, it has been found that the dislocations and defects can be passivated by hydrogen giving them much higher efficiency. As a part of this thesis, we have studied hydrogen passivation of dopants in  $\text{CdZn}_{1-x}\text{Te}_x$  quantum well heterostructure and defect passivation in InAs quantum dots.

The incorporation of H into a semiconductor is an unavoidable device fabrication problem. Fabrication of a semiconductor device involves a large number of processing steps. These processing steps inevitably expose the semiconductor to hydrogen environment, which can lead to hydrogen incorporation. The incorporation of hydrogen both intentional and unintentional has advantages as well as disadvantages. Sticking on to its

advantages, it is seen that presence of hydrogen during the growth is very beneficial for the production of p-type GaN. In p-type GaN hydrogen suppresses the native-defect compensation and enhances the acceptor solubility [159]. However, the hydrogen also neutralizes acceptors. To deactivate the passivated acceptors, thermal annealing or electron radiation is required. In float zoned Si, hydrogen is used to suppress swirl defects [160]. The most notable disadvantage is the passivation of shallow impurities by hydrogen. This is generally not desirable because such passivation eliminates the intended electrical activity of both donor and acceptor atoms and this in turn will strongly affect the device behaviour, i.e. the switching and transmission characteristics of a device will be adversely affected [159,161].

### [3.6] Sources of Hydrogen in Device Processing

Hydrogen being a light material is easy to get diffused into the semiconductor. There are a number of processing steps, which contributes to the hydrogen incorporation. The source of hydrogen incorporation can either be intentional or unintentional. Both these modes are explained here, respectively.

#### [3.6.1] Hydrogen Implantation

Hydrogen implantation is widely used in electronic and photonic devices to isolate neighbouring devices. Usually, low ion energy and high beam current is employed to actually implant hydrogen. Upon implantation, the damage produced reduces carrier mobility in the material and creates deep level centres, which trap free carriers. Once the material is implanted, it will exhibit high resistivity. These schemes are widely used in III-V semiconductors and in silicon. On annealing the implanted sample, H produces dislocations, stacking faults, vacancies, interstitials and complexes. In short, implantation (of H for the device isolation) and annealing damages the sample [161,162]. The damage created in the semiconductor has adverse effects on its electrical properties and these defects could also dominate the transport mechanism.

#### [3.6.2] Annealing in H<sub>2</sub> -Containing Ambient

Hydrogen is often used as an annealing ambient in order to prevent oxidation of the semiconductor surface. There are a variety of heat treatments done during processing, such as, annealing for activating implanted ions, for ohmic contacts to make alloys and for "after-implant" isolation. All this annealing is usually performed in H<sub>2</sub> containing ambient. The annealing can bring in the passivation of near surface dopants. The annealing in H<sub>2</sub> ambient can also cause "out-diffusion" of existing H in the semiconductor [161].

### [3.6.3] Hydrogen Plasma

This is a very common method for hydrogen incorporation. Usually the sample is exposed to low power-density  $H_2$  plasma for hydrogen incorporation. Basically any system in which hydrogen glow discharge of plasma is produced can be used to hydrogenate a semiconductor sample. There are several methods for hydrogen plasma creation, like, RF plasma, microwave plasma and dc-plasma. Hydrogen incorporation using plasma technique is an effective method for defect neutralization. This technique depends very much on the sample temperature, i.e. the temperature at which the sample is heated during the plasma exposure. For example, the exposure of hydrogen plasma on InP at a temperature of 95~100-degree Celsius can produce an increase in the 77 K photoluminescence intensity. This increase in PL is due to the passivation of non-radiative surface states. But upon exposure above 100 degree Celsius leads to a loss of phosphorous with indium droplets left on the surface [161]. Hydrogen plasma can also be effective in removing oxides and carbon contamination from the surface of certain semiconductors even at very low temperature. The most simple uses chambers having a two-electrode electrochemical cell. This simple technique of inserting hydrogen is damage free; in fact there is no ion bombardment. The results obtained from this technique are similar to those obtained from plasma hydrogenation.

Apart from the above methods for hydrogen incorporation, there are also several other processing method during which hydrogen is incorporated.

### [3.6.4] Dry Etching

Some of the commonly used dry etchants contain hydrogen. Their chemistry is based on methane or ethane and hydrogen etc. The plasma generated during dry etching can cause hydrogenation on the semiconductor samples.

Hydrogenation may also occur when  $H_2$  is not an intentional component of the plasma source gases because of the presence of water vapour, small leaks, out gassing of internal surfaces of the reactor or erosion of photo resist etch masks [163].

### [3.6.5] Wet Etching & Water Boiling

Hydrogen is one of the most abundant elements in the acids and solvents used for wet chemical cleaning or etching. It is also seen that hydrogen can be incorporated while boiling the semiconductor in water. A measurable amount of hydrogen gets incorporated while boiled in water if the boiling is done in dark. This is due to the minority carrier induced reactivation of passivated dopants [161]. Amount of hydrogen incorporated also depends on the time scale of etching or boiling the water. The amount incorporated in III-V and II-VI semiconductors is considerably less when compared to Si samples.

### [3.6.6] Chemical Vapour Deposition

Virtually any chemical vapour step involves hydrogen. For example,  $\text{SiO}_2$  is deposited from  $\text{SiH}_4$  and  $\text{O}_2$ . Therefore, Chemical Vapour Deposition also incorporates hydrogen into the material bringing in passivation related effects.

Since, hydrogen is unavoidable during semiconductor processing; unintentional mode of hydrogen incorporation can passivate the sample. Under this situation, it is the priority of the design engineer to determine the amount of passivation happening to the semiconductor.

## [3.7] Basic Principle Governing Hydrogen Passivation

A variety of computational and experimental techniques are used to explain the role of hydrogen in semiconductors. Computational techniques based on density functional theory in the local-density approximation [164] have given some systematic understanding about hydrogen in a semiconductor. The experimental techniques include both electrical and optical characterization. The electrical characterization includes current-voltage measurement, deep level transient spectroscopy (DLTS) etc. A wide variety of optical spectroscopy like Photoluminescence (PL), Fourier Transform Infrared Spectroscopy (FTIR), Raman spectroscopy, etc could be employed.

The isolated interstitial hydrogen in a semiconductor has different charge states. It can exist in positive, neutral or negative charge state. The positive charge state of hydrogen is basically a proton. This is electrostatically attracted to regions of high charge density. *For example*, in covalent semiconductors, this charge density is highest at the bond centre. In semiconductors like GaN where they are more ionic, the regions of high charge density are more spherical around the anion i.e. in an anti-bonding (AB) site behind a nitrogen atom. The hydrogen is in a negative state when its 1s shell is filled. This reduces the tendency of hydrogen to interact with host atoms, thus occupying a tetrahedral interstitial ( $T_d$ ) site. In compound semiconductors, the preferred location is the tetrahedral interstitial site surrounded by cations [165].

The interaction or the bond formation between hydrogen and the host atoms are basically due to some disruption present in the perfect crystal. These disruptions can be on the surface, on the interface, or near a point defect in the bulk. The formation of such strong bonds between hydrogen and the host atoms is considered as the implication of passivation of the dangling bonds. The dangling bonds can either be present in the deep level or in the shallow level defects. It is often assumed that the intrinsic deep levels are all due to dangling bonds [165]. Point or extended type lattice defects or metallic impurities seen in a

semiconductor reduces the efficiency of the device. These deep levels have a strong influence on the minority carrier lifetime in the material and a direct effect on the breakdown voltage of Schottky diodes and of p-n junctions. Atomic hydrogen could effectively neutralize the effect of minority carrier lifetime killers, i.e. hydrogen can passivate the deep levels present. It can react with certain point defects or impurities in crystalline Si, GaAs, GaP, AlGaAs, CdTe, HgCdTe, Zn<sub>3</sub>P<sub>2</sub> or Ge, thus passivating their electrical activity. In short, atomic hydrogen can reduce some of the troublesome recombination centres in devices that affect the efficiencies, leading to improved yields and reliability of these devices. A number of process-related defects are passivated by reaction with atomic hydrogen. As discussed earlier, some of the examples of processing steps in which electrically active defects may be introduced include Reactive Ion Etching (RIE), sputter etching, laser annealing, ion implantation, thermal quenching and any form of irradiation with photons or particles with energies above the threshold value for atomic displacement. As the name implies, hydrogen passivation is a reaction between the hydrogen and the defects and impurities leading to a state in which the neutralization of impurities takes place. Neutralization of impurities can include simple ion pairing with acceptors ( $A^-H^+$ ) in p-type material or passivation of unsatisfied bonds. In the case of passivation of unsatisfied bonds the presence of nearby hydrogen species may change the nature of the electrical activity [166,167]. Passivation implies that the H interacts with the level in the bandgap, rendering it inactive and can include the formation of a stable impurity- or "host-H" bond or a rearrangement of the defect structure. These reactions are typical of hydrogen with donor type levels and imply that hydrogen may be in a *neutral charge state* in these cases, although it is also possible to have ion pairing-type associates of negatively charged hydrogen with a positively charge donor ( $H^-D^+$ ). In certain cases it is more correct to describe the effect of hydrogen on acceptor defects as neutralization or compensation, and again imply that hydrogen is in a positive charge state under these conditions. More work is to be done to understand this passivation mechanism for deep levels [168].

After hydrogen passivation, the dangling bond gives rise to a state in the bandgap. The subsequent attachment of hydrogen to the dangling bond forms bonding and anti-bonding states, the bonding states being in the valence band and the unoccupied anti-bonding states being in the conduction band becomes electrically inactive. The architecture of restructured bonds in a hydrogen passivated deep level is yet to be understood [160].

The passivation of shallow impurities in a variety of semiconductors is well understood and it has been concluded that it is generally undesirable to have shallow impurity passivation. Shallow level passivation is an example of chemically induced reconstruction of bonds by hydrogen; this means that a dangling bond is created chemically by the hydrogen. Such passivation eliminates the intended electrical activity of the dopants and therefore strongly affects device behaviour. Shallow impurity passivation can be readily understood on the basis of the properties of isolated interstitial hydrogen. In p-type material,  $H^+$  is the preferred charge state.  $H^+$  will diffuse towards electrically active, negatively charged



acceptors.  $H^+$  is attracted to these acceptors through Coulomb force. This forms H complex which is electrically inactive. H is now located in a preferred position in p-type material. This means that, bond centre (BC) is the preferred position for more covalent materials and anti-bonding (AB) centre behind an anion is the preferred position of ionic materials like GaN. In an n-type semiconductor,  $H^-$  will seek out positively charged donors, and assume an anti-bonding position in the complex [165]. This phenomenon occurs for both acceptors and donors in Si, GaAs, GaP and AlGaAs and has been observed for acceptors in Ge, CdTe, ZnTe and InP [169]. Since hydrogen is "omnipresent" during growth and processing of semiconductor devices, its effect on shallow impurities need to be carefully scrutinized. In Si, annealing the material at temperatures above 150 degree can readily eliminate hydrogen passivated shallow acceptors and donors. Upon annealing, the dangling bonds dissociate and form dopant-hydrogen complexes and neutralization of the hydrogen. The annealing temperature varies in different semiconductors.

Apart from interaction between hydrogen and the host atoms, hydrogen can also have a hydrogen-hydrogen interaction in a semiconductor. Though there are several theoretical predictions on its existence, direct experimental observation is limited. Experimental observation is difficult because of the dipole moment of  $H_2$ . This makes it difficult to observe the dipole with infrared spectroscopy. Raman spectroscopy has also been employed to learn this problem [169,170]. It gave only a limited success. The computational studies show that incorporation of  $H_2$  in an interstitial position decreases the binding energy and the vibrational frequency and increases the bond length. The decrease in binding energy and corresponding decrease in the vibrational frequency is related to the charge density near the interstitial site.

It has also been found that hydrogen and deuterium gives different device performance upon passivation [171,172]. A comparative study was done on the Si/SiO<sub>2</sub> interface of MOS transistors. Those incorporated with deuterium were found to have increased lifetime compared to those with hydrogen-incorporated interface [173]. This indicates that Si-D is more resistant to hot-electron excitation than the Si-H bond. These results are surprising because H and D are entirely equivalent from an electronic point of view. It should be noted that the static electronic structure of the Si-H and Si-D bonds is identical. The difference must therefore be attributed to the dynamics [174].

### [3.8] Heterostructures Used For This Study

We have carried out experiments on several semiconductors, belonging to group II-VI, III-V and IV semiconductors. This includes epilayers and low dimensional systems. The description about the materials presented here are for those papers that are attached along this thesis.

### [3.8.1] II-VI Materials:-CdZnTe Quantum Well and ZnSeTe Epilayer

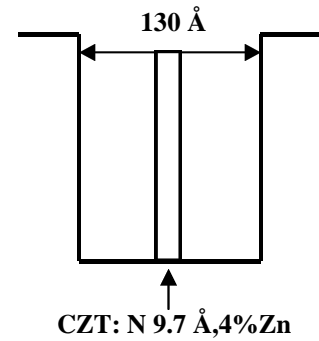
The interest in wide band gap II-VI semiconductors can be attributed to the progress in visible light emitters, particularly blue-green light emitting devices [175,176], and other applications like solar cells [177,178]. Most of the II-VI compounds crystallize in zincblende or Wurtzite-type structures. They have a direct bandgap and allow band-to-band-transition that makes them useful for photonic devices. They have high ionicity and high melting points. Because of large ionicity, their thermal conductivity is small. They are difficult to grow by the traditional pulling method because of their thermal conductivity. Large number of stacking faults and point defects are also seen in those II-VI samples. Also, dislocations are easily created in these samples [179]. Due to the success in epitaxial growth in recent years, there has been a major interest in these materials.

Among the II-VI family, telluride (Te) (for example, CdTe) and selenium (Se) (for example ZnSe) based structures are the most technologically important materials because of their device applications. Te alloys like CdHgTe are used for the fabrication of focal plane arrays and selenium (Se) alloys are now being exploited for visible laser applications [180]. Recently, CdZnTe alloys have become the centre of attraction because of their high crystalline quality. This is attributed to the Zn present in the alloy. The best quality  $\text{Cd}_{1-x}\text{Zn}_x\text{Te}$  crystals are obtained when the Zn concentration is kept below 20% (i.e.  $x < 20\%$ ) [181]. Indium [182] and nitrogen [183] are seen as the n and p-type dopants in II-VI semiconductor materials. The n-type dopants that have been tried on II-VI semiconductors are chlorine [184], iodine [185], bromine [186], and aluminium [187]. Though N had been proposed as an ideal p-type shallow acceptors in ZnSe [188,189], it is only until recently that a control of the doping level and the localization of doping atoms has been achieved in other II-VI materials like CdTe and CdZnTe [183,190]. Due to the importance of acceptor doping in II-VI materials, we have selected delta doped CdZnTe samples for our studies. More details on the samples are given in the next subsection.

$\text{ZnSe}_{1-x}\text{Te}_x$  epitaxial layers were chosen for our study due to their fundamental and technological importance. These materials are seen as a good contact layer for ZnSe based blue-green laser diodes. By using  $\text{ZnSe}_{1-x}\text{Te}_x$  with varied concentration of Te, one can obtain n-type and p-type contact layers, i.e., when the Te concentration is less than 0.4%, it can be doped into an n-type material and when the concentration is above 0.6%, it can be made as a p-type material. The reason is n-type doping is possible with ease in ZnSe material and while p-type doping is possible for ZnTe. These materials are also interesting for fundamental studies. For example, When the Te concentration is less than 0.1% in  $\text{ZnSe}_{1-x}\text{Te}_x$ , a broad band luminescence is observed. Normally broad band luminescence is due to the impurities or defects in the material. Since Te is isoelectronic in nature, our aim was to passivate charge defects. We have also studied these materials for their thermal stability. For a detailed review on II-VI materials refer [110,191].

#### [3.8.1.1] $\text{CdZn}_{1-x}\text{Te}_x$ Quantum Well

The  $\text{CdZn}_{1-x}\text{Te}_x$  single quantum well structure used for hydrogen passivation studies is as given below. The sample was grown on (001) CZT with 12% Zn in an MBE system. The barrier region was 1000 Å thick CZT with 14% Zn concentration. The well region was 130 Å thick CZT with 4% Zn concentration. Nitrogen was doped in the centre of the well with an approximate thickness of 9.7 Å. The nitrogen doping level was of the order of  $5 \times 10^{17}/\text{cm}^3$ .



**Fig. 3.6:-** CdZnTe QW structure

Another set of similar structures but with different Zn concentration was used for thermal annealing studies.

#### [3.8.1.2] $\text{ZnSe}_{1-x}\text{Te}_x$ Epilayers

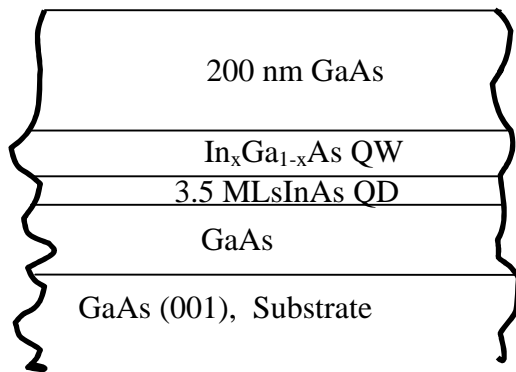
The  $\text{ZnSe}_{1-x}\text{Te}_x$  ( $x < 0.1\%$ ) epilayers were grown on GaAs (001) substrate using an EPI 620 model molecular beam epitaxial (MBE) system. EPI 40 cc low temperature cells were used for evaporation of the elemental solid sources: Zn, Se and Te. The cell temperatures of Zn were fixed at 300 °C, while, the cell temperatures of Se and Te ranged from 178 °C to 162 °C and from 230 °C to 310 °C, respectively. Samples were grown on substrates with various temperatures ranging from 280-340 °C. The growth rate was about 0.3-0.4 micrometer/hour ( $\mu\text{m}/\text{h}$ ). During the growth, reflected high energy electron diffraction (RHEED) was used to monitor the process of epitaxial growth. The Te concentration was determined by an energy dispersive x-ray (EDX) measurement with a detectivity of about 0.1%.

#### [3.8.2] III-V Materials: - InAs Quantum Dot

GaAs is the most researched III-V material. Its direct band gap property makes it the ideal candidate for making optical lasers and the higher mobility and saturation drift velocity makes it the material for making high frequency devices. Since Goldshmidt [192], found this material in 1920, numerous numbers of fundamental and technical papers have been published. Some other potentially important III-V compound semiconductor materials are InP, GaN, AlN.

Quantum dots made of III-V compounds like InAs/GaAs and InGaAs/AlGaAs material combinations seem to be the most promising candidate for immediate application in optoelectronics. The quantum dots made of these materials can do lasing in the optical range of 1.3 and 1.55 microns which are the key wavelengths for fibre optic communication

networks. The quantum dots made on ternary substrates like AlGaAs can replace InP substrates that are presently at use in communication networks. Experimental results show that the shape and size of InAs dots strongly depend upon process conditions such as the substrate temperature, growth rate, capping layer and nominal InAs thickness [193, 194, 195]. Since the confined energies of electrons and holes in dots are determined by the shape, size and strain distribution, the emitting wavelength from InAs dots can be tuned by changing the growth and post processing conditions. In order to fabricate the InAs dots lasers at the emission wavelength of 1.3  $\mu\text{m}$ , it is not only needed to know what influences the emission wavelength, but it is also important to obtain high efficiency of the radiative recombination from InAs QDs. A high efficiency of radiative recombination leads to a high optical gain. In this thesis, the paper on InAs QDs (Paper VI) show how the non radiative recombination centres can be efficiently passivated to obtain high optical gain.



**Fig. 3.7:-** The cross-sectional view of InAs QD structure.

a cap layer of approximately 200 nm GaAs was grown, and for some an  $\text{In}_x\text{Ga}_{1-x}\text{As}$  quantum well layer was first grown prior to the 200 nm GaAs cap layer. The important difference between all the samples is in their  $\text{In}_x\text{Ga}_{1-x}\text{As}$  layer. A schematic cross-sectional view of the samples is given in the Figure 3.7.

The samples for these studies are grown using an EPI930 solid source molecular beam epitaxy (SSMBE) system. The substrates for the growth of QDs were semi-insulating (001) GaAs. The substrate temperature was maintained at 510  $^\circ\text{C}$  during the growth of InAs layer. A buffer layer of GaAs of approximately 50 nm was grown prior to the growth of 3.5 monolayer (ML) growth of InAs layer. After every 0.1 ML of InAs growth, a growth interruption for 2 seconds was allowed under a continuous flow of As. For some samples,

### [3.9] Sample Preparation

Thermal processing of all our heterostructure samples was done on a commercially available 3-zone furnace. The temperature fluctuation of the annealing chambers can be of the order of  $\pm 2$   $^\circ\text{C}$ .

For the passivation studies, either hydrogen or deuterium was used. Deuterium is a non-radioactive isotope of hydrogen. Incorporation of hydrogen or deuterium was done by two methods depending on the sample used for the passivation studies.

1. One of the methods was to anneal the samples in hydrogen/deuterium atmosphere. The samples were first inserted in quartz ampoules with 0.8 atm  $\text{H}_2/\text{D}_2$ . They were

then annealed at various temperatures in the commercially available furnace that is used for semiconductor processing. The temperature fluctuation of the annealing chambers can be of the order of  $\pm 2$  °C. The highest temperature of annealing was always kept below the growth temperature of the sample.

2. Plasma passivation of InAs quantum dot samples were done using dc plasma technique. The samples were mounted on a heater block which can control the sample temperature  $T_s$  with an accuracy of 2 °C, and placed 10 cm downstream from the plasma with a bias voltage of 300 V. Both the pressure of the plasma and the bias voltage were kept constant. The substrate temperature and duration time and duration of plasma exposure was varied.

# 4

## Characterization: Tools & Technology

To obtain a semiconductor device with desirable performance, semiconductor growth and process techniques must be optimized. This is done by involving various physical, optical and electrical spectroscopic characterization facilities. This chapter gives an introduction about various characterization tools used for accomplishing this work. It begins with an introduction on electrical characterization, followed by optical characterization and then structural characterization.

### [4.1] Electrical Characterization

Current-Voltage (I-V) and Capacitance-Voltage (C-V) measurement techniques are the most effective characterization tools to give a wealth of information for an MOS device. These techniques can also be extended with time dependent studies to obtain reliability of a device. For example, time dependent dielectric breakdown (TDDB), charge to breakdown (QBD) and stress induced leakage current (SILC) can be studied to get information on the carrier generation life time, recombination life time etc. But in the ultrathin oxide regime, both the measurements and the analysis of these techniques become complicated and sometimes ineffective. For example, due to the large tunnelling current quasistatic C-V measurement technique, deep level transient spectroscopy (DLTS) etc. can not be used. This current leakage problem can be solved by doing the C-V measurements at high frequencies. In this thesis, we have employed current-voltage (I-V) and high frequency capacitance-voltage (C-V) technique to characterize the MOS system in the low temperature regimes. The measurements were done for temperatures ranging from 50 K to 300 K. The details regarding these techniques are given in the following subsections.

As the gate oxide thickness is reduced, various quantum mechanical effects take place both in the gate and the channel region. Some of these effects are described below.

### [4.1.1] Leakage Current Transport Mechanism

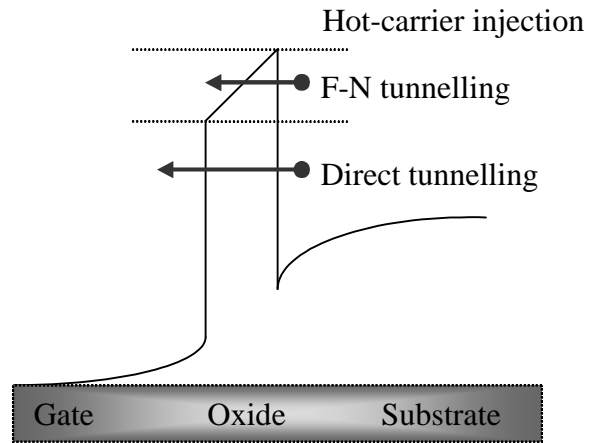
If a gate current can be measured while applying a gate bias (positive or negative), it is due to the tunnelling mechanism. Tunnelling current becomes higher as the oxides get thinner. There are basically three kinds of leakage current transport mechanisms. These are Fowler-Nordheim (F-N) tunnelling, hot carrier injection, and direct quantum mechanical tunnelling. These three primary mechanisms for gate leakage can be illustrated as shown in the Figure 4.1.1.

#### [4.1.1.1] Fowler-Nordheim Tunnelling

When the electrons tunnel to the conduction band in the SiO<sub>2</sub>, it is called as Fowler-Nordheim (F-N) tunnelling. This mechanism takes place when the oxide is sufficiently thicker i.e. of the order of ~5 nm. For a simple case (i.e., when ignoring the effects of finite temperature and image-force barrier lowering), the tunnelling current density can be written as [196,197],

$$(4.1) \quad J_{FN} = \frac{q^3 E_{ox}^2}{16\pi^2 \hbar f_{ox}} \exp\left(-\frac{4\sqrt{2m^*} f_{ox}^{3/2}}{3\hbar q E_{ox}}\right)$$

where  $q$  is the charge of an electron,  $m$  is the effective mass of an electron in the SiO<sub>2</sub> ( $m^*=0.42 m_0$ ),  $f_{ox}$  is the barrier height between Silicon and silicon dioxide and  $E_{ox}$  is the electric field in the oxide. From this equation, it is estimated that F-N tunnelling current is a straight line when  $\log(J/E_{ox}^2)$  versus  $1/E_{ox}$  is plotted. This equation also states that for a normal device operation, F-N tunnelling current is negligible.



**Fig. 4.1.1:** Different Transport Mechanisms

#### [4.1.1.2] Hot Carrier Injection

Hot carrier injection normally takes place when the device is under deep depletion [2]. This happens when carriers from the silicon acquire sufficient energy (due to high electric field) to reach the SiO<sub>2</sub> region. This mechanism is more probable for electrons than holes and the reason is due to their comparatively less effective mass. Also, the Si-SiO<sub>2</sub> interface energy barrier for an electron is approximately 3.1 eV while for a hole it is 4.6 eV. Monitoring this mechanism is of importance as it influences the reliability of the device to a greater extent. This is because hot carrier injection generally creates large number of interface states and

these increases with applied field and temperature. Since this is a complicated process, modelling of hot carrier density involves Monte Carlo simulations.

#### [4.1.1.3] Direct Tunnelling

When the electrons tunnel through the entire silicondioxide layer it is called as direct tunnelling. By definition, direct tunnelling can be defined as the elastic, quantum mechanical tunnelling of low energy carriers directly through the gate oxide potential barrier. The probability that a carrier with an energy  $E$  can tunnel through an oxide barrier is described by the tunnelling coefficient,  $TC(E)$ . The tunnelling coefficient is strongly dependent on the mass of the carrier in the three device regions; substrate, oxide and gate. The  $TC$  is also strongly dependent upon the thickness of the barrier, the height of the barrier and the energy of the incident carrier. Upon temperature, the tunnelling current has only a weak dependence. Direct tunnelling is dominant over other tunnelling mechanisms even at moderate gate bias for an oxide thickness below 40 Å. Indeed the tunnelling current increases exponentially with decrease in oxide thickness [198].

#### [4.1.2] Poly-Silicon Gate Depletion & Boron Penetration

When a gate voltage is applied to the gate electrodes made of poly-silicon (e.g. charge coupled devices are made of poly-silicon as the gate electrode), a depletion layer “ $x_{poly}$ ” is formed. Poly gate depletion effect is mainly due to the insufficient activation of the dopants. Due to this problem the resistance of the polysilicon region increases. This results in a voltage drop. This voltage drop “ $V_{poly}$ ” results in reducing the effective gate voltage while simultaneously increasing the effective electrical thickness of the oxide. A simplified equation to estimate the voltage drop “ $V_{poly}$ ” is written as [199]

$$V_{poly} = \frac{e^2 \epsilon_{ox} E_{ox}^2}{2q e_{Si} N_{poly}} \quad (4.2)$$

where  $\epsilon_{ox}$  is the dielectric constant of  $SiO_2$ ,  $\epsilon_{Si}$  is the dielectric constant of silicon and  $N_{poly}$  is the doping concentration in the poly silicon. Poly depletion results in the degradation of inversion gate capacitance and effectively decreases the transconductance through the channel [200,201]

From the above equation, it is clear that to decrease the poly depletion; the poly gate doping must be increased. This can be increased either by increasing the dopant concentration through “insitu” doping or by increasing the implantation dose and then by annealing them at a suitable higher temperature. Higher doping concentration or larger thermal budgets invariably creates another problem called dopant penetration in ultrathin oxides. Dopant



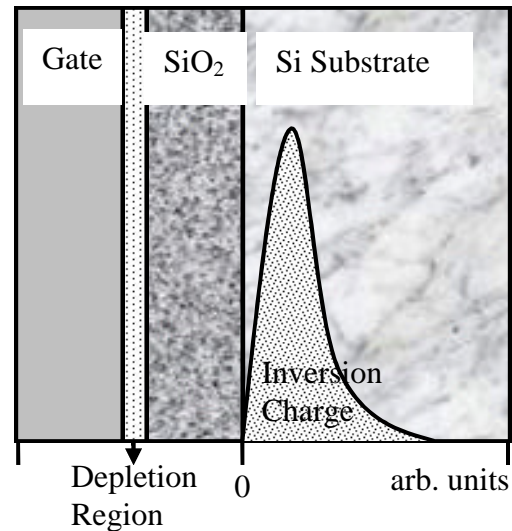
penetration results in charge trapping centres and defects regions in the Si/SiO<sub>2</sub> interface. This invariably can also cause fluctuation in the threshold voltage.

Some of the relevant proposals to reduce the gate depletion and boron penetration could be to use novel gate dielectric and alternate gate electrodes. Oxynitrides, especially by direct nitrogen implantation and small concentration of Ge into the polysilicon has also been proposed to decrease these effects and has been studied in this thesis.

Quantum mechanical investigation is necessary to precisely model the effects such as (i) polysilicon depletion (ii) scattering mechanism (iii) defects, on the transconductance in the channel region of a CMOS device [202,203,204].

### [4.1.3] Oxide Thickness

In the ultrathin oxide regime, the quantum effects give various definitions for oxide thickness like physical thickness and electrical thickness. The physical oxide thickness can be measured by Ellipsometry, Transmission Electron Microscopy (TEM) etc, or can be extracted from the CV data using quantum mechanical simulations. The electrical thickness of the oxide is the sum of the physical thickness, the thickness of the depletion region at the poly silicon and the thickness of the charge layer at the inversion region. As the thickness of the oxide regime is reduced, these definitions on the oxide thickness become more significant to consider. We have extracted our oxide thickness from the accumulation region of the capacitance curve. But, the industry standard for the oxide thickness in the ultrathin regime is to derive them from the inversion capacitance. An analytical solution relating the oxide thickness and various other parameters derived from accumulation region, inversion region etc can be found in [205]. The physical oxide thickness is used during the processing of the device to monitor the inline production and the DC effective thickness is used in BSIM compact model for CMOS circuit simulation. The schematic description of the depletion region and the inversion region of MOS device is given in figure 4.1.2.



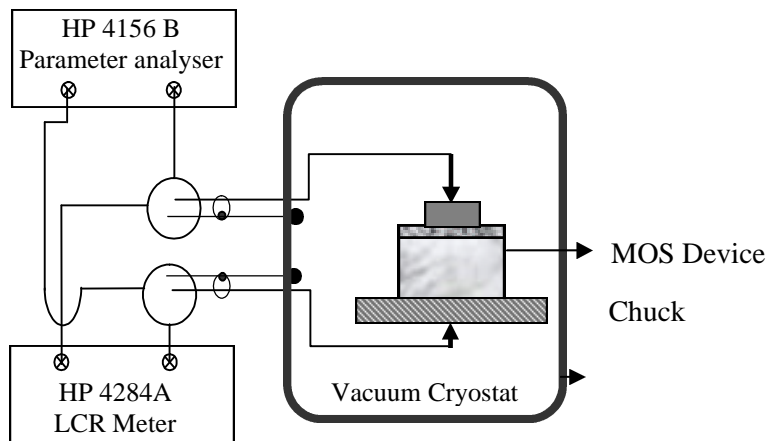
**Fig. 4.1.2:** Schematic description of depletion and inversion charge region

#### [4.1.4] Current-Voltage Measurements

Figure 4.1.3 gives the schematic diagram of the electrical measurement system. The devices were connected with a probe on the front pad and a chuck was used to connect the backside of the chip.

I-V measurements were done using an HP4156 B precision semiconductor parameter analyzer. The basic information we have derived from the current-voltage measurement is the amount of tunnelling leakage current. I-V characteristics were done for a temperature range of 300 to 50 K. Fractional change in the leakage current with respect to the temperature was observed in our measurements. The scanning was done from the negative bias to the positive biasing range. A maximum biasing voltage of -3 to + 3 V was applied. Beyond this voltage regime, the device was unstable and succumbed to breakdown.

#### [4.1.5] Capacitance-Voltage Measurements



**Fig. 4.1.3:** Schematic Diagram for the Electrical Measurement Setup.

High frequency C-V measurements were carried out using HP 4284 A precision LCR meter as shown in figure 4.1.3.

The high frequency CV method was introduced by Terman [206]. At high frequency, it is the capacitive current that is dominant over the tunnelling current and therefore the interface charge and inversion charge can

respond to small signals. This means that, the frequency of the ac signal is superimposed on the dc bias and this is sufficiently high to suppress the surface states such that they don't follow the ac test signal. However, they still contribute when the surface states are varied by changing the applied bias voltage. But at high frequencies, the series resistance becomes dominant because of the low impedance of the capacitor. This can be accounted for by correlating the measurements of both series and parallel mode setup. By series and parallel mode, it means that the meter assumes the device under test to consist of a either a parallel connection or a series connection with a resistor. Also, it is necessary to correlate the C-V measurements done at various frequencies to obtain the true capacitance. We have carried out measurements in both series and parallel mode and at various frequencies ranging from 10

kilohertz (KHz) to 1 megahertz (MHz). Only those measurements that correlated in both series and parallel mode and also at various frequencies were chosen for parameter extraction.

The capacitance of an MOS device is dependent upon the oxide thickness, silicon doping concentration and the trapping properties of the system. A typical high frequency C-V curve has three regions to specify; the region of accumulation, depletion and inversion. Some of the device parameters that are extracted from the C-V curve are the oxide thickness, substrate doping concentration, flatband capacitance and flatband voltage, threshold voltage, work function, effective and total bulk oxide charge. The above parameters can qualitatively give information that can optimize the processing parameters for the critical performance of the device. A detailed description on the C-V curves and how various parameters can be extracted is given in “Nicollian and Brews” and “S. M. Sze” [1,2]. We have performed a temperature dependent study for a temperature range of 50 K to 300 K.

In the ultrathin oxide regime, a quantum mechanical evaluation is necessary to completely involve the entire phenomenon to accurately measure the capacitance curves. This is because, for very ultrathin oxides, tunnelling current influences the accumulation and inversion capacitances. For example, it can be deep depletion that is being measured and not inversion as ultrathin oxides can not completely invert the device and for the region of accumulation, it is difficult for the device to completely accumulate and therefore when deriving the oxide thickness from the accumulation, a quantum mechanical correction for tunnelling mechanism must be added to derive the exact thickness without error.

The flat band capacitance ( $C'_{FB}$ ) can be obtained from the formula

$$C'_{FB} = \frac{\epsilon_{ox}}{t_{ox} + \frac{\epsilon_{ox}}{\epsilon_{si}} \sqrt{\frac{K_B T}{e} \left( \frac{\epsilon_{si}}{e N_D} \right)}} \quad (4.3)$$

where  $\epsilon_{ox}$  and  $\epsilon_{si}$  are oxide and silicon dielectric constant,  $t_{ox}$  is the oxide thickness,  $e$  is the electron charge,  $K_B$  is the Boltzmann constant and  $T$  is the temperature at which the device is measured. The substrate doping concentration ( $N_D$ ) is obtained from

$$\frac{d \frac{1}{C^2}}{dV_g} = \left[ \frac{1}{2} q \epsilon_s A^2 N_D \right]^{-1} \quad (4.4)$$

Here  $\frac{d \frac{1}{C^2}}{dV_g}$  is the slope obtained by plotting gate voltage ( $V_g$ ) in the deep depletion capacitance region. The corresponding voltage for the flat band capacitance ( $C'_{FB}$ ) is the flat band voltage ( $V_{FB}$ ).

#### [4.1.6] Notes for C-V Measurements

A successful measurement can only be done with a lot of patience and observations. One of the major problems while doing measurement is the stray capacitance. The valid capacitance value is that when it is at equilibrium conditions (please read the next paragraph for equilibrium condition). The measurement signal also needs to be applied in a sequence. All the measurements that are performed and reported in this thesis were carried out from inversion to accumulation. That is, all our measurements were done from negative to positive voltages. The C-V measurements were initially carried out in a probe station and then transferred to a probe centre in a cryostat. Signals to the test structure are routed between the C-V analyzer and interconnecting cables. The cables provide stray capacitance to the measurements. This is compensated by cable compensation and using an offset cancellation function in the analyzer. Thus, one can prepare the system for the key measurements. This is actually done by calibration capacitors present in the system. About measurements done at equilibrium condition, this is probably most neglected.

An equilibrium condition is when the MOS capacitor is fully charged. Since the MOS takes time to get fully charged after the voltage is applied, it is adequate to wait a bit before the measurement is recorded. Similarly, after each measurement, it is necessary to take a time step before the next measurement is recorded. Also, since the CV curve measured from inversion to accumulation and accumulation to inversion would look different, it is necessary to make a few recording in both directions before taking the final measurement or a delay time should be set in the meter. Also, it is better to take the final measurement from inversion to accumulation since this would give the device to be in equilibrium condition. Another problem with the MOS device is the series resistance. The series resistance can come from either the substrate or the back side of the wafer. If there is any oxide in the backside, stray resistance can definitely arise and distort the CV curve. This is important for a high frequency CV curve because the curve depends on amplitude change and phase shift. Some times, this can be eliminated by using the series and parallel mode measurement that is an option in the LCR meter. Otherwise, one need to do some calculations based on Nicollian and Brews; page 224 [1]. In the measurements done for the satisfaction of this thesis, it is made sure that the series resistance was eliminated.

#### [4.1.7] Low Temperature Measurements

For low temperature measurement, we used a helium cryostat and a temperature regulator from Leybold to measure from 50 K to 300 K. Temperature scanning was always done from high temperature to low temperature. One point to note here is that the low temperature measurements are really painstaking as it requires a lot of time and patience.

## [4.2] Optical Characterization

### [4.2.1] Photoluminescence (PL)

We have employed Photoluminescence (PL) for studying the incorporation of hydrogen in low dimensional semiconductor heterostructures.

Photoluminescence is a wide, sensitive and efficient method to characterize semiconductors. This is a non-destructive spectroscopy and analyses both the intrinsic and extrinsic properties of semiconductors. It is a fundamental optical characterization tool because of its simplicity in doing the experiment. Practically, no sample preparation is required to obtain the results. PL provides information on both minority and majority (information on the majority carrier depends on the amount of doping in the semiconductor) carrier properties. The lifetime, the diffusion length, the quantum efficiency etc. can be inferred through the study of the recombination paths. It can detect semiconductor parameters like effective mass and bandgap [207]. It is very sensitive to the chemical nature of impurities and defect centres and can be detected even at a very low concentration, that is, qualitative information can be obtained [208,209,210]. This technique has also been employed to study complex defects in semiconductors. Apart from the fundamental semiconductor characterization, PL is also used to study device characteristics in heterostructures, Si-MOS structures etc [211,212,213].

In principle PL is an emission spectroscopy. Three processes can be distinguished in photoluminescence:

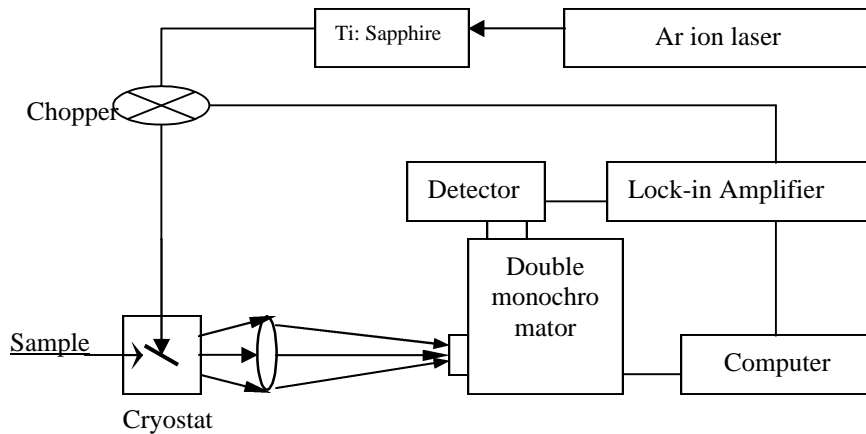
- (i) Creation of electron hole pairs by absorption of the exciting light.
- (ii) Radiative recombination of electron hole pairs.
- (iii) Escape of the recombination radiation from the sample.

Thus, photoluminescence is the optical radiation emitted by a physical system resulting from excitation to a non-equilibrium state by light irradiation. So, the excitation is the creation of a non-equilibrium state. The sample then returns to an equilibrium state and during this process carrier recombination takes place both radiatively and non-radiatively. In PL measurements, it is the light that is emitted from the sample which is examined. For a more complete understanding of the system it is useful to analyze certain recombination mechanism. Various recombination processes are explained in the next section under the sub title "Recombination processes".

### [4.2.2] Photoluminescence Measurements:-Principles

From the above discussion, it is clear that PL is a time-dependent perturbation problem of an electromagnetic wave impinging on an electron (matter). The quantum mechanical description is derived through the Quantum mechanical Hamiltonian operator  $H$  where  $H=H_0 + H(t)$  where  $H_0$  and  $H(t)$  are the non-perturbative and the time dependent perturbative terms respectively. The Hamiltonian  $H$  describes the interactions between matter and the electromagnetic field. By solving the eigenstates  $|\mathbf{y}\rangle$  and eigenvalues  $|E\rangle$  of this Hamiltonian, (i.e.,  $H|\mathbf{y}\rangle = E|\mathbf{y}\rangle$ ), we can derive terms for absorption and emission process. Almost all quantum mechanics textbooks treat this problem. Much before the quantum mechanical solution came, Einstein treated this as a classical problem and derived expressions for absorption and emission (both spontaneous and stimulated) processes.

### [4.2.3] Experimental Setup for PL



**Fig. 4.2:** The schematic description for the PL experimental setup.

An excitation source, a cryostat, a monochromator and a detector make up the basic building block of a PL setup. The excitation source in our case is an  $\text{Ar}^+$  gas laser. The laser excites the sample with energy above the bandgap energy of the semiconductor such that this creates an electron hole pair. A tuneable Titanium-Sapphire laser was also used for resonant excitation below the bandgap energy. The resonant excitation below the band gap energy is called selective photoluminescence (SPL). The samples were mounted in a liquid helium cryostat. The sample temperature was varied from 4.2 K to 77 K. Higher temperature could be reached by heating the copper block on which the samples were mounted. The PL spectrum from the sample was dispersed with a spex double grating monochromator. The signal was amplified in ac mode at the chopping frequency with a lock-in amplifier. The PL signal from the monochromator was detected with liquid nitrogen cooled Ge photodetector and photomultiplier. The schematic description for the PL experimental setup is given in Figure 4.2.

#### [4.2.4] Photoluminescence Excitation Spectroscopy (PLE)

In this spectroscopy, the monochromator is kept at particular observed emission energy from the sample. The intensity of the emission is then recorded as a function of the excitation photon energy. By exciting at energies higher than the detected transition energy, the involved particles will relax back to the ground state of the transition before recombining. This relaxation process is more efficient from an excited state, which is the principle mechanism for PLE spectra and the essential distinction from standard absorption measurements.

#### [4.2.5] Radiative Recombination Process

The recombination mechanism takes place both radiatively as well as non-radiatively [214]. In this thesis, the radiative recombination process is examined. Different non-radiative recombination processes are discussed in reference [215]. The radiative recombination mechanism can be either due to intrinsic process or due to extrinsic process. The former is crystal related. Band-to-band transitions, free excitons, electron-hole droplets etc are the examples of intrinsic process. The latter is divided into localized and unlocalized. In the unlocalized type, the electrons and holes of the host lattice, i.e., free electrons in the conduction band and free holes in the valence band, participate in the luminescence process. In the localized type the luminescence excitation and emission processes are confined in a localized luminescence centre [216]. Luminescence caused by intentionally incorporated impurities or defects is classified as extrinsic luminescence as opposed to intrinsic luminescence. Most of the observed types of luminescence that have practical applications belong to this category. Extrinsic recombination mechanism involves free-to-bound transition, donor-to-acceptor pair transitions, bound excitons etc. A brief description of some of these mechanisms is given below.

##### [4.2.5.1] Band-to-Band Transitions

Band to band transitions involve the recombination of free electrons and free holes across the bandgap, i.e., it is the recombination between an electron in the conduction band (CB) and a hole in the valence band (VB). Band-to-band transition is more probable in direct semiconductors, like GaAs than in indirect semiconductors like Si.

##### [4.2.5.2] Free Excitons

An exciton is an electron-hole system, coupled through a weak Coulomb force. Frenkel first introduced the concepts about these excitonic states in 1931 [217]. Since then it has been widely used to study optical properties of materials. Depending on the kind of material that is being analyzed; the excitons may be divided into Frenkel excitons and

Wannier-Mott excitons. Frenkel excitons are usually being observed in ionic crystals. Here, the electrons and holes are strongly attracted and these excitons are tightly bound. They are usually observed in a single atom. It is the Wannier-Mott excitons that are seen in semiconductors. These excitons are weakly bound. This is because in most semiconductors the Coulomb interaction is strongly screened by the valence electrons via the large dielectric constant [218,219,220,221]. The electron-hole wave functions of these excitons are seen to spread over a large number of atomic sites. The Wannier-Mott excitons have a high mobility and a small binding energy.

#### [4.2.5.3] Free-to-Bound Transitions

Transitions involving a free carrier (e.g. an electron or a hole) and a charge (e.g. a hole or an electron) bound to an impurity are known as free-to-bound transitions. These transitions are usually observed at low temperatures when the carriers are frozen on the impurities. Emission due to free-to-bound transitions is a simple way of measuring impurity binding energy. Free-to-bound transitions are more prominent when the deep impurities are present.

#### [4.2.5.4] Donor-Acceptor Pair Transitions (DAP Transition)

Consider a semiconductor containing both donors and acceptors. Under equilibrium conditions, the acceptors can capture some of the electrons from the donors. As a result, the sample contains both ionized donors ( $D^+$ ) and acceptors ( $A^-$ ). On optical excitation, (non-equilibrium condition) the electrons and holes which are produced can be trapped at the  $D^+$  and the  $A^-$  sites to produce neutral  $D^0$  and  $A^0$  centres. To attain the equilibrium condition, some of the electrons on the neutral donors recombine radiatively with holes on the neutral acceptors. This process is known as a donor-acceptor pair transition.

#### [4.2.5.5] Bound Excitons

At low temperatures, the semiconductor sample can have a small number of donors or acceptors in their neutral state. The excitons will then be attracted to these impurities via Van der Waals interaction. Since this attraction lowers the exciton energy, neutral impurities are very efficient at trapping excitons to form bound excitons. Thus the bound excitons can be divided into different classes depending on the nature of the impurity; e.g. excitons bound to acceptors, donors, or an isoelectronic impurity. The electronic and optical property of each exciton depends on where it is bound and then properties are very much different for isoelectronic impurity compared to donor and acceptor impurity bound excitons. The theoretical prediction of BE was given by Lampert in 1958 [219] and its experimental validity was given shortly [222,223]. The study of BE is a powerful tool to obtain information about the corresponding impurity. This is because the electronic structure of the BE is more governed by the impurity potential than the coulomb potential of the electrons and holes.



#### [4.2.6] Luminescence:-Low Dimensional System

The low dimensional systems in semiconductor include quantum well, quantum wire and quantum dots. These are of two- one- and zero-dimensions respectively. In low dimensional systems, electrons and holes are spatially confined causing quantum confinement. As a result energy-level structures and hence optical properties become essentially different from those in three-dimensional bulk systems [224,225]. The dependence of the well width is briefly described here. Let us consider a quantum well. The energy levels in a quantum well with infinite potential is given by,

$$E_n = \left( \frac{h^2}{8p^2 m_e} \right) \left( \frac{n\pi}{L} \right)^2 \quad (4.5)$$

Where  $n=1, 2, 3, \dots$  and where  $L$  is the thickness of the quantum well layers. The absorption corresponding to the band-to-band transition shifts to higher energies with decreasing  $L$ . Also, in one- and zero-dimensional systems, the absorption shows blue shifts as the characteristic size of the system representing the low dimensionality as  $L$  decreases.

Characteristics of excitons in low-dimensional systems are also substantially different from those in three-dimensional systems. The binding energy and oscillator strength are noticeably enhanced in low-dimensional systems because of the increase in the overlap of electron and hole wave functions. The enhancement becomes generally more significant with decreasing dimensionality. Thus, two kinds of quantum effects are seen in the transition energy of low-dimensional systems. The first is the effect of the quantization of the motion of electrons and holes causing blue shifts with decreasing the characteristic size of the system. The second is the enhancement of the exciton binding energy causing red shifts. In most cases the blue shifts exceed the red shifts, so that the net result is that the exciton absorption shows a blue shift with decreasing characteristic size.

In our quantum dot system, we have done PL and time dependent PL measurements. Our measurements give luminescence from an ensemble of quantum dots. In order to get luminescence from a single dot, micro-photoluminescence is commonly used. The results obtained from micro-PL gives a direct proof for the existence of quantum phenomena in low dimensions.

#### [4.3] Other Physical Characterization

1. High resolution X-Ray Diffraction: This was employed for a wide variety of structural characterization; including thermal stability, interface quality etc of CMOS and low dimensional semiconductor structures.

2. Transmission Electron Microscopy: This was exploited to analyze the oxide thickness, interface quality, strain etc of the MOS device described in this thesis.
3. Secondary Ion Mass Spectroscopy: This was used to study the nitridation and boron diffusion of MOS devices used for this thesis.

#### [4.3.1] High Resolution X-ray Diffraction (HR-XRD)

X-ray diffraction is a fundamental characterization technique in microelectronics to examine the structural features (for example, of semiconductors, electronic packages) with atomic scale resolutions by diffraction method. It is simple, non-destructive and requires no sample preparation. Also, the sample area needed for examining can be of the order of mm<sup>2</sup>.

The information of the sample is extracted by studying the intensity of the diffracted beam. The diffracted beam obeys the Braggs diffraction law. The basic assumptions for arriving at Bragg's law are scattering, reflection and interference. The assumption behind scattering could be seen as the interaction of electromagnetic beam with the charges (electrons) of the scatters. This interaction is known as coherent Thomson scattering, which means that the phase of the absorbed and the emitted radiation is a constant. As for scattering (theory), it is divided in to geometrical scattering theory and dynamical scattering theory. Geometrical scattering theory is described when the intensity of the primary beam is constant in the crystal and dynamical scattering theory is when the assumptions are taken for a journey through absorption, electron distribution etc [226,227].

According to Bragg's law, this scattering is assumed as a mechanical reflection of light beams on lattice planes and the reflection can only be measured in angles where the phase shift of two interfered waves is a multiple of the incident wavelength. With these three assumptions, we state the Braggs law as  $n\lambda = 2d_{hkl} \sin(\Theta_{hkl})$ , where n is an integral number (1, 2, 3...) describing the order of reflection. This is a fundamental relation between the wavelength of the X-ray ( $\lambda$ ), distance of the lattice planes ( $d_{hkl}$ ), and the angle of incidence of the beam ( $\Theta_{hkl}$ ).  $hkl$  are the Miller indices of a set of parallel planes [228].

The diffraction data obtained can be due to two kinds of reflections. These are symmetric and asymmetric reflections. A basic knowledge of crystal structure and  $hkl$  parameters is needed to understand these two reflections. Reflections with structure (001) are called symmetric reflections e.g. (004) where as ( $hhl$ ) reflections where ( $h,l$ ) are even or odd numbers, are asymmetrical reflections.

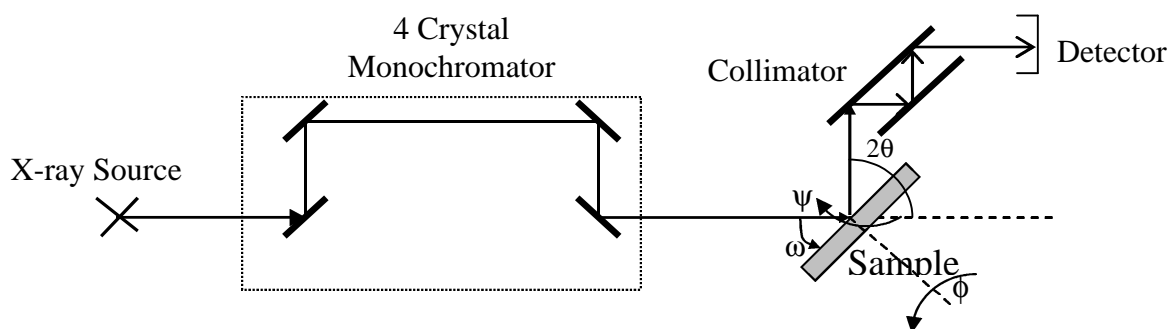
X-rays diffraction can measure the lattice parameter of a semiconductor. They can be used to study the presence of defects and "mosaic" kind of structures in highly perfect semiconductors. They are used to study the poly-crystallinity, amorphousness and the long-

range order in a semiconductor. Since the lattice parameter of each semiconductor is different from each other, this technique can be used to examine the composition of the semiconductor film very accurately. By looking into the strength of scattering or the "finite thickness fringes", the thickness of the sample can be determined. The basic information of thickness and composition can be utilized to examine the strain and structure factor. HRXRD can be used to determine the periodicity in a heterostructure or a low dimensional structure like multiple quantum wells. They can also be used to study the interface property in a heterostructure or a low dimensional structure. They can also be used to obtain width of low dimensional structures, their strain modulation etc. Thus, HRXRD technique can be used to optimize the parameters related to the semiconductor growth technology of bulk semiconductors, heterostructures and low dimensional systems.

The most usual form of high-resolution X-ray diffractometry is the one-dimensional rocking curve [229]. This is nothing but a  $\theta$ - $2\theta$  curve. It can be done on very simple diffractometer like single crystal diffractometer that has an X-ray source, a slit, a sample and a detector. But a diffractometer with more number of "monochro crystals" are preferred over single crystal diffractometer because of the better resolution obtained. More number of slits or crystals (for example, there are two slits in a double crystal diffractometer) substitutes the large X-ray dispersion obtained in a single crystal diffractometer (due to its single slit) thus giving out monochromatic beams to the sample. That is, the disappearance of large tail in the rocking curve is attributed to the collimating capability of more number of slits. Certain weakness in double crystal diffractometer is overcome by using four-reflection two-crystal monochromator [230,231]. There are a lot of information's that can be obtained through rocking curves. The intensity of the peaks relates to the scattering matter and the volume sampled. The oscillation period or the fringes relates to the thickness of the layer. The large peaks that are observed in the rocking curves (for example, of an epitaxial grown sample) could be related to the lattice parameter of the sample and the substrate. The width of the peak profiles is a function of the correlation length in depth and the intrinsic diffraction width for the material and variation of strain with depth and structural quality. Thus a lot of information can be obtained through the rocking curve analysis and all these information's are obtained by collecting the intensity, associated with each data point, from a large region in diffraction space. Practical interpretation of a rocking curve can be seen in a simplified paper written by M. A. G. Halliwell [229]. But this information obtained from rocking curve is extracted through a large number of assumptions. This can be overcome by plotting the X-ray scattering data points in reciprocal lattice space. This is called diffraction space mapping. This mapping technique is highly sensitive and an easy method to interpret the results. Detailed descriptions of both these techniques are given in [231,232].

#### [4.3.1.1] Experimental Setup for HR-XRD

Figure 4.4 gives the Schematic diagram of a high resolution X-ray diffractometer in triple axis mode. The X-ray measurements were performed in a multi-crystal high resolution Philips Extended X-pert Material Research Diffractometer equipped with a computer controlled motorized goniometer. This enables the optimization of the scattering angles with angular step sizes down to  $1.0 \times 10^{-4}$  degree for the angles of incidence and reflection, and step sizes down to  $1.0 \times 10^{-2}$  degree for the angles of rotation around the surface normal and rotation around the in-plane horizontal direction, respectively. Both double crystal and triple axis configurations were employed. A Ge (220) Bartels monochromator is used to collimate the Cu-tube x-ray incident beam with a divergence of 12 arc-sec and for secondary optics, the rocking curves were collected using a slit with a width of 180 arc-sec. While in triple axis configuration, which is an improvement over the rocking curve configuration, a Ge (220) triple-bound channel-cut crystal which gives a divergence of less than 12 arc sec was employed [233]. The reduction of the detector acceptance angle to less than 12 arc sec will imply the reduction of the probing size to similar dimensions and hence the possibility of resolving the different orientation distributions of the diffracted beam, and acquire a two dimensional iso-intensity contours. This configuration will enable the detection of minute mosaicity and strain variations that correspond to Ge fraction variations down to 0.02%. In addition the full width at half-maxima in different directions can be obtained from the 2D-RSM, and can lead to separate different structural effects.



**Fig. 4.3:** Schematic diagram of a high resolution X-ray diffractometer in triple axis mode.

#### [4.3.1.2] Synchrotron X-rays

As the thin film era has reached zero dimensionality, high power beams have become necessary to precisely evaluate the structure of surfaces and interfaces even to atomic level. It is therefore necessary to mention about Synchrotron radiation. This radiation can be utilized for the evaluation of low dimensional thin films [234]. These radiations are extremely intense

(hundreds of thousands of times higher than conventional X-ray tubes) and are highly collimated. They have a wide energy spectrum and can be highly polarized. They also emit radiation in very short pulses of the order of nano second. Due to these unique properties of synchrotron radiation, scientists can determine the structure of materials and molecules, the electronic structure of surfaces and interfaces even at the level of mono layers which is especially necessary for the analysis of quantum dots, analyze trace element concentration in micron sized regions [234,235] etc. The above mentioned advantages of synchrotron radiation give much in depth understanding in the field of Nanoelectronics.

#### [4.3.2] Transmission Electron Microscopy (TEM)

As the name depicts, this is a technique that uses electron beam as a source instead of light. In a transmission electron microscope (TEM), a monochromatic beam of electrons go through a thin sample ( $\leq 100$  nm). This monochromatic beam which is highly energetic in nature interacts with the atoms in the sample producing characteristic radiation (basic principle is the electromagnetic interaction of electrons with matter and is same as all other characterization techniques used in this thesis, reference: classical electrodynamics by J. D. Jackson) [236]. The resolution of the microscope is very much dependent on the energy of electrons. These radiations emitted can be collected to provide necessary information about the material under investigation. These radiations can be both deflected and non-deflected transmitted electrons, backscattered and secondary electrons and emitted photons. In general, the information on the size and shape of grains and arrangement of the atoms on the specimen can be obtained by using high resolution TEM. Apart from this, the degree of order of the atoms and the atomic scale defects can be analyzed. For an alloy material, their respective composition and their arrangement in the sample can be obtained. A detailed description on the principles of this technique and their application can be obtained from the reference [237,238]. By focusing the electron beam through the microscope, the electron beam can be converged towards the cross sectional plan of the sample and an array of disks can be obtained. This technique called as convergent beam electron diffraction (CBED) is widely used in Si/Si<sub>1-x</sub>Ge<sub>x</sub> system as well as in various heterostructures to obtain the strain at the interface. There are attempts by a few groups to analyze the strain in a Si/SiO<sub>2</sub> system as the strain in a tri layer system like ours can definitely influence the mobility and reliability of the device. A detailed description on these parameters that affects an MOS is more discussed in the next chapter.

We have used TEM to obtain information about the microstructure of Si/SiO<sub>2</sub>/poly-Si interface in an ultrathin MOS capacitor, which includes the oxide thickness and micro structural evolution of poly Si with various Ge doping. We obtained information like oxide thickness. Convergent beam electron diffraction technique (CBED) was used to derive the local strain in the poly-gate/SiO<sub>2</sub>/Si interface.

Samples were prepared by gluing them together with an M-bond. This was done to minimize the damage caused during the preparation (grinding) of the sample. Here, the poly-Si region was kept face to face. The setup was then clamped and hardened in a furnace at a temperature of 100 °C for 2 hour. Then the specimen was ground, polished, dimpled and ion milled.

#### [4.3.3] Secondary Ion Mass Spectrometry (SIMS)

When a material surface is bombarded by primary ions, secondary ions are emitted. The mass spectrometry of these secondary ions is the basis of SIMS technique. During SIMS analysis, the sample surface is slowly sputtered away. Thus the information of the elements as a function of depth (depth profile) can be obtained from this technique. Depth profile is indeed very useful for semiconductor industry where layered structures are commonly used. One of the advantages that SIMS offers over other depth profiling techniques like Auger electrons spectroscopy is its sensitivity (~ppm and for some elements ~ppb) to very low concentrations of elements. One disadvantage of this technique could be its destructive nature. Some of the variants of this technique are static SIMS, dynamic SIMS and Imaging SIMS. These variant techniques can be used for sub-monolayer elemental analysis, for obtaining compositional information as a function of depth below the surface and for spatially resolved elemental analysis, respectively. More details into this technique can be obtained from reference [239]. This technique can be employed to detect the presence of all the elements in the periodic table. Trace elements on a solid material like thin films and semiconductors can be quantitatively detected using this technique.

During the studies for this thesis, SIMS technique was used for various analyses. This technique was used to obtain the diffusion profile of boron in MOS devices. They were also used to study oxynitridation in MOS samples that were nitrogen ion implanted. Here, a time temperature study was done. Both rapid thermal annealing and furnace annealing were employed. This technique was also used to study trace elements in low dimensional heterostructures that are used in this thesis work. It has also been used to investigate tensile strained  $\text{Si}_{1-x}\text{Ge}_x$  grown on relaxed pure Ge on Si (001) substrates.

For our SIMS measurements, CAMECA ims 6f, was used. Prior to the analysis, the samples were kept for one day in a high vacuum at 50 C. The vacuum during the analysis was  $4 \times 10^{-10}$  mbars. For oxynitridation study Caesium ions, accelerated by 10 kV, were used as primary ions. The primary current was 20-30 nA. As secondary ions  $\text{O}_{16}$ ,  $\text{Si}_{30}$  and  $\text{Ge}_{73}$  isotopes were analysed. For determination of nitrogen distribution secondary ions  $\text{SiN}_{42}$  were analysed. The investigation of tensile SiGe was done using the same isotopes. The primary current was around 45 nA. The depths of the craters were measured with a tallysurf.

Happy is he who gets to know the reasons for things.

*Virgil (70-19 BCE) Roman poet.*

## Summary of Appended Papers

The summary of appended papers is given as follows:

- Paper I. In this paper, we have performed low temperature electrical characterization of ultrathin oxide MOS capacitors with  $p^+$  poly-Si<sub>1-x</sub>Ge<sub>x</sub> and poly-Si gate. The aim of this study is to compare the low temperature performance of poly-Si<sub>1-x</sub>Ge<sub>x</sub> and poly-Si gate MOS structures in the nanoscale channel length regime. Apart from the significant change in the flat band voltage, the result shows that all the poly-Si and poly-Si<sub>1-x</sub>Ge<sub>x</sub> gated MOS structures exhibit two centres of polarity change (zero temperature coefficients) in capacitance. The second polarity change leads to an exclusive phenomenon in these structures. The low temperature capacitance is found to be less than high temperature capacitance at strong accumulation and this is in contrast to what has been observed so far in metal gated capacitors. It is also observed that the temperature dependence of the tunnelling current is only on the oxide thickness and not on the gate material used.
- Paper II. In this paper, we have explored the microstructure and local interface strain in poly-Si<sub>1-x</sub>Ge<sub>x</sub>/SiO<sub>2</sub>/Si tri-layer system with ultrathin oxides. High resolution transmission electron microscopy (HRTEM) and high resolution x-ray diffraction rocking curves (HR-RC) and two dimensional reciprocal space mapping (2D-RSM) were the main characterization tools. The poly-Si<sub>1-x</sub>Ge<sub>x</sub>/SiO<sub>2</sub>/Si structures have  $x = 0, 0.2,$  and  $0.35$  for ultra thin oxides (2.0-3.0 nm). The result shows that for the adopted growth process, the poly grain size depends very strongly on the Ge concentration, and it increases with increasing the Ge mole fraction. In turn, this increase of the grain size in the poly-Si<sub>1-x</sub>Ge<sub>x</sub>/SiO<sub>2</sub>/Si reduces the strain in the film which then affects the interface strain at the lower SiO<sub>2</sub>/Si interface as observed by both 2D-RSM and TEM. In addition, presence of defects at the SiO<sub>2</sub>/Si interface was found to be larger for samples with no local interface strain.



Paper III.

Effect of temperature and time of heat treatment on the distribution of ion implanted nitrogen in poly-Si<sub>0.65</sub>Ge<sub>0.35</sub> gate MOS samples was studied. Secondary ion mass spectrometry (SIMS) was used for the qualitative analysis of the nitrogen distribution. Rapid thermal processing was done for a temperature range of 950 to 1070 °C for the re-distribution of ions. Our nitrogen implantation doses were  $5 \times 10^{14} \text{ cm}^{-2}$ ,  $2 \times 10^{15} \text{ cm}^{-2}$  and  $5 \times 10^{15} \text{ cm}^{-2}$ , all with implantation energy of 50 keV. For a uniform distribution of nitrogen in the SiO<sub>2</sub> region, an optimal temperature at a well calibrated time must be applied and this depends on the implantation dose. For medium and high concentrations the optimal conditions were 1050 °C and 15 second, and 1070 °C and 15 seconds, respectively. A uniform nitrogen distribution could be obtained through out the SiO<sub>2</sub> film. Prolonged heat treatment can cause degradation of the oxide layer and movement of the nitrogen and oxygen into the channel and the poly-Si<sub>0.65</sub>Ge<sub>0.35</sub> layer.

Paper IV.

We have investigated the relaxation properties of a tri-layer consisting of tensile strained SiGe grown over a fully relaxed Ge on Si 001 in an uninterrupted growth sequence. The uninterrupted growth was accomplished using chemical vapour deposition (CVD). High-resolution x-ray rocking curves (HR-RC) and two-dimensional reciprocal space mapping (RSM) were employed as the main characterization tool. Secondary ion mass spectrometry (SIMS) was used for chemical analysis for complementary measurement. A reference sample (B1) with only 1.5 µm thick fully relaxed Ge was first characterized. A second batch of two samples (B2 and B3), with an extra top 1.0 µm tensile strained Si<sub>1-x</sub>Ge<sub>x</sub> ( $x = 0.79$  for B2, and  $0.74$  for B3), were grown at slightly higher temperature compared to the initial Ge layer. For this tensile strained Si<sub>1-x</sub>Ge<sub>x</sub>, we have varied the Si flux, where it was doubled for B3 compared to B2. The variation of the Si flux was found to influence slightly the  $x$  fraction and a more pronounced variation of the tensile strain can be observed between B2 and B3. Moreover, all the lattice parameters were accurately extracted. For the bottom initially grown Ge, the derived lattice parameters for both the in- and perpendicular to plane, were extremely close to the bulk tabulated value of intrinsic Ge layer, indicating that a rather high quality pure fully relaxed Ge layers were resulted. From an initial estimation of the linear density of misfit dislocations at the interface, we found that the linear density of misfit dislocation is lower at the upper interface than the lower interface. This implies that, with the

adapted growth approach, high quality top final tensile strained  $\text{Si}_{1-x}\text{Ge}_x$  epitaxial layer can be obtained.

Paper V. The deactivation of nitrogen acceptors confined in  $\text{Cd}_{0.96}\text{Zn}_{0.04}\text{Te}/\text{Cd}_{0.86}\text{Zn}_{0.14}\text{Te}$  quantum well structures by hydrogen (deuterium) have been investigated by optical spectroscopy. Hydrogen (deuterium) was incorporated into the samples by annealing them in an atmosphere of hydrogen and cadmium. The annealing temperature and annealing time were varied to determine the optimum condition at which the maximum passivation is achieved without causing structural degradation. The emissions related to nitrogen acceptors were monitored in low-temperature photoluminescence measurements in order to deduce the passivation effect. The results indicate that hydrogen can effectively neutralise the nitrogen acceptors in cadmium zinc telluride quantum well structures. It is estimated that as much as 90% of the nitrogen acceptors can be passivated by this method.

Paper VI. A systematic study on the hydrogen passivation of nonradiative centres in InAs quantum dot's grown on GaAs substrates is presented. The samples used in this study were grown by molecular beam epitaxy. The structures contain an  $\text{In}_x\text{Ga}_{1-x}\text{As}$  insertion layer between the InAs quantum dots layer and the GaAs cap layer. The thickness and In-concentration of the  $\text{In}_x\text{Ga}_{1-x}\text{As}$  are varied to achieve the emission wavelength at 1.3  $\mu\text{m}$ . The samples after the  $\text{H}_2$  plasma treatment show a significant increase of the photoluminescence intensity. The experimental results show that the quality of the InAs quantum dot structures does not degrade after the hydrogen ( $\text{H}_2$ ) plasma treatments. The enhancement of the photoluminescence (PL) intensity from the InAs quantum dots is thought to be due to the passivation of nonradiative centres like defects in the structures. High resolution X-ray diffraction rocking curves are used to correlate photoluminescence results.

Paper VII. Photoluminescence experiments have been performed to systematically study the effect of thermal processing on  $\text{ZnSe}_{1-x}\text{Te}_x$  ( $x < 0.01\%$ ) epilayers. Our results show that, ZnSeTe epilayer under proper post growth thermal can emit light in the visible range of 5500-7000  $\text{\AA}$  at room temperature. Thus by systematically processing these samples, they could be used for II-VI laser diodes that can operate at room temperature. Hydrogen passivation study done on these samples

confirms the previous reports that the broad band emission is related to isoelectronic defect, i.e., excitons bound to the Te clusters.

Paper VIII.

In this paper, the post growth structural stability regarding relaxation, defect propagation interlayer layer diffusion, and Zn precipitation and/or out diffusion in  $\text{Cd}_{0.83}\text{Zn}_{0.17}\text{Te}/\text{Cd}_{0.92}\text{Zn}_{0.08}\text{Te}/\text{Cd}_{0.83}\text{Zn}_{0.17}\text{Te}$  quantum well (QW) heterostructures grown on (001) oriented  $\text{Cd}_{0.88}\text{Zn}_{0.12}\text{Te}$  substrates at 300 °C by molecular beam epitaxy is investigated. The investigated heterostructures were subjected to post growth thermal treatment in an ambient atmosphere in a temperature range between 280 °C and 550 °C for 3 hours each. We have used high-resolution x-ray diffraction as the main characterisation tool. High resolution rocking curves (HR-RC) as well as the powerful two-dimensional reciprocal space mapping (2D-RSM) was employed in both symmetrical as well as asymmetrical reflections. The results indicate that at a post growth temperature cycle of 350 °C for 3 hours; slight modification of the  $\text{Cd}_{0.83}\text{Zn}_{0.17}\text{Te}/\text{Cd}_{0.92}\text{Zn}_{0.08}\text{Te}$  barrier/QW heterointerface smoothness is affected. This indicates the onset of migration of Zn atoms at this post growth temperature time cycle. At 450 °C, this effect is more pronounced and seen as the complete disappearance of thickness fringes. For higher post growth thermal treatment of 550 °C for 3 hours, high relaxation level accompanied by Zn content reduction is observed. A reduction of the Zn content down to 0.11 fractional value in the thick  $\text{Cd}_{0.83}\text{Zn}_{0.17}\text{Te}$  barrier is attributed to Zn out diffusion and/or Zn precipitation.

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“The woods are lovely, dark and deep.  
But I have promises to keep,  
And miles to go before I sleep  
And miles to go before I sleep”

-Robert Frost, Stopping By Woods On A Snowy Evening.

# Paper I

Cryogenic Performance of Ultrathin Oxide MOS Capacitors  
with In Situ Doped  $p^+$  poly-Si<sub>1-x</sub>Ge<sub>x</sub> and poly-Si  
Gate Materials



# Cryogenic performance of ultrathin oxide MOS capacitors with *in situ* doped p<sup>+</sup> poly-Si<sub>1–x</sub>Ge<sub>x</sub> and poly-Si gate materials

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## Abstract

A low-temperature electrical characterization of ultrathin oxide MOS capacitors with p<sup>+</sup> poly-Si<sub>1–x</sub>Ge<sub>x</sub> and poly-Si gate is performed. The investigated structures are suitable for future nano-scaled high speed MOSFETs. The aim of this study is to compare the low-temperature performance of poly-Si<sub>1–x</sub>Ge<sub>x</sub> and poly-Si gate MOS structures in the nanoscale channel length regime. Apart from the significant change in the flat band voltage, the result shows that all the poly-Si and poly-Si<sub>1–x</sub>Ge<sub>x</sub> gated MOS structures exhibit two centres of polarity change (zero-temperature coefficients) in capacitance. The second polarity change leads to an exclusive phenomenon in these structures. The low-temperature capacitance is found to be less than high-temperature capacitance at strong accumulation and this is in contrast to what has been observed so far in metal-gated capacitors. It is also observed that the temperature dependence of the tunnelling current is only on the oxide thickness and not on the gate material used.

## 1. Introduction

The search for smaller, high performance, reliable CMOS transistors has reached quantum regime. The basic issue when fabricating smaller devices is to preserve the long-channel behaviour even after miniaturization. Thus scaling the channel region has invariably reduced the oxide thickness to the nanometre regime. Though there is a trend towards searching new gate materials, Si-based gate materials such as poly-Si are still being preferred because of the work function difference between the substrate Si and the gate Si. In the tunnelling regime, poly-Si<sub>1–x</sub>Ge<sub>x</sub> is more advantageous

because of the tuneable work function, improved resistivity, reduced gate depletion and reduced boron penetration.

Though new materials are introduced to assist in scaling a higher performance CMOS, never has a proper temperature scaling to optimize the performance been done. This is because there have been very few temperature-dependent studies to further the expertise. It appears that as long as improvements in the performance can be made at room temperature, low-temperature operation will not be taken seriously. Several research groups have recently shown a greater interest in low-temperature characteristics to assist in the scaling and have shown that the CMOS performance

can be improved by a factor of 1.5 to 2 over the room temperature CMOS [1, 2]. This is because in the tunnelling regime the oxide reliability is said to depend on voltage and temperature scaling [3]. Some of the other advantages include increased carrier mobility, reduced interconnect resistance, reduced susceptibility to latch up with the integrated circuit and a drastic reduction in thermally activated degradation mechanisms. The other reason for carrying out low-temperature investigations is to study the general properties of the new materials and the physics of devices that are scaled down to nanometre regime. There are also reports on the production of cryogenic operated CMOS circuits based computers and supercomputers [4]. But the interest in them slowly died due to lack of research in this area.

Most of the room temperature and low-temperature studies on MOS structures are done either on metal-gated structures or on thicker oxides [5, 6]. The room temperature studies have concentrated on the flat band voltage, capacitance in strong accumulation and inversion. This is because the flat band voltage and capacitance are of importance when designing the MOS devices and MOS circuits. The consistency of these parameters at all temperatures is important when a circuit is designed. The low-temperature studies have shown that at higher accumulation, there is a region called zero-temperature coefficient. This is a particular point at which Si capacitance changes polarity [7]. Zero-temperature coefficient is also of fundamental importance when designing a circuit to perform its function in a wide range of temperature.

In this work, we have investigated the low-temperature performance of  $p^+$  poly-Si and  $p^+$  poly-Si<sub>1-x</sub>Ge<sub>x</sub> (with two different Ge concentration, Ge = 20% and Ge = 35%) gated ultra thin oxide MOS structures. Though there are a few reports available for the theoretical evaluation of the dependence of flat band capacitance on temperature [8], there are no reports to verify them experimentally. In fact this is the first experimental attempt to elucidate the flat band voltage of an ultra thin oxide MOS device with poly-Si and poly-SiGe gate at low temperature. We have also performed tunnelling current measurements at various temperatures.

## 2. Experiment

PMOS capacitors were fabricated on 0.142  $\Omega$  cm (100) n-type Si wafers from Wacker Siltronic. Nitrated oxide (NO)-grown ultra thin gate oxides ( $3.0 \pm 0.2$  nm according to ellipsometry, TEM,  $C-V$  and  $I-V$  measurements) were grown at 750–800 °C, using an ASM A400 vertical furnace. The gate electrodes,  $p^+$  poly-Si<sub>1-x</sub>Ge<sub>x</sub> ( $x = 0, 0.20, 0.35$ ) were deposited in an LPCVD ASM system using SiH<sub>4</sub> and GeH<sub>4</sub> at a pressure of 40 Torr and temperatures of 615 °C and 640 °C, respectively. In order to facilitate nucleation of poly-Si<sub>1-x</sub>Ge<sub>x</sub> on the SiO<sub>2</sub>, an undoped Si seed layer with a nominal thickness of 1 nm was deposited at 615 °C prior to the poly-Si<sub>1-x</sub>Ge<sub>x</sub> layer deposition. Previous reports indicate that this adhesion layer has negligible influence on determination of the basic characteristics such as flat band voltage and work function of the  $p^+$  poly-Si/Si<sub>1-x</sub>Ge<sub>1-x</sub> [14]. Varying the SiH<sub>4</sub> flow at a fixed GeH<sub>4</sub> flow controlled the Ge content. The thickness of the gate layers was 200 nm according to optical Tencor Spectra map measurements and high-resolution

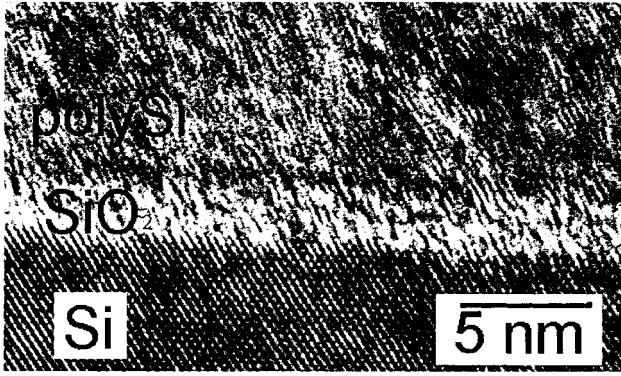
transmission electron microscopy (HRTEM) measurements. HRTEM observations were performed with a Philips CM 200 electron microscope, operating at 200 kV. A cross-sectional TEM specimen was prepared by mechanical grinding and ion milling. Aluminium (~500 nm) was used as a metal contact.

To suppress B penetration and gate depletion, nitrated gate oxides and *in situ* doping was used. Diborane (B<sub>2</sub>H<sub>6</sub>) was used during poly-deposition to induce p-type doping. Thus all these devices under consideration are *in situ* doped and the dopants are already electrically active after deposition.

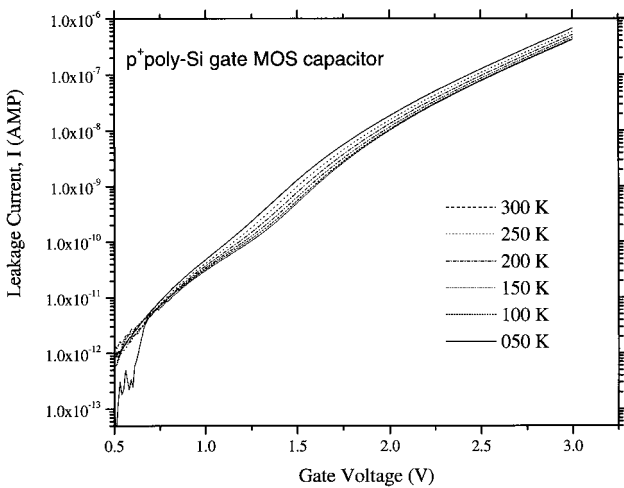
The processed devices are of different dimensions ranging from 600  $\mu\text{m}^2$  to 200  $\mu\text{m}^2$ . Measurements were performed on all these devices. The results were consistent. The results reported in this paper are for 500  $\mu\text{m}^2$  devices. Two different measurement techniques have been employed: capacitance–voltage–temperature ( $C-V-T$ ) measurements and current–voltage–temperature ( $I-V-T$ ) measurements. The voltage sweeps were always conducted from low negative to high positive voltage such that the n-type substrate went into accumulation. For temperature control a cryostat has been used allowing a temperature span of 50–300 K. All measurements were carried out in the dark. The  $C-V$  curves were measured at frequencies ranging from 1 MHz to 1 kHz. There was no difference in the  $C-V$  curves for those frequencies below 100 kHz. In our analysis, we consider the  $C-V$  measurements taken at 10 kHz. The  $C-V$  curves were also correlated for both the series and parallel resistance mode. This means that a resistor is connected in series or parallel with the device under test (DUT). It was found that those devices which did not correlate their results for the series and parallel mode measurements did not show similar characteristics as the temperature is reduced. Also, poor accumulation was observed at temperatures below 100 K. These devices also showed no zero-temperature coefficients. This disparity in the  $C-V$  curves can be accounted for series resistance effects which can occur due to poor contacts in these devices. These devices are thus discarded. The measurement data shown in this paper correspond to those devices that match both in frequency and resistance modes. In order to avoid electrical stress that is common at moderately high voltages for ultra thin oxides, the biasing was limited to between  $-3$  and  $+3$  V.

## 3. Results and discussions

Figure 1 is an HRTEM cross-sectional view of the capacitor with poly-Si gate material. The Si substrate provides a good single-crystal silicon [110] lattice image. Grains in the poly-Si (Ge) layer orientate along different directions. Lattice fringes can only be observed from poly-Si or Ge when the grains are aligned along certain zone axis. Silicon dioxide layer is formed uniformly between poly-Si or Ge and single Si, and it does not show lattice fringes, which corresponds to amorphous material. The Si–SiO<sub>2</sub> interface is rather smooth, while the poly-Si(Ge)–SiO<sub>2</sub> interface is not so even, and its non-uniformity in thickness is about 0.2 nm. Using Si (111) lattice spacing (0.314 nm) to calibrate the magnification of the image, the average thickness of the oxide layer is  $3.0 \pm 0.2$  nm.



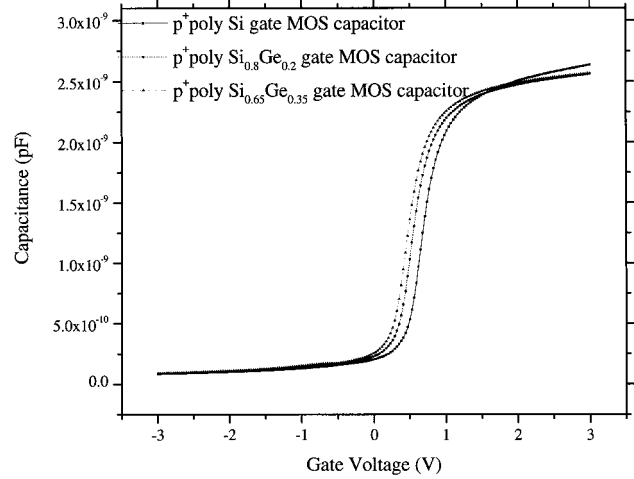
**Figure 1.** High resolution cross-sectional TEM of an ultra thin-oxide poly-Si gate MOS capacitor. The average oxide thickness is estimated to be  $3.0 \pm 0.2$  nm.



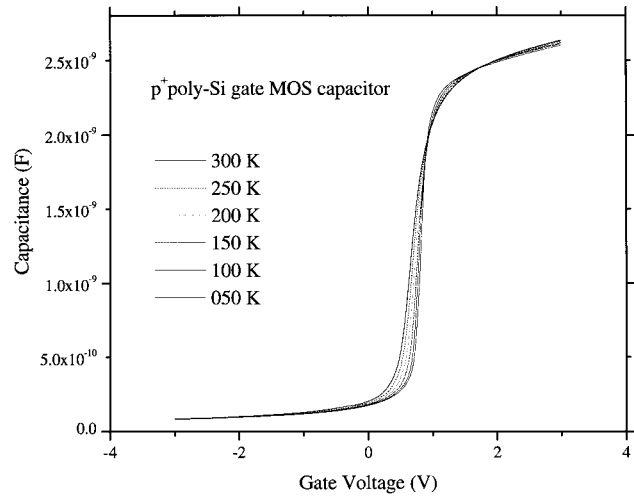
**Figure 2.** The temperature dependence of the gate leakage current of a poly-Si gated MOS capacitor in the accumulation mode.

Figure 2 shows the temperature dependence of the gate leakage current–voltage characteristics of a poly-Si gated MOS capacitor. We find that the leakage current appreciably decreases with temperature for a specific voltage. There is also no significant change in the leakage current density of poly-Si gated devices and poly-SiGe devices, for positive gate voltages at a specific temperature. A fractional increase in current was also calculated for a voltage value of 2.5 V for all the devices. This voltage was preferred because the sample is under strong accumulation. The values show that as long as the device is under strong accumulation, there is no appreciable change in their values. This is as expected because the tunnel current depends on the oxide thickness. Similar studies showed that temperature dependence could be found only when Fowler–Nordheim tunnelling takes place. When comparing with the previously reported work [6], it can be concluded that the temperature–tunnelling current correlation is independent of the gate material. Thus this result is complementary to the previous report [6].

Figure 3 shows the  $C$ – $V$  characteristics of poly-Si and poly-Si<sub>1-x</sub>Ge<sub>x</sub>,  $x = 0.20$  and  $0.35$ , respectively [9]. These measurement results are taken at room temperature. The oxide thickness was extracted from this figure with a conventional



**Figure 3.** Capacitance–voltage characteristics for  $p^+$  poly-Si gate MOS capacitor and  $p^+$  poly-Si<sub>1-x</sub>Ge<sub>x</sub> gate MOS capacitor with  $x = 0.20$  and  $0.35$ , respectively. The figure shows how the flat band voltage changes with increasing Ge concentration.

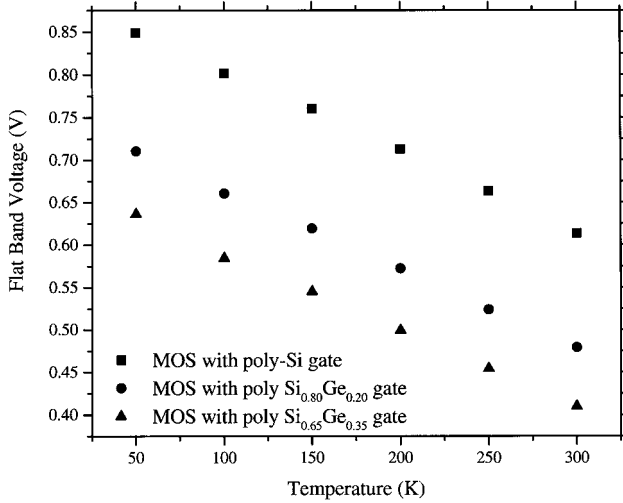


**Figure 4.** The capacitance–voltage–temperature ( $C$ – $V$ – $T$ ) scan for poly-Si device.

$CV$  theory [10]. The values obtained for the oxide thickness using  $C$ – $V$  measurement is around  $3.0 \pm 0.1$  nm. This is in agreement with the values obtained through spectroscopic ellipsometry and HRTEM.

Figure 4 shows the  $C$ – $V$ – $T$  (capacitance–voltage–temperature) scan for poly-Si device. The effect of the temperature on the flat band regime and in the accumulation is clearly visible from this plot. Similar curves corresponding to the respective temperature were obtained for the other samples with different Ge concentration. Parameters such as doping concentration, flat band capacitance and flat band voltage were obtained from these curves. Conventional MOS theory [11, 12] was used to derive the temperature dependence of these various parameters. The following expression is used to derive the flat band capacitance:

$$\text{Flat band capacitance, } C_{\text{FB}} = \frac{\epsilon_{\text{ox}}}{t_{\text{ox}} + \frac{\epsilon_{\text{ox}}}{\epsilon_{\text{Si}}} \sqrt{\frac{K \times T}{e} \left( \frac{\epsilon_{\text{Si}}}{e \times N_{\text{D}}} \right)}}$$

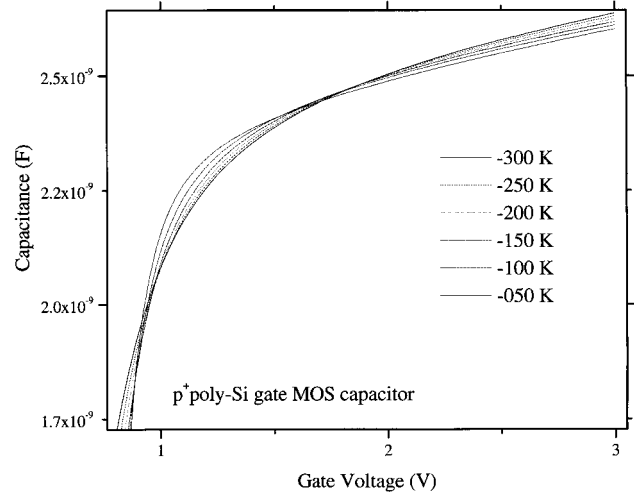


**Figure 5.** Flat band voltage as a function of temperature for poly-Si and poly-Si<sub>x</sub>Ge<sub>1-x</sub> (with  $x = 0.20$  and  $0.35$ ) structures are shown in this figure.

where  $\epsilon_{ox}$  and  $\epsilon_{Si}$  is the absolute dielectric permittivity of the oxide and the semiconductor, respectively,  $t_{ox}$  denotes the thickness of the oxide,  $K$  corresponds to the Boltzmann constant,  $T$  is the absolute temperature,  $e$  represents charge of an electron and  $N_D$  is the equilibrium concentration of the majority carriers in the silicon substrate. The substrate doping concentration was obtained by extrapolating the depletion region. This is found to be  $(5-6) \times 10^{16} \text{ cm}^{-3}$  at room temperature and is in agreement with the manufacturer's measurements.

Figure 5 shows the dependence of flat band voltage upon the temperature of both the poly-Si and poly-Si<sub>x</sub>Ge<sub>1-x</sub> (with  $x = 0.20$  and  $0.35$ ) structures. We have extrapolated the flat band voltage from the flat band capacitance using the conventional MOS theory described above. The figure shows how the flat band voltage of individual devices corresponding to both poly-Si and poly-Si<sub>x</sub>Ge<sub>1-x</sub> changes with various temperatures. It is seen that the flat band voltage difference for these structures is consistent over the temperature range under consideration. This difference in flat band voltage between different devices is due to the work function difference between the different poly-gate materials. Below 100 K, one expects partial ionization of impurities. But, by using these expressions to derive the flat band voltage, we get a better correlation even below 100 K. It should be worth noting that for devices that showed series resistance problems, the derived flat band voltages were inconsistent, and in many cases, poor accumulation resulted in difficulty to extrapolate the flat band voltage.

Figure 6 shows the  $C-V-T$  plot of the poly-Si gated MOS device in the accumulation region. The results for the other two devices (poly-SiGe, Ge = 20%, and 35%) also show similar results. In this region, the temperature dependence is not in accordance with that of those measured for metal gated or thicker oxide MOS structures [6]. In metal gated and thicker oxide structures, the low-temperature capacitance in the accumulation region is higher than that of the high temperature capacitance. In the devices considered in this work, it is found



**Figure 6.** An enlarged figure of  $C-V-T$  curve for a p<sup>+</sup> poly-Si device in the accumulation region. Zero temperature coefficient points are shown in the figure.

that the low-temperature capacitance is lower than that of the high-temperature capacitance (see figure). Also in a similar work done previously, it was found that there is only a single zero-temperature coefficient. The first reported theoretical and experimental work on zero-temperature coefficient [7] showed that this is a region where the substrate capacitance–substrate voltage ( $C_S-V_S$ ) plots intercept, i.e. at a unique crossover point, is independent of temperature. This region is said to depend on the oxide thickness, interface trap density, the doping level of both Si substrate and the doping level of poly-Si region. The reported work [9] was carried out at room temperature and elevated temperatures. But, our results show that the poly-Si based tunnelling devices give two such regions where the Si capacitance changes its polarity. It is to be noted that the zero-temperature coefficient is not a point but a small region of a definite voltage value. The broadening of this intersection into a spot is attributed to the oxide capacitance in series with the silicon capacitance [13]. In our devices, each zero-temperature coefficient spans a voltage range of around  $0.1 \pm 0.04 \text{ V}$ . The voltage difference between the two zero-temperature coefficient, i.e. between the two polarities is around  $0.8 \pm 0.1 \text{ V}$ . This is similar for all the three samples described here. These voltage values are just a rough estimate. Thus, these values are irrespective of the gate material being used. The significance of these crossover voltages needs further investigation because the results are of fundamental importance. From the figure, we found that in strong accumulation, the capacitance decreases with temperature and this reduction in capacitance is consistent as we lower the temperature. This second polarity could be due to poly-depletion. We believe that this very much depends on the doping concentration of the poly-region. If we increase the poly-doping to higher concentration, the voltage difference between the two polarities will be decreasing and we would be able to see only one of the crossing over voltage. That is, this difference is speculated to be negligible at a doping concentration of  $10^{23} \text{ cm}^{-3}$ . A thorough theoretical evaluation is needed to explain this phenomenon. As stated



earlier, these results are cross-checked for all measurement frequencies (1 kHz–100 kHz) and series as well as parallel resistance configurations in the LCR meter. Though the 1 MHz showed similar figures, we do not compare those results because of the small difference seen in the accumulation capacitance when compared with lower frequencies. Even the devices with smaller dimensions showed similar results.

#### 4. Conclusion

The low-temperature characterization of  $p^+$  poly-Si and  $p^+$  poly-Si<sub>1-x</sub>Ge<sub>x</sub> MOS capacitors is performed. We have done current–voltage ( $I$ – $V$ ) measurements for various temperatures. The fractional current values derived from the  $I$ – $V$ – $T$  plot, show that the tunnelling current at accumulation at various temperatures does not depend on the gate materials used. We have done an experimental attempt to elucidate and compare the flat band voltage of an ultra thin oxide MOS device with poly-Si and poly-SiGe gate at low temperature. Upon comparing the flat band voltage between various devices, we find that they are consistent at all measured temperatures. The flat band dependence of temperature and its consistency is very much important for all devices that are to operate at varying temperatures. Another major result of fundamental importance is that these structures do not follow similar characteristics in the accumulation region as observed in a thicker oxide or metal-gated MOS structures. In our structures, we can find two regions in the accumulation region where the polarity of the Si capacitance changes. This is thus different from the previously reported works on metal gated or thicker oxide structures.

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## Paper II

Structural Roughness and Interface Strain Properties in  
Si/SiO<sub>2</sub>/Poly-Si<sub>1-x</sub>Ge<sub>x</sub> Tri-layer System with Ultra Thin  
Oxide





# **Structural Roughness and Interface Strain Properties in Si/SiO<sub>2</sub>/Poly-Si<sub>1-x</sub>Ge<sub>x</sub> Tri-layer System with Ultra Thin Oxide**

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## **Abstract**

We have explored the microstructure and local interface strain in poly-Si<sub>1-x</sub>Ge<sub>x</sub>/SiO<sub>2</sub>/Si tri-layer system with ultrathin oxides. High resolution transmission electron microscopy (HRTEM) and high resolution x-ray diffraction rocking curves (HR-RC) and two dimensional reciprocal space mapping (2D-RSM) were the main characterization tools. The poly-Si<sub>1-x</sub>Ge<sub>x</sub>/SiO<sub>2</sub>/Si structures have  $x = 0, 0.2, \text{ and } 0.35$  for ultra thin oxides (2.0-3.0 nm). The result shows that for the adopted growth process, the poly grain size depends very strongly on the Ge concentration, and it increases with increasing the Ge mole fraction. In turn, this increase of the grain size in the poly-Si<sub>1-x</sub>Ge<sub>x</sub>/SiO<sub>2</sub>/Si reduces the strain in the film which then affects the interface strain at the lower SiO<sub>2</sub>/Si interface. In addition, presence of defects at the SiO<sub>2</sub>/Si interface was found to be larger for samples with no local interface strain.

## **Introduction**

Microstructural evaluation of future nanoscaled CMOS devices is becoming very important. The reason is that the quality and reliability of these quantum structures can be improved only thorough fundamental understanding in the nano-regime. Two basic structural problems that require attention for an ultrathin oxide MOS structure is the roughness [1, 2] and the strain [1, 3] at the poly-Si/SiO<sub>2</sub>/Si interface. The roughness and the strain in the Si/SiO<sub>2</sub> interface region of a thermally grown ultrathin oxide are much higher when compared to the thicker oxides. This is because ultrathin thermal oxides are grown at a comparatively

lower temperature. The interfacial roughness increases the surface scattering thus decreasing the mobility in the silicon channel region [4, 5]. Strain in a SiO<sub>2</sub>/Si region could be differentiated into two kinds: it could be either macroscopic or interfacial in nature or a mixture of both types. The macroscopic strain is seen in the bulk region of the oxide. This strain originates due to two reasons: the intrinsic property of the oxide and the stress exerted upon them by the gate electrode. The difference in the thermal expansion coefficients of Si and SiO<sub>2</sub> could be the reason for such an intrinsic oxide property [6]. The interfacial strain is tensile and is due to the lattice mismatch between the bulk Si and SiO<sub>2</sub> system. The strain can be extended both into the SiO<sub>2</sub> and bulk Si to a few monolayers. Due to the strain, O-Si-O bonds get distorted and become weak. When carriers are injected into a structure which is rough and strained, the injected hot electrons or holes can easily break these weak bonds causing oxide degradation [6-10]. But it is seen that the oxynitrides exhibits improved reliability as compared to the pure oxides [11]. This improvement in oxynitrides could be due to the relaxation of the strain at the interface and the reduction of the trap density. The mechanism can be explained as follows: the nitrogen atoms bonded to the dangling bonds present in the interface releases the interface strain. This could subsequently reduce the trap density, suppressing the breakdown of the oxide and increase the immunity of the trap generation under the current stress [6, 12]. The performance of the deep sub-micron regime MOS structures also depends on the morphology of poly-Si gate electrode [13]. The growth of poly-Si films on SiO<sub>2</sub>/Si system introduces compressive strain to the bulk film and the quantity of this strain depends on the poly thickness [14]. In quantum regime, poly-gate electrodes also face problems like poly-depletion, dopant diffusion etc. Thus, the poly-grain size, crystal orientation, strain between the poly-grains, strain at the conducting channel (Si/SiO<sub>2</sub> interface) and interface roughness of the poly-gate/SiO<sub>2</sub> region are all necessary to be evaluated carefully, in order to improve and understand the performance of MOS ultra short channel devices.

Some of the common analytical techniques that are generally used for the study of strain and microstructure are Rutherford backscattering (RBS) [15], medium energy ion scattering (MEIS) [16], x-ray photoelectron spectroscopy (XPS) [15, 17] and x-ray diffraction [14] etc. On the other hand transmission electron microscopy (TEM) gives the possibility of obtaining much more information in the length scale of these devices. In addition, TEM is a powerful and versatile technology to observe the morphology of interfaces in image mode and also to analyse the strain around interface in diffraction mode. Cross-sectional high-resolution

TEM has been effectively used to investigate the thickness of amorphous layer and the statistical properties of random fluctuation in the interface boundary [18, 19]. Furthermore, convergent beam electron diffraction (CBED) and large angle CBED (LACBED) have been applied to measure the local strain, especially lattice mismatch at crystalline interfaces [20-23]. However, the situation between crystalline and amorphous interface could be different. Banhart et al [24] showed that the splitting and blurring of deficiency line in LACBED patterns implied for the strain and dislocations around the interface area, as well as the bending of layers towards the substrate. Moreover, high resolution x-ray diffraction (HR-XRD) is also another powerful tool for detecting minute structural fluctuations such as defects, strain, and dislocations. With the use of both high resolution rocking curves (HR-RC) and two dimensional reciprocal space mapping (2D-RSM), lattice parameter variation in the order of  $10^{-8}$  can be achieved [25]. In addition, the roughness and local minute strain fields at interfaces can be detected and identified from careful analysis of the nature of diffraction peaks from XRD [26]

The aim of the present work is to investigate microstructural properties and strain at poly-Si<sub>1-x</sub>Ge<sub>x</sub>/SiO<sub>2</sub>/Si interfaces. The thickness of SiO<sub>2</sub>, roughness of poly-Si<sub>1-x</sub>Ge<sub>x</sub>/SiO<sub>2</sub> with or without N in the SiO<sub>2</sub>, and the microstructure evolution of poly-gates were studied by HREM. Strain field at SiO<sub>2</sub>/Si interface was revealed by LACBED, and it was confirmed by HR-XRD measurements using both HR-RC and 2D-RSM.

## Experiment

PMOS capacitors were fabricated on (100) n-type Si wafers from Wacker Siltronic. Ultra thin nitrated oxide (NO) gate dielectric structures (2.5 and 3.0 nm) were grown at 750-800 °C, using an ASM A400 vertical furnace. The gate electrodes, p<sup>+</sup> poly-Si<sub>1-x</sub>Ge<sub>x</sub> (x=0, 0.20, and 0.35) were deposited in a low pressure chemical vapour deposition (LPCVD) ASM chamber using SiH<sub>4</sub> and GeH<sub>4</sub> at a pressure of 40 torr and temperatures of 615 °C and 640 °C, respectively. In order to facilitate nucleation of poly-Si<sub>1-x</sub>Ge<sub>x</sub> on the SiO<sub>2</sub>, an undoped Si seed layer with a nominal thickness of 1 nm was deposited at 615 °C prior to the poly-Si<sub>1-x</sub>Ge<sub>x</sub> layer deposition. Varying the SiH<sub>4</sub> flow at a fixed GeH<sub>4</sub> flow is adopted to control the Ge content. The thickness of the gate layers was 200 nm according to optical Tencor Spectra map measurements and high-resolution transmission electron microscopy (HRTEM) observations.

Four different samples (S1-S4) were used for cross-section HRTEM, LACBED, HR-RC, and 2D-RSM measurements. Table I describes the details for the different samples. The samples for TEM were cut into several pieces with size of  $3 \times 1 \text{ mm}^2$ . In order to obtain a thin area from the cross section, as well as to avoid destroying the polycrystalline  $\text{Si}_{1-x}\text{Ge}_x$  layer, two surfaces of poly- $\text{Si}_{1-x}\text{Ge}_x$  were glued together with the M-bond glue. Before gluing the two samples, their surfaces were cleaned by acetone. The samples were glued, clamped and hardened in the furnace at  $100^\circ\text{C}$  for 2 h. The specimen was then polished on both sides to a thickness of around  $70\text{-}80 \text{ }\mu\text{m}$ . Before ion milling, the thin film was dimpled in the centre of cross-section part giving a thickness around  $20 \text{ }\mu\text{m}$ . Ion milling was carried out by using Precision Ion Polishing System (PIPS). The HR-TEM was performed on a Philips CM200 equipped with energy x-ray dispersive spectroscopy and Gatan image filtering (GIF) system. The point resolution of the microscope is  $2.4 \text{ }\text{\AA}$ . HR-RC and 2D-RSM were performed using Philips Extended X-pert material Research Diffractometer. This diffractometer is equipped with a computer- controlled motorized goniometer. Both double crystal and triple axis configurations were employed. A four crystal Ge (220) Bartels monochromator is used to collimate the Cu-tube x-ray incident beam with a divergence of  $12 \text{ arcsec}$ , and for secondary optics, the rocking curves were collected using a slit with a width of  $0.5 \text{ degree}$ . For collecting the 2D-RSMs, the diffractometer was set into the extended configuration and a Bartels monochromator was used.

## Results and discussion

Figure 1 (a-d) show the cross sectional HRTEM micrographs for specimen S1-S4 respectively (described in Table I). For all the specimens, the substrate gives a single crystalline silicon  $[110]$  lattice image. The single crystal  $\text{SiO}_2/\text{Si}$  interface plane is parallel to the  $(002)$  substrate planes. On average the lower  $\text{SiO}_2/\text{Si}$  interface is very sharp. However, the upper poly $\text{Si}_{1-x}\text{Ge}_x/\text{SiO}_2$  interface is not well defined. The oxide layer is lighter in appearance than the poly- $\text{Si}_{1-x}\text{Ge}_x$  layer or the crystalline Si, showing that the oxide is amorphous in nature. In some regions, the poly- $\text{Si}_{1-x}\text{Ge}_x$  gives a mottled structure, showing that some of the grains are off the zone axis. This may cause blurring at the interface between poly- $\text{Si}_{1-x}\text{Ge}_x$  and  $\text{SiO}_2$  from microstructural observation. Based on the comparison for a long range of  $120\text{-}200 \text{ nm}$  cross sectional view, it is found that specimen S1 and S2 have a relatively flatter poly-electrode/ $\text{SiO}_2$  interface than the samples S3 and S4. This might be because the samples S3 and S4 have poly- $\text{Si}_{1-x}\text{Ge}_x$  gate electrodes. Furthermore,  $\text{SiO}_2$  thickness deviation was also

observed in all the specimens. The deviation in specimen S3 is around 0.5-0.8 nm in some areas. The average thickness value of SiO<sub>2</sub> layer in different specimens measured by HREM and a comparative thickness obtained from Capacitance-Voltage (C-V) measurements are illustrated in table II. The oxide thickness was extracted from the accumulation region of the capacitance spectrum [27]. The uncertainty caused by TEM roughness and measurement is about  $\pm 0.2$  nm.

The evolution of the poly-Si<sub>1-x</sub>Ge<sub>x</sub> ( $x = 0, 0.2, 0.35$ ) morphologies in the four different samples is shown in figure 2(a-d). For specimen S1 and S2 ( $x = 0$ ), the grains are columnar perpendicular to the surface with grain width around 10 nm. From x-ray diffraction studies, the diffraction peaks of sample S1 and S2 are dominated by the {220} line. This indicates that the development of the columnar structure is associated mainly with growth along the {220} orientation and the random phase corresponding to other peaks is proportionally much less in the observation. The grains grow much wider for specimen S3, increasing to around 25-50 nm while still keeping the columnar shape. However the grain size increases dramatically in specimen S4, with a tooth-like grain shape. In our samples, it is found that as the Ge concentration increases, the average grain size of the poly-SiGe is larger.

Several studies have shown that boron diffusion is less in poly-Si(Ge) samples compared to poly-Si samples [28, 29]. One of the possible reasons for the decrease in boron diffusion in the poly-Si(Ge) gate could be due to its larger grain size compared to the poly-Si material. The presence of more grain boundaries in poly-Si enhance the dopant diffusion in them. Besides the grain size and grain boundaries, boron diffusion in poly-Si can also be enhanced by the compressive strain inside the polycrystalline region. Usually the larger the grain size, the less strain is observed in the polycrystalline film. This means that the relatively larger grain size observed in the poly-Si(Ge) could possibly reduce the strain in them. This reduced strain in turn affects the whole tri-layer system. In particular the strain at the lower SiO<sub>2</sub>/Si interface, which is the conducting channel for MOS devices, is observed to be dependent on the strain on the top poly-material status (see discussion of the interface strain below). The reliability of MOS devices with poly-Si(Ge) is observed to be higher than those employing poly-Si as gate electrode [30].

The LACBED patterns from the lower Si/SiO<sub>2</sub> interface were obtained for all the four samples. Figure 3 (a) gives the pattern for an area which is far away from the interface. Figure

3 (b-d) gives the patterns for the sample S1, S2 and S4. These patterns were obtained by focusing the probe on the specimen. Within the pattern, the image and diffraction lines corresponding to reciprocal-lattice planes can both be observed at the same time. For sample S1, S2 and S3, it is clearly observed that the diffraction lines running towards the interface become more blurred or splitted when they are close to the interface. The blurring is more pronounced when the lines tend to be parallel and is less when it is normal to the interface. This indicates that the lattice planes parallel to the (002) oriented-interfaces must be tilted or strained; whereas lattice planes perpendicular to the (002) plane is only slightly affected. It is also observed that the width of splitting increased when the probe is closer to the interface. Although the splitting or blurring effect of the diffraction lines is observed in sample S4, the distortion is not as serious as other samples. This shows that there is less of strain in the Si/SiO<sub>2</sub> interface of Sample S4.

The volume expansion of SiO<sub>2</sub> compared to that of Si is larger by a factor of 2.25. This leads to a compressive lateral force on Si, and results in a tetragonal distortion of the lattice perpendicular to the interface. This indicates that the lattice planes closer to the interface could change their lattice spacing or deviate from their original position slightly. In another words, the change in lattice spacing and inclination of the diffraction planes shift the diffraction lines in LACBED pattern. The change of Bragg angle  $\theta$  and the inclination angle  $\varphi$  of the diffraction plane to the interface is related by:

$$\Delta\theta = (\Delta d/d) \tan\theta_B \quad (1)$$

$$\Delta\varphi = (\Delta d/d) \tan\varphi \quad (2)$$

Here  $d$  is the lattice plane spacing. The shifting of the diffraction lines are caused by both  $\Delta\theta$  and  $\Delta\varphi$ . If the plane parallel and close to the interface bend due to the stress, the curved plane acts as several small planes and rotates along the axis parallel to the interface, i.e., the electron beam is perpendicular the axis. It is then that the shifted diffraction lines are observed. If the plane perpendicular to the interface is distorted when it comes to the interface, the fragments of curved plane like to rotate along the axis perpendicular to the interface. As a result, the diffraction line rotates, and the splitting is obtained. Both situations mentioned above are the extreme cases; the common case is something in between.

To directly investigate the strain and/or defect propagation at the Si/SiO<sub>2</sub> interface we also performed HR-XRD measurements. Both HR-RC and 2D-RSM for symmetric and asymmetric reflections were measured and carefully evaluated for samples S1-S4. The same measurements were also performed on a blank Si as a reference, which is the same type (orientation and doping concentration) of those used for the processing of S1-S4. The Si reference sample is R1.

Figure 4 shows the asymmetric 113 HR-RC of samples S1, S2, S3, S4, and a simulated curve for the silicon reference wafer. It is clearly seen that all samples exhibit different full-width at half-maxima value (FWHM). Figure 5 shows the summary of the FWHM obtained from the 113 asymmetric curve variation with the oxide thickness for all samples. Comparing sample S1 and S2 we see that sample S1 has a FWHM of 0.0043 while sample S2 has a FWHM of 0.0084. For sample S3 it has a value of 0.0045 and finally for S4 the FWHM is about 0.011. The simulated curve has a value of 0.0028, which is comparable with sample S1.

The 113 asymmetric reflections with small angle of incidence  $\sim (2 \text{ to } 3^\circ)$  are chosen due to its sensitivity to interfaces for structures with thin layers as the one in the present study. Evaluating the FWHM of the symmetric 004 HR-RC, the same samples has not yielded any observable increase or decrease of the FWHM as expected. This is due to the fact that the 004 reflection with an angle of incidence of more than 30-degree will carry very little information from the interface.

In general the FWHM from HR-RC can not be used as an absolute figure of merit due to the fact that it contains a sum of contributions from many different sources. These sources are the resolution of the incident monochromator and contributions from finite thickness effect of these layers. In addition, strain and composition variations beside defects can all contribute to the FWHM value. From evaluating HR-RC these effects can not be separated. However, 2D-RSM is much more useful and gives a direct quantitative and qualitative evaluation of all these different effects separately. Thus, to separate these effects we have performed 2D-RSMs of all samples around the 113 reciprocal lattice points. The measurements of the 2D-RSMs were performed for all samples using the same acquisition conditions (scan ranges, steps, time per step etc.). This is important for the present investigation to systematically monitor and compare minute local strain fields. The time

collection of these 2D-RSMs was more than 10 hours for each sample. From 2D-RSMs, we evaluate the FWHM along different directions. The two most important directions are along  $\omega$  and  $\omega/2\theta$  scan angles. In addition, the elongation along the low count iso-contours, i.e. along  $\omega$ -scan direction is very useful, since it gives quantitative information about the local strain/relaxation fields.

Figure 6 is a typical 2D-RSM around 113 reciprocal lattice points for all the samples from S1- S4, together with the Silicon reference wafer R1. Here we concentrate on two parameters. The first is the FWHM along the  $\omega$ -scan direction and the  $\omega/2\theta$  scan direction. The second is the elongation and shape of the low iso-intensity contours (outer contours). Figure 7 shows the summary of the FWHM along the  $\omega$  scan direction obtained from the measurements of Fig. 6. As it is clear, sample S2 and S3 are the structures with the lowest density of interfacial and structural defects while the sample S4 is having the highest interfacial structural defects. Investigating and comparing the elongation of the low count iso-intensity contours of the 2D-RSM, we can categorize them in two groups. The 1<sup>st</sup> is the silicon reference sample and the S4. Here both maps show no elongation of the low count iso-intensity contours along the  $\omega$  scan direction while the S1, S2 and S3 show a clear elongation of the low count iso-intensity contours along the  $\omega$ -scan direction. This is an indication of local strain fields, which means that silicon at the interfacial and to a depth of few monolayers is subjected to tensile strain in the samples S1-S3.

The electrical stress measurements performed on sample S2 and S4 shows that the reliability of sample S4 is higher than S2 [30], and is consistent with the above results. This can be explained on the basis of strain. In Sample S2, there is high interfacial strain compared to S4 and this interfacial strain distorts the O-Si-O bonds and becomes an easy prey for the injected hot electrons or holes. This electrons or holes break these spots faster in S2 than in S4 reaching the breakdown of the device [9, 10]. The reason for the increased reliability seen in S4 is explained as the presence of Ge in the gate [30]. The presence of Ge could be reducing strain and the formation of bias dependent trap densities.

The columnar structure of the poly-material may introduce a relatively high-compressive macroscopic stress, due to the existence of a preferred growth orientation [14]. Generally, the stress in a thin film is composed of a thermal stress and an intrinsic stress [31].



The thermal stress on the poly-Si deposited on oxidized silicon substrate is tensile, and the intrinsic stress in poly-Si is compressive. Since the thermal stresses are negligible compared with the intrinsic stresses, the stress on poly-Si thin film is generally considered to be compressive. Based on deformation mechanism maps (DMMs) constructed for thin films, it is suggested that the yield limit of poly Si films is characterized by the plastic strain rate and the deformation is controlled by the grain boundary and dislocation climb mechanism [32]. Therefore, as the average grain size of the poly-Si increase, the stress decreases. Poly-Si<sub>1-x</sub>Ge<sub>x</sub> alloys have a lower melting point than poly Si. As a result, the grain growth tends to occur at a lower temperature than in poly Si [33]. Thus the poly-Si<sub>1-x</sub>Ge<sub>x</sub> suffers less stress than the poly-Si, especially with growth resulting in larger grain size. It is to be observed that the larger the grain size, the less grain boundary length and grain boundary. This provides a lower electrical resistivity because of a reduction in the trapping of charge carriers and of the formation of potential barriers at grain boundaries [34]. The above discussion is very consistent with the observation of the local strain field at the lower Si/SiO<sub>2</sub> interface for different poly-Si<sub>1-x</sub>Ge<sub>x</sub>/SiO<sub>2</sub>/Si (Fig. 6).

## Conclusion

In summary, the microstructure of poly-Si<sub>1-x</sub>Ge<sub>x</sub>/SiO<sub>2</sub>/Si having ultra thin oxides of 2.0-3.0 nm and Ge fraction of  $x = 0, 0.2, \text{ and } 0.35$  is performed. Moreover, the local strain at the SiO<sub>2</sub>/Si lower interface is monitored using large angle CBED in TEM. The powerful two-dimensional reciprocal space mapping technique was then used to complement and confirm this observation. A consistency was obtained from monitoring the local interface strain at the different samples using the two techniques. Increasing the Ge fraction leads to an increase of the grain size and consequently reducing the stress in the poly-gate material. This in turn will affect the under lying thin oxide and its interface strain with Si. In addition, and from HR-XRD oxynitrides was observed to yield interfaces with lower defect density.

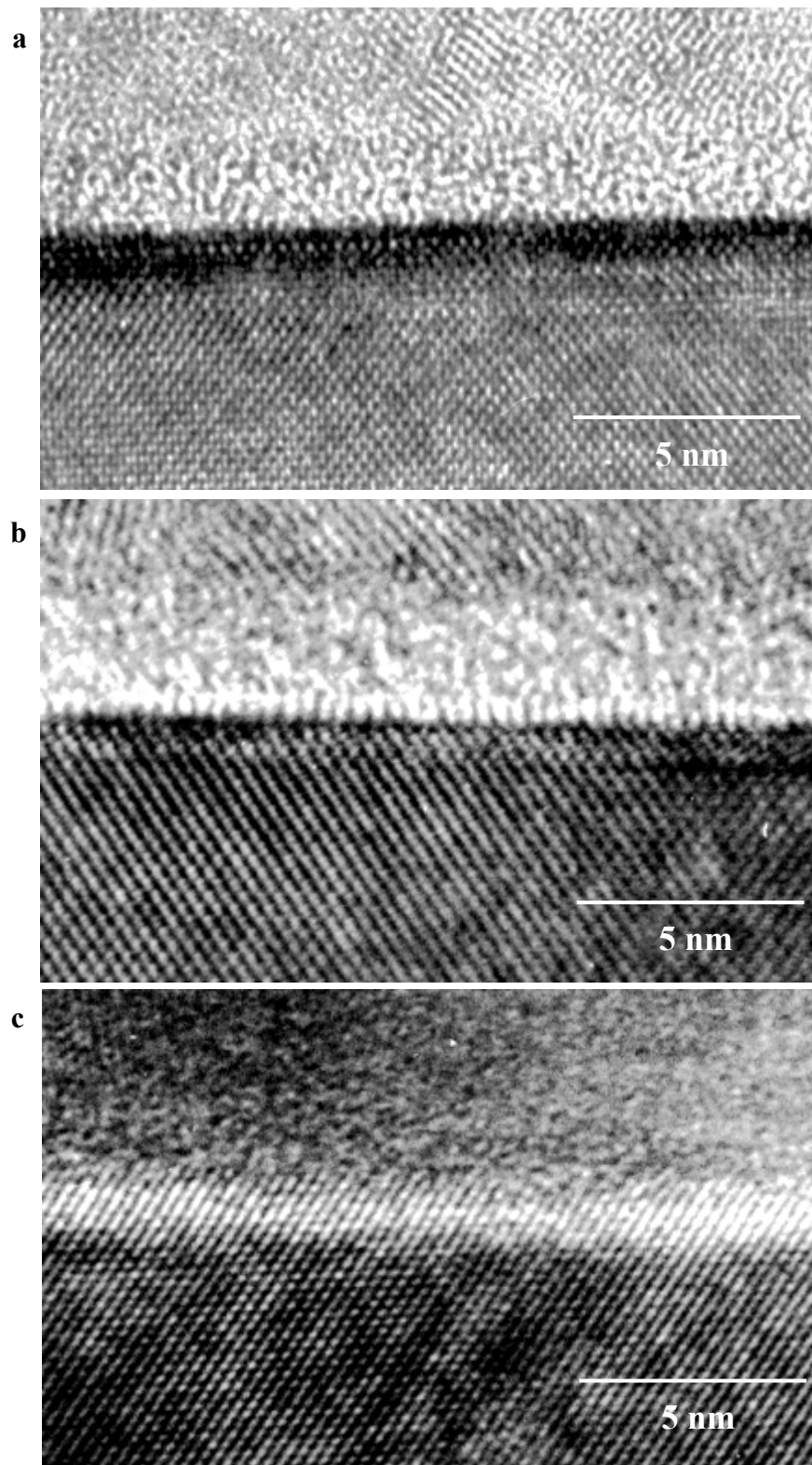
<b>Sample No.</b>	<b>Ge Content</b>	<b>Gate doping/ Thickness</b>	<b>Remarks for Oxidation</b>
S1	0	B <sup>+</sup> ; 1 x 10 <sup>20</sup> ; 200 nm	Without nitridation
S2	0	B <sup>+</sup> ; 1 x 10 <sup>20</sup> ; 200 nm	With nitridation
S3	0.20	B <sup>+</sup> ; 1 x 10 <sup>20</sup> ; 200 nm	With nitridation
S4	0.35	B <sup>+</sup> ; 1 x 10 <sup>20</sup> ; 200 nm	With nitridation

Table 1: Specifications for oxide and poly-Si<sub>1-x</sub>Ge<sub>x</sub> deposition

<b>Sample No</b>	<b>Oxide Thickness from HREM (nm)</b>	<b>Oxide thickness from C-V measurement (nm)</b>
S1	2.7 ± 0.2	2.3 ± 0.1
S2	3.2 ± 0.2	3.0 ± 0.1
S3	3.2 ± 0.2	3.0 ± 0.1
S4	3.6 ± 0.2	3.0 ± 0.1

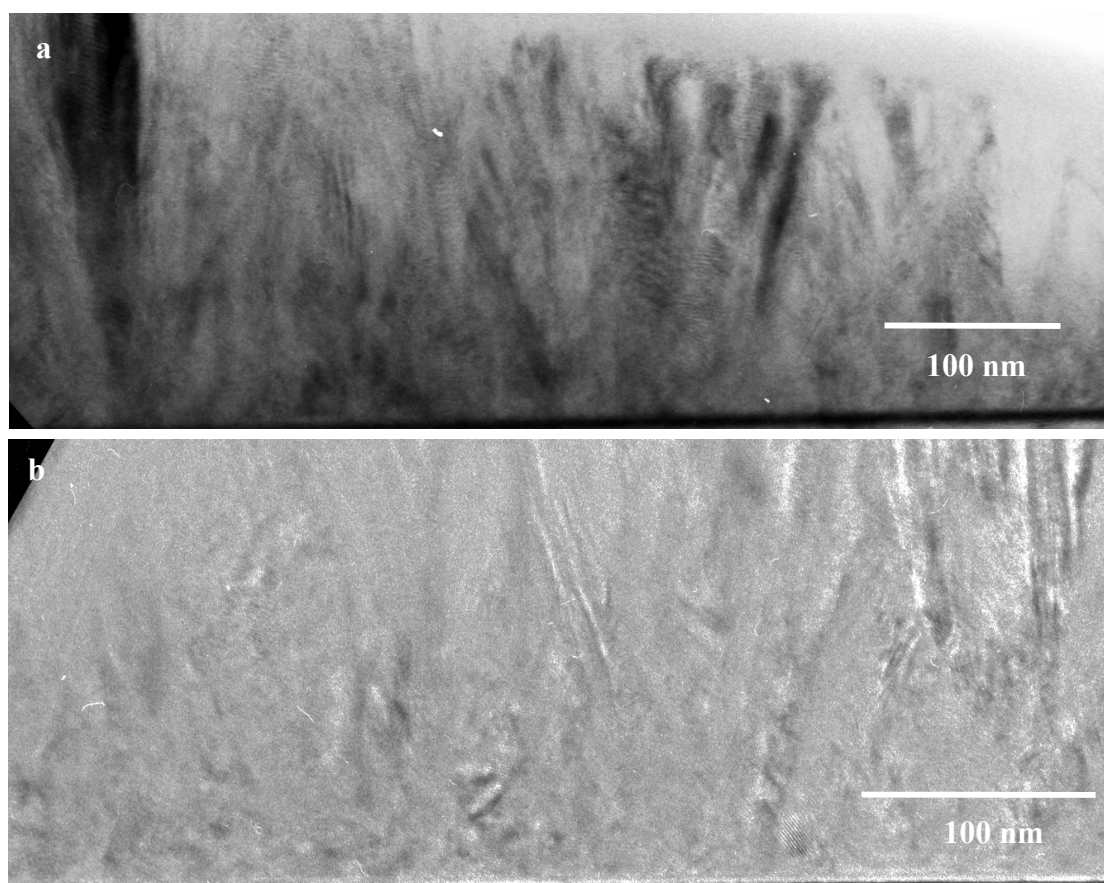
Table II- Oxide thickness from HREM and electrical measurement

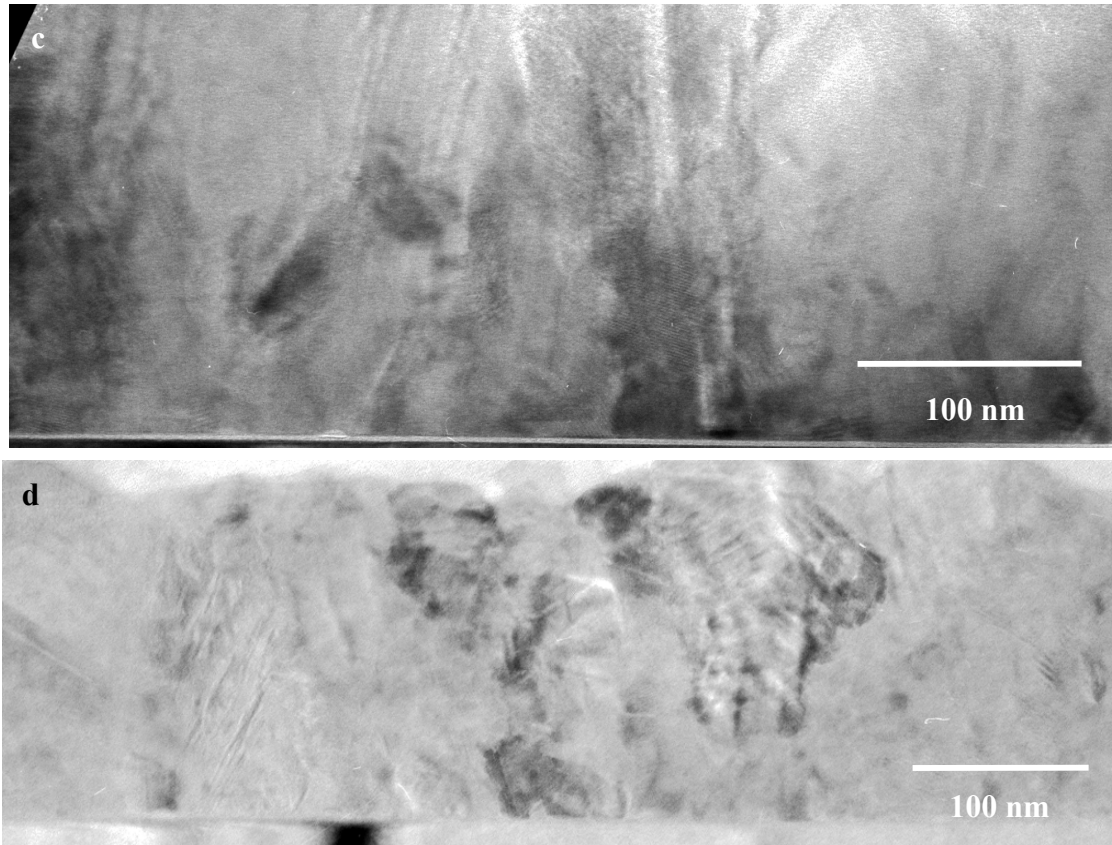




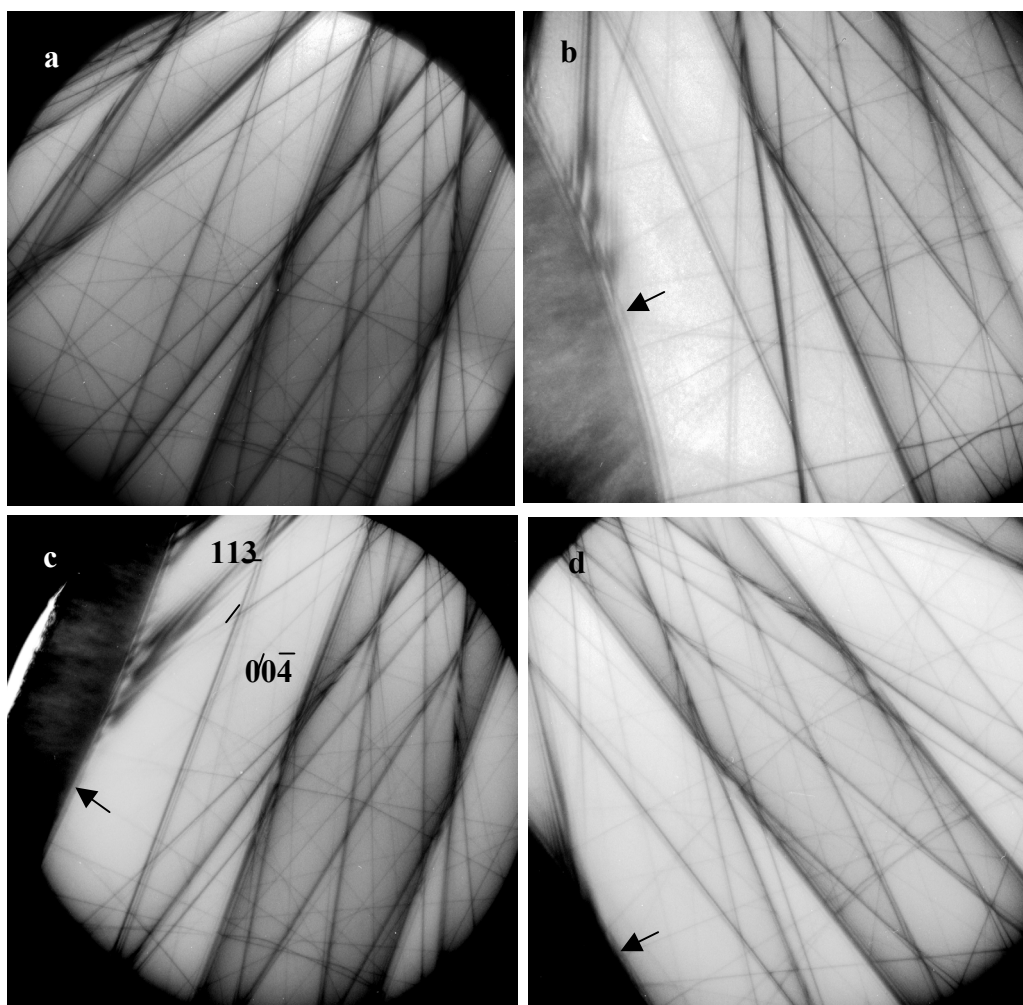


**Figure 1:** High resolution cross-sectional TEM of Si/SiO<sub>2</sub>/poly-Si<sub>1-x</sub>Ge<sub>x</sub>.  
 (a) sample S1, (b) sample S2, (c) sample S3 and (d) sample S4.

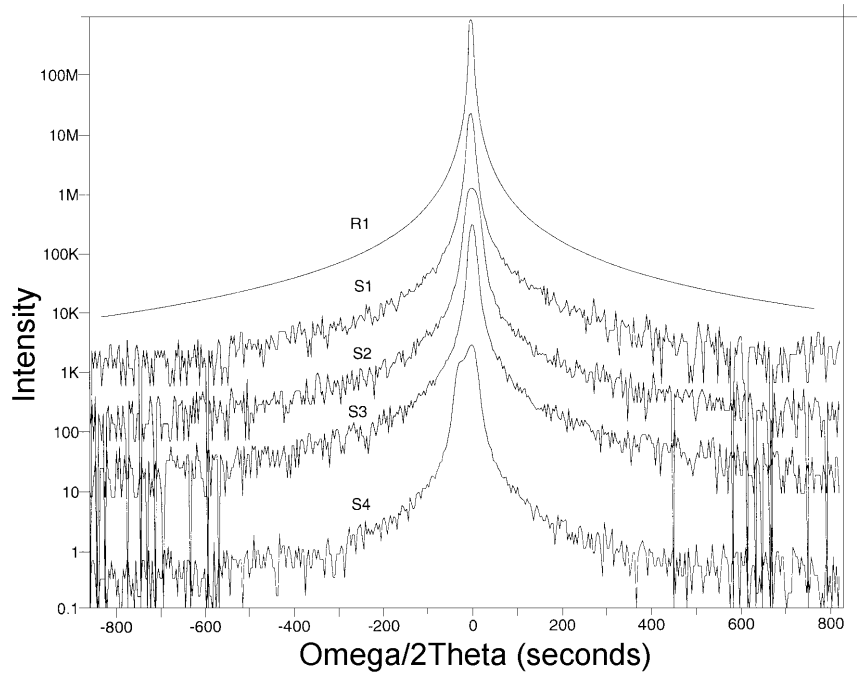




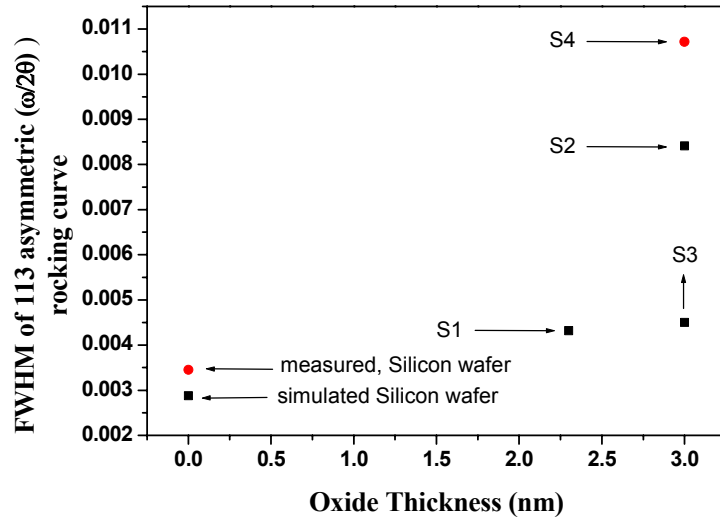
**Figure 2:** TEM micrograph of polySi<sub>1-x</sub>Ge<sub>x</sub>. (a) Sample S1, (b) Sample S2, (c) Sample S3 and (d) Sample S4.



**Figure 3:** Large angle convergent beam patterns from Si/SiO<sub>2</sub> interface. The arrows show the Si/SiO<sub>2</sub> interface. (a) the area far away from the interface, (b) sample S1, (c) sample S2 and (d) sample S4.

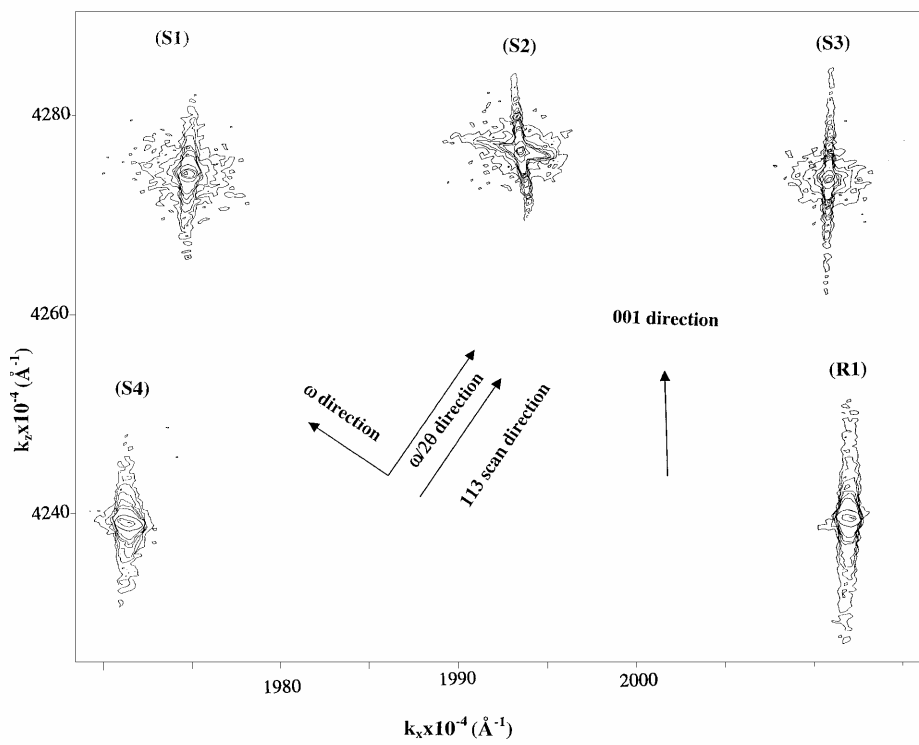


**Figure 4:** The 113 asymmetric HR-RC of all the samples S1-S4 and R1.

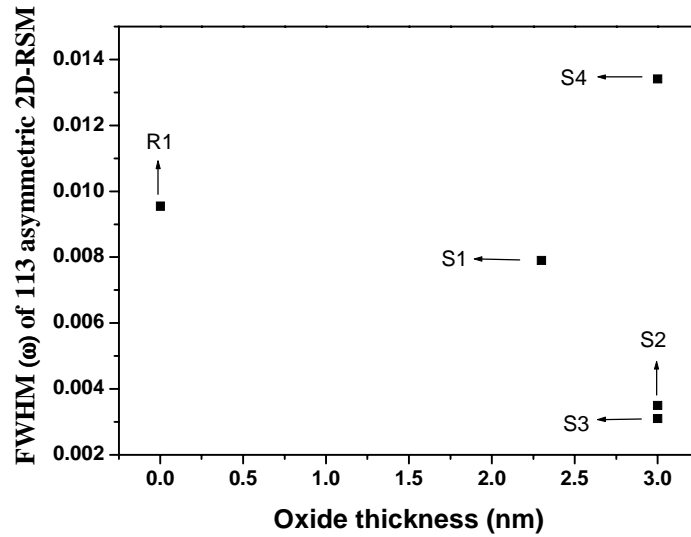


**Figure 5:** The FWHM obtained from the 113 HR-RC of all samples as function of the oxide thickness including a simulated case for a Si wafer.





**Figure 6:** A typical 2D-RSM around the 113 asymmetric reciprocal lattice points for all the samples S1, S2, S3, S4, and R1. The iso-intensity contours are for 14200, 7100, 3000, 350, 50, 20, 10, 5 and 2 counts/seconds.



**Figure 7:** Summary of the FWHM along the  $\omega$ -scan direction obtained from the 113 asymmetric 2D-RSM for all the samples.

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# Paper III

Ultrathin Oxynitridation Process Through Ion  
Implantation in a Poly-Si<sub>1-x</sub>Ge<sub>x</sub> Gate MOS Capacitor



# **Ultrathin Oxynitridation Process through Ion Implantation in a Poly-Si<sub>1-x</sub>Ge<sub>x</sub> Gate MOS Capacitor**

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## **Abstract**

The effect of temperature and time of heat treatment on the distribution of ion implanted nitrogen in poly-Si<sub>0.65</sub>Ge<sub>0.35</sub> gate MOS samples was studied. Secondary ion mass spectrometry (SIMS) was used for the qualitative analysis of the nitrogen distribution. Rapid thermal processing was done for a temperature range of 950 to 1070 °C for the re-distribution of ions. Our nitrogen implantation doses were  $5 \times 10^{14} \text{ cm}^{-2}$ ,  $2 \times 10^{15} \text{ cm}^{-2}$  and  $5 \times 10^{15} \text{ cm}^{-2}$ , all with implantation energy of 50 keV. For a uniform distribution of nitrogen in the SiO<sub>2</sub> region, an optimal temperature at a well calibrated time must be applied and this depends on the implantation dose. For medium and high concentrations the optimal conditions were 1050 °C and 15 second, and 1070 °C and 15 seconds, respectively. A uniform nitrogen distribution could be obtained throughout the SiO<sub>2</sub> film. Prolonged heat treatment can cause degradation of the oxide layer and movement of the nitrogen and oxygen into the channel and the poly-Si<sub>0.65</sub>Ge<sub>0.35</sub> layer.

## Introduction

Boron diffusion is found as a companion of scaling in poly gated p-MOS transistors [1,2]. The diffusion of boron into the channel region can not only change the capacitance characteristics of an MOS device but also reduces its reliability [1,2]. The solution to this problem is to either use silicon nitrides or to nitridate the  $\text{SiO}_2$  [3]. Another option could be to use an alternate high-K dielectric material [4]. Though using an alternate dielectric material is seen as a promising approach, the process compatibility of the materials with silicon is a complicated issue [4,5]. Thus, nitridation becomes the only immediate solution for the oxides [3]. There are several approaches to incorporate nitrogen in an oxide like furnace oxidation, rapid thermal oxidation (RTO), downstream plasmas [6,7] and nitrogen ion implantation. Though nitrogen ion implantation is a relatively new approach, it is seen as a promising processing step [8,9]. Among these growth methods, furnace oxynitridation, RTO and plasma nitridation either use nitrous oxide ( $\text{N}_2\text{O}$ ) [6] or Nitric oxide (NO) [10] or mixtures of nitrogen and oxygen gas to incorporate nitrogen [11].  $\text{NH}_3$  nitridation of the gate oxides is also studied extensively [12]. The thermal oxynitrides is seen to have a roughly uniform nitrogen distribution throughout the film in  $\text{NH}_3$  process, while RTO process accumulates the nitrogen at the  $\text{SiO}_2/\text{Si}$  interface or at the surface of  $\text{SiO}_2$  [6]. The  $\text{NH}_3$  gas mixture incorporates a maximum amount of nitrogen, while NO and  $\text{N}_2\text{O}$  incorporates comparatively fewer amounts of nitrogen [13]. An advantage of NO over  $\text{N}_2\text{O}$  is that higher drain current is observed for NO oxynitridated transistors [14]. The drawback of using  $\text{NH}_3$  is that the hydrogen is also incorporated along nitrogen and upon biasing the hydrogen migrates to the interface and acts as trap centres paving the way to its breakdown [15]. Nitridation by ion implantation is a relatively new process. Here nitrogen incorporation is performed by implanting  $\text{N}^+$  or  $\text{N}_2^+$  either into the silicon wafer prior to oxidation or directly into the grown oxides. The advantage of using nitrogen implantation is the feasibility in having the desired nitrogen dose in the oxides. The amount of nitrogen in the oxide depends on the nitrogen implantation dose. Though there are some studies done on nitridation by ion implantation into poly-Si gate electrode structures, this is the first time such a study is being conducted on structures with poly- $\text{Si}_{1-x}\text{Ge}_x$  gate electrodes.

In this work, the effects of time and temperature of heat treatment on the distribution of ion implanted atomic nitrogen (N) into poly- $\text{Si}_{0.65}\text{Ge}_{0.35}$  gate structures were studied. The

studies show that an optimal time and temperature have to be applied in order to obtain a nitrogen free poly-Si<sub>1-x</sub>Ge<sub>x</sub> (x = 0.35) gate electrode. Under these conditions the nitrogen is totally redistributed into the SiO<sub>2</sub> layer. The amount of nitrogen in the oxide depends on the nitrogen implantation dose.

## Experiments:

PMOS capacitors were fabricated on 0.142-Ωcm (100) n-type Si wafers from Wacker Siltronic. An ultrathin SiO<sub>2</sub> film of 2.5 nm was grown at 750-800 °C using an ASM A400 vertical furnace. A 200 nm thin film of poly-Si<sub>1-x</sub>Ge<sub>x</sub> (x = 0.35) was then deposited in an LPCVD ASM system. The gaseous precursors were SiH<sub>4</sub> and GeH<sub>4</sub>. They were deposited at a temperature of 615 °C and 640 °C respectively at a pressure of 40 torr. A Si seed layer with a nominal thickness of 1 nm was deposited at 615 °C prior to the poly-Si<sub>1-x</sub>Ge<sub>x</sub> layer deposition. This was done to facilitate the nucleation of poly-Si<sub>1-x</sub>Ge<sub>x</sub> on the SiO<sub>2</sub>. Varying the SiH<sub>4</sub> flow at a fixed GeH<sub>4</sub> flow controlled the Ge content. The thickness of the gate layers was 200 nm according to optical Tencor Spectra map measurements and high resolution transmission electron microscopy (HRTEM) measurements.

Atomic nitrogen (N) ions were implanted by using a Varian DF4 ion implanter. The implantation energy was 50 keV which places the peak of the N distribution in the middle of the Si<sub>1-x</sub>Ge<sub>x</sub> gate. The N distribution was estimated by simulation program TRIM prior to the implantation and confirmed by the SIMS measurement after the implantation. Three similar samples were implanted with an ion dose of 5 x 10<sup>14</sup> cm<sup>-2</sup>, 2 x 10<sup>15</sup> cm<sup>-2</sup> and 5 x 10<sup>15</sup> cm<sup>-2</sup>. The samples were then annealed at temperatures ranging from 950 to 1070 °C for a time span of 5 to 60 seconds.

For analysis of nitrogen distribution, CAMECA ims 6f, was used for SIMS technique. Cesium ions, accelerated by 10 kV, were used as primary ions. The primary current ranged from 20 to 30 nA. Prior to the analysis, the samples were kept for one day in a high vacuum at 50 °C. The vacuum during the analysis was 4 x 10<sup>-10</sup> mbars. As secondary ions O<sub>16</sub>, Si<sub>30</sub> and Ge<sub>72</sub> isotopes were analysed. For determination of nitrogen distribution secondary ions SiN<sub>42</sub> were analysed. The depths of the craters were measured with a tallysurf technique.



## Results

Figure 1 shows a sequence of SIMS analyses of samples obtained from the nitrogen implanted poly-Si<sub>0.65</sub>Ge<sub>0.35</sub>/SiO<sub>2</sub> test block structure. The implantation dose of nitrogen is the medium one,  $2 \times 10^{15} \text{ cm}^{-2}$ . Figure 1a gives the SIMS analysis of an as implanted sample. The nitrogen analysis show that the nitrogen is mainly implanted in the poly- Si<sub>0.65</sub>Ge<sub>0.35</sub> region and in the SiO<sub>2</sub> layer, having the peak in the poly Si<sub>0.65</sub>Ge<sub>0.35</sub> region. A part of the implanted nitrogen has also penetrated through the thin oxide region into the channel. Further, profiles of germanium, silicon and oxygen are shown. The SiO<sub>2</sub> layer is indicated by the large peak in the concentration profile of oxygen. The width of this peak is much larger than the thickness of the silicon dioxide film. The broadening of the peak is an artifact caused by the mode of analysis in which the SIMS instrument was employed. As mentioned above Cs ions were used as primary ions to analyse the oxygen. The broadening is caused by the high acceleration energy of the primary ions, 10 kV, and the acceleration energy cannot be lowered significantly to obtain a realistic thickness of the oxide layer [16]. On the other hand, the aim of the investigation was to study qualitatively the effect of heat treatments on the nitrogen distribution. The oxygen profile shows a tail going in to the channel material and this is partly due to the artefact caused during the sputtering technique. The analysis was done by continuously sputtering all three materials, starting from the poly- Si<sub>1-x</sub>Ge<sub>x</sub> towards the Silicon channel.

Figure 1b shows the SIMS spectrum of the sample treated at 1050 °C for 10 seconds. It is seen that upon annealing, a large change in the nitrogen concentration profile occurs in the SiO<sub>2</sub> dielectric region. The nitrogen in the poly- Si<sub>0.65</sub>Ge<sub>0.35</sub> region and the silicon channel region shows a tendency to concentrate in the region of higher oxygen concentration. The larger concentration of nitrogen seen in the surface of the film could be due to the artefact during sputtering. In the poly- Si<sub>0.65</sub>Ge<sub>0.35</sub> region, the concentration of nitrogen is still high. The implantation peak indicates that the nitrogen movement has not been completed. In this region, the oxygen profile indicates that a reaction between the nitrogen and oxygen has taken place. The profiles follow each other and the oxygen shows enhanced yield compared with the profile in Fig.1a. The concentrations of Si and Ge are not influenced by the changes in oxygen and nitrogen distributions.

Figure 1c shows the SIMS spectrum of the sample annealed for 15 seconds at 1050 °C. It is seen that this time is long enough for a complete redistribution of the nitrogen in the SiO<sub>2</sub> region. The profile indicates that the nitrogen has now concentrated in the silicon dioxide film. Even in this spectrum, the nitrogen and oxygen profiles follow each other and are validating the previous figure. The analysis further shows that the concentration of oxygen and nitrogen in the poly- Si<sub>0.65</sub>Ge<sub>0.35</sub> gate electrode was reduced drastically. This region has been depleted of the oxygen, compared to the analyses shown in Fig.1a and Fig.1b. Thus, it can be concluded that the oxygen and nitrogen moved together and have concentrated in the silicon dioxide layer. This should cause a broadening of the oxide film due to the volumetric expansion, but this effect cannot be detected by the type of analysis used in this investigation.

A sufficiently higher temperature of heat treatment than the optimal temperature of 1050 °C for 15 seconds does not have any impact on the distribution of the oxygen and nitrogen. However, deleterious effects on the sample can be observed when it is annealed for a much longer time (i.e., 60 seconds). Figure1d shows the spectrum of the sample annealed at 1050 °C for 60 seconds. The silicon dioxide peak has been strongly broadened showing dissociation of oxygen and nitrogen and they move in to the channel and the poly- Si<sub>1-x</sub>Ge<sub>x</sub> regions. Upon dissociation, the oxygen and nitrogen are found to move together into the poly- Si<sub>0.65</sub>Ge<sub>0.35</sub> gate electrode and their profiles are found to meet together. But the diffusion of oxygen into the channel region is found to be faster than that of nitrogen. This is in contrast to the previously obtained results for the diffusion process in a furnace oxynitride MOS system [17]. Since nitrogen is the lighter atom, it is expected to diffuse faster. Also, Si-O bonds are much stronger than Si-N bonds and therefore it should be much more difficult to be broken.

By decreasing the temperature of the heat treatment of the samples with the medium implantation of nitrogen to 1000 and 950 °C, the SIMS analysis gave a broadening in the silicon oxide film region. Fig.2 shows SIMS analysis of a sample heat treated at 1000 °C for 10 seconds. The concentration profiles of oxygen and nitrogen have the same features as those profiles presented in Fig.1b and 1c. Due to this effect the samples with medium and high nitrogen concentrations were heat treated only at 1050 and 1070 °C, respectively.

Figure 3 gives the SIMS spectrum of the samples with high ( $5 \times 10^{15} \text{ cm}^{-2}$ ) nitrogen implantation dose. Fig. 3a gives the SIMS analysis of the as implanted sample. Compared to

the medium concentration implant, here much larger part of the implanted nitrogen is present in the channel. An analysis of a sample heat treated at 1070 °C for 15 seconds is shown in Fig. 3b. This analysis indicates that the same reaction as in the medium case has occurred, the large amount of nitrogen has moved from the channel and the poly-  $\text{Si}_{0.65}\text{Ge}_{0.35}$  into the silicon dioxide film. The profiles of the oxygen and nitrogen have the same features as the profiles in analyses of the samples with medium nitrogen concentration. It can be noted that the peak in the oxygen profile, representing the silicon dioxide film, exhibits almost no tail on the channel side. When treated at 1050 °C, a longer time (20 seconds) is necessary to apply in order to obtain a complete redistribution of the nitrogen into the silicon oxide film.

Figure 4a gives the sequence of analyses for the sample with low ( $5 \times 10^{14} \text{ cm}^{-2}$ ) nitrogen implantation concentration. The analysis of the as implanted sample is shown in Fig. 4a. Fig. 4b shows analyses of samples heat treated at 1000 °C for 15 seconds. The profiles of oxygen and nitrogen exhibit the same features as in the analyses of samples with medium and high nitrogen concentrations. In the case of low nitrogen concentration, the sample can be heat treated at a lower temperature for a shorter time.

## Conclusions

We have successfully implanted and processed nitrogenated oxides for fabricating an MOS capacitor. The nitrogen ion dose in the dielectric region can be varied by implanting different nitrogen dose and through the requisite post implantation heat treatment. Under optimal conditions of temperature and time the implanted nitrogen is completely redistributed into the silicon oxide film. The analyses indicate that during the heat treatment a reaction between nitrogen and oxygen probably occurs. Further, the investigation shows that nitrogen is strongly bound in the silicon dioxide film. Additional heat treatment does not cause nitrogen diffusion out from the film. The optimal temperature and time can be adjusted according to the nitrogen concentration. In the poly- $\text{Si}_{1-x}\text{Ge}_x$  sample used for this study, it is found that by keeping a time constant of 15 seconds, the optimum temperatures were found to be 1000, 1050 and 1070 °C for low, medium and high concentrations of the implanted nitrogen. Prolonged heat treatments and higher temperatures can create damage in the silicon dioxide film

## Figures

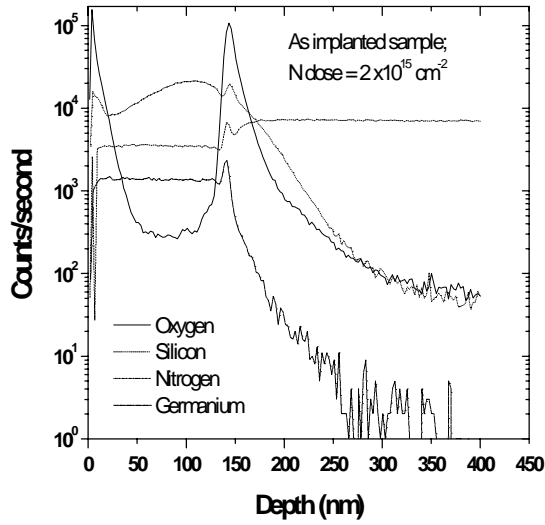


Fig. 1-a

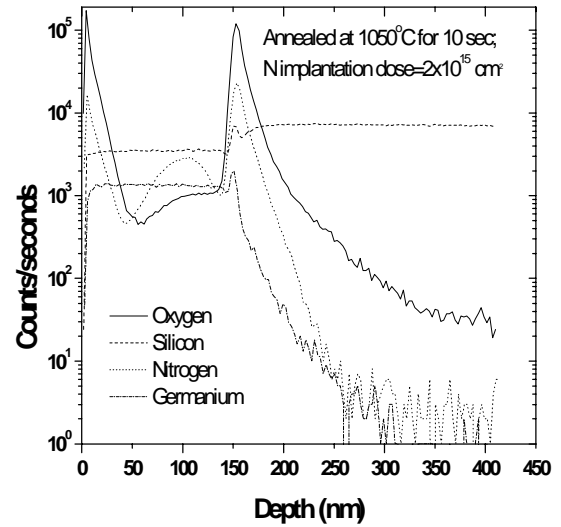


Fig. 1-b

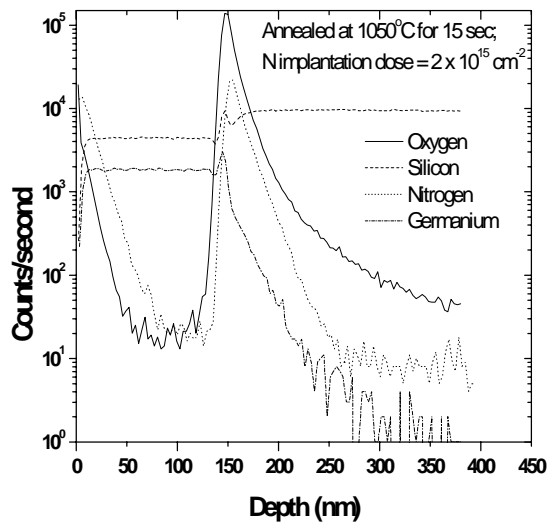


Fig. 1-c

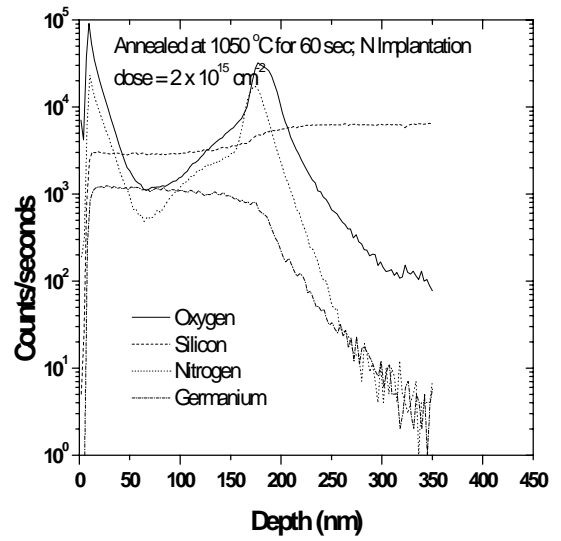
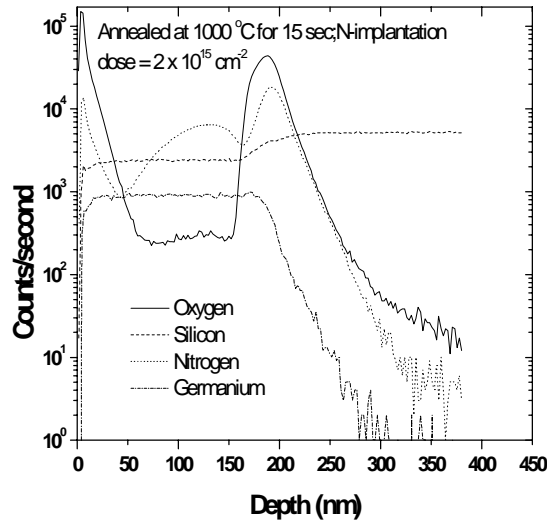


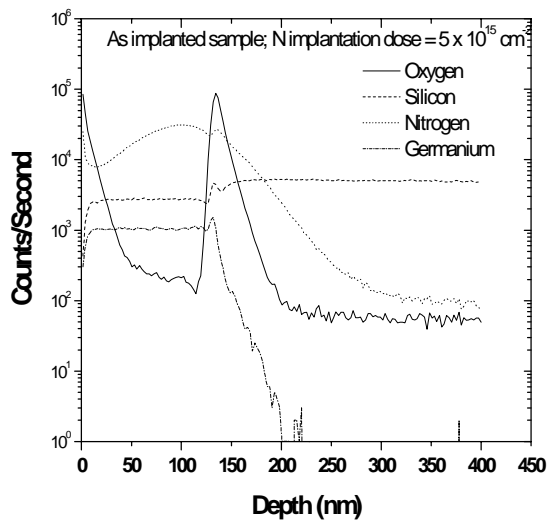
Fig. 1-d

Figure 1 a-c: shows a sequence of SIMS analysis for an implantation dose of  $2 \times 10^{15} \text{ cm}^{-2}$ .

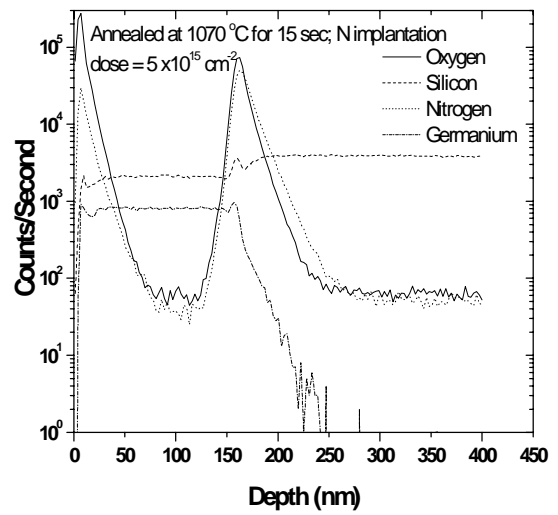


**Fig. 2**

**Figure 2:** SIMS analysis of the sample with N implantation dose of  $2 \times 10^{15} \text{ cm}^{-2}$  and heat treated at 1000 °C for 15 seconds



**Fig. 3 a**



**Fig. 3 b**

**Figure 3 a –b:** sequence of SIMS analysis of the sample with N dose of  $5 \times 10^{15} \text{ cm}^{-2}$ .

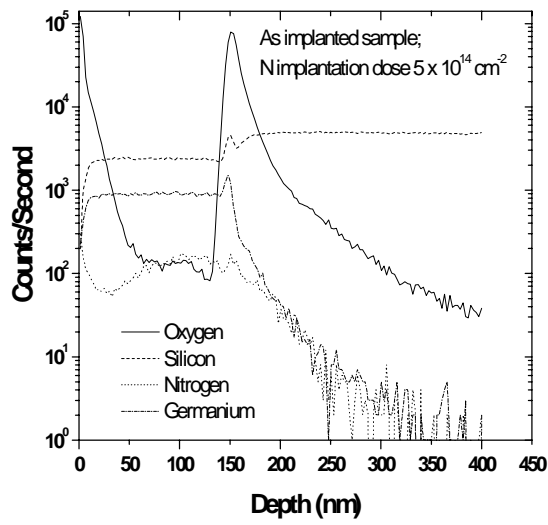


Fig. 4 a

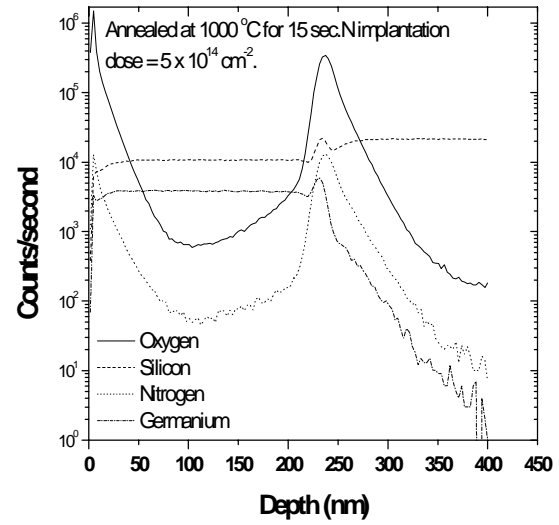


Fig. 4 b

Figure 4 a-b: sequence of SIMS analysis for an implantation dose of  $5 \times 10^{14} \text{ cm}^{-2}$

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# Paper IV

Relaxation Properties of Tensile Strained  
 $\text{Si}_{1-x}\text{Ge}_x$  Uninterrupted Over Growth on Fully  
Relaxed Ge on Si 001



# **Relaxation Properties of Tensile Strained Si<sub>1-x</sub>Ge<sub>x</sub> Uninterrupted Over Growth on Fully Relaxed Ge on Si 001**

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## **Abstract**

We have investigated the relaxation properties of a tri-layer consisting of tensile strained SiGe grown over a fully relaxed Ge on Si 001 in an uninterrupted growth sequence. The uninterrupted growth was accomplished using chemical vapour deposition (CVD). High-resolution x-ray rocking curves (HR-RC) and two-dimensional reciprocal space mapping (RSM) were employed as the main characterization tool. Secondary ion mass spectrometry (SIMS) was used for chemical analysis for complementary measurement. A reference sample (B1) with only 1.5  $\mu\text{m}$  thick fully relaxed Ge was first characterized. A second batch of two samples (B2 and B3), with an extra top 1.0  $\mu\text{m}$  tensile strained Si<sub>1-x</sub>Ge<sub>x</sub> ( $x = 0.79$  for B2, and 0.74 for B3), were grown at slightly higher temperature compared to the initial Ge layer. For this tensile strained Si<sub>1-x</sub>Ge<sub>x</sub>, we have varied the Si flux, where it was doubled for B3 compared to B2. The variation of the Si flux was found to influence slightly the  $x$  fraction and a more pronounced variation of the tensile strain can be observed between B2 and B3. Moreover, all the lattice parameters were accurately extracted. For the bottom initially grown Ge, the derived lattice parameters for both the in- and perpendicular to plane, were extremely close to the bulk tabulated value of intrinsic Ge layer, indicating that a rather high quality pure fully relaxed Ge layers were resulted. From an initial estimation of the linear density of misfit

dislocations at the interface, we found that the linear density of misfit dislocation is lower at the upper interface than the lower interface. This implies that, with the adapted growth approach, high quality tensile strained  $\text{Si}_{1-x}\text{Ge}_x$  epitaxial layer can be obtained.

## Introduction

Epitaxially grown relaxed  $\text{Si}_{1-x}\text{Ge}_x$  and Ge structures are widely used as virtual substrates. The proposed advantage of these structures is either to grow strained Si or  $\text{Si}_{1-x}\text{Ge}_x$  layers or to integrate Si technology with optoelectronic devices [1,2,3,4]. Field effect transistors made of strained Si are found to have higher mobility (~70% increase in mobility) [5,6]. Indeed the epilayer growth of Ge and  $\text{Si}_{1-x}\text{Ge}_x$  itself can be used to make photodiodes. One of the problems that hinder the growth of these epilayers is the dislocations that originate due to the misfit strain [7]. These threading dislocations can even penetrate to the surface of the grown epilayer. Due to the misfit strain, an increase in surface roughness and generation of crosshatch pattern is also seen along with the dislocations.

Though Si and  $\text{Si}_{1-x}\text{Ge}_x$  layers grown on  $\text{Si}_{1-x}\text{Ge}_x$  have not yielded the theoretically set target, reports have shown that  $\text{Si}_{1-x}\text{Ge}_x$  grown on Ge substrates gives much better mobility values. This is because, the epitaxially grown Si and  $\text{Si}_{1-x}\text{Ge}_x$  on Ge substrates carries tensile strain. The tensile strain can be used to tailor the band structure of the device. Another advantage could be the integration of Ge infrared detectors with VLSI devices. So far, the published reports have been concentrated towards the growth of  $\text{Si}_{1-x}\text{Ge}_x$  epitaxial layers on Ge single crystals substrates. In addition, relaxed Ge lattice constant matches GaAs and some other III-V semiconductors. This implies these virtual substrates can in fact facilitate a route for integrating III-V photonic advantages into silicon technology. For the integration of III-V semiconductors on silicon technology for photonic applications, it was demonstrated that an improvement of the III-V semiconductors can be achieved via the growth on tensile strained- $\text{Si}_{1-x}\text{Ge}_x$  grown on relaxed Ge or on tensile strained-Si grown on relaxed Ge on Si rather than directly grown on relaxed Ge on Si [8].

In this paper, we characterize tensile strained  $\text{Si}_{1-x}\text{Ge}_x$  virtual substrates over-growth on fully relaxed Ge which was grown directly on Si 001. High resolution X-ray diffraction measurements were done to characterize the quality of these structures. Chemical analysis (SIMS) was performed to correlate the x-ray results. Our studies show that the adapted growth

procedure have resulted in growing high quality Ge layers and the  $\text{Si}_{1-x}\text{Ge}_x$  layers grown on these Ge layers also show higher quality with no measurable layer misorientation.

### **Experiment:**

The growth technique (single direct Ge epitaxy) of the present samples (B1-B3) was performed on 200 mm Si001 wafers in a commercial advanced semiconductor material chemical vapour deposition chamber (ASM-CVD) at STMicroelectronics, France. This growth technique uses  $\text{SiH}_4$  and  $\text{GeH}_4$  as gaseous precursors and  $\text{H}_2$  as the carrier gas. In contrast to previous reported similar growth, we do not use ultra-high vacuum UHV-CVD systems, although we still use an equivalent process temperature (600 °C to 750 °C). Our CVD with built in commercial mass-flow meters permits processing with partial pressure well above what is used in UHV-CVD (in the 10 Torr range). This results in growth rate of more than 3  $\mu\text{m}$  in less than 15 minutes. In addition, the advent of better growth control in our chamber, and improved technological steps in the fabrication line at STMicroelectronics, namely the quality of the pre-cleaning step and surface preparation prior to the heteroepitaxy, the chemical quality of the gaseous species of the all add up to much better cleanness during processing.

In this work, we first realize a high quality 100% germanium layer of 1.5  $\mu\text{m}$  thick (sample B1), followed by 1  $\mu\text{m}$  thick layer of silicon germanium (tensile strained  $\text{Si}_{1-x}\text{Ge}_x$ , samples B2 and B3). However, sample B3 during the growth was exposed to twice the silicon flux compared with sample B2. Thus having established first a template of good quality 1.5  $\mu\text{m}$  thick germanium deposition with surface finishing, we here investigate and compare further the deposition of 1  $\mu\text{m}$   $\text{Si}_{1-x}\text{Ge}_x$  layers. Secondly, we study the influence of silicon flux for cases of strained  $\text{Si}_{1-x}\text{Ge}_x$ . It should be noted that the tensile strained layers were grown at slightly higher temperature compared to the 1.5  $\mu\text{m}$  fully relaxed Ge grown initially.

The present structural evolution study was performed by high-resolution X-ray diffraction measurement. High-resolution rocking curves (HR-RCs) and two-dimensional reciprocal space maps (2D-RSMs) were performed on these heterostructures. We have employed a multi-crystal high resolution Philips Extended X-pert material Research Diffractometer, equipped with a computer-controlled motorized goniometer. This diffractometer enables the optimization of the scattering angles with angular step sizes down

to  $1.0 \times 10^{-3}$  degrees for the angles of incidence and reflection, and step sizes down to  $1.0 \times 10^{-2}$  degrees for the angles of rotation around the surface normal and around the in plane horizontal directions. Both double crystal and triple axis configurations were employed. A four crystal Ge (220) Bartels monochromator is used to collimate the Cu-tube x-ray incident beam with a divergence of 12 arc sec, and for secondary optics, the rocking curves were collected using a slit with a width of 0.5 degree. For collecting the 2D-RSMs, the diffractometer was set into the extended configuration and a combination of mirror and a Bartels monochromator was used. The addition of a mirror is necessary as it increases the intensity by at least an order of magnitude while still maintaining a low background noise level. SIMS analysis was done using CAMECA ims 6f equipment. Cesium ions were used as the primary ions at an accelerated potential of 10 KV. The primary current was around 40 to 50 nA.  $\text{Si}_{30}$  and  $\text{Ge}_{74}$  were analyzed as the secondary ions.

## Results and Discussions:

Symmetric and asymmetric 2D-RSMs for all samples have been performed; in addition high HR-RC was also collected for all samples (B1, B2, and B3). All samples have been collected with the same acquisition parameters. This is important because qualitative comparison between different samples is straightforward. Figure 1 a-b shows a typical symmetric and asymmetric 2D-RSM of the reference sample (B1). By using the symmetric 2D-RSM and looking at the peaks position in  $\omega$  we can determine relative layer tilts (misorientation). It is seen that the substrate and layer peak lie in the same straight line along the surface normal in this case (vertically in reciprocal lattice axis units  $k_x$  parallel to surface and  $k_z$  normal to it). It follows from Fig 1a that there is relatively small miscut and crystallographic tilts between the substrate and the grown fully relaxed Ge layer. It is clearly seen that there is an asymmetric elongation of the low intensity contours of the layer peak along the 001 direction both in the 004 and the 113 reciprocal lattice points. From Fig. 1b, it is clearly seen that the line joining the substrate and the layer peak is parallel to the  $\omega/2\theta$  scan direction. This indicates a high relaxation degree [9]. By looking into the peak position of the asymmetric curve we can calculate the lattice parameters, the Ge fraction, and the relaxation level. The procedure we have followed is described in [10]. Indeed the relaxation factor is extracted for this sample as well as for all other sample. The extracted relaxation level for the Ge layer was indicating full relaxation. The lattice parameters extracted where  $5.6479 \pm 0.0001$

Å, and  $5.6624 \pm 0.0001$  Å for the parallel and the perpendicular directions, respectively. These lattice parameters have less than 0.2% difference compared to the standard well tabulated value for the Ge having the value of 5.64613 Å [11]. The Ge fraction was found to be  $0.987 \pm 0.005$ , in consistency with the intended growth of a pure Ge layer and the SIMS chemical analysis of sample B1 showing a pure top Ge layer (Fig. 2). In addition, the relaxation factor was found  $0.993 \pm 0.002$  implying that a fully relaxed Ge layer was achieved. This was also the same order of magnitude for the parameters obtained for the Ge peaks for the other samples (B2 and B3). The extracted misorientation of this fully relaxed Ge layer (for all the three samples B1, B2, and B3) with respect to the Si001 substrate was found to less than  $0.006^\circ$ . This implies that an on axis Ge layers on Si001 was achieved.

Figure 3 show a typical 004 HR-RC obtained from all three samples (B1-B3). The top curve showing two diffraction peaks while the rest two curves shows three peaks. For sample B1, the top curve, the two peaks represent the Ge004 and the Si004 diffraction peaks. As clearly seen the Ge shows high crystalline quality as the peak is sharp. The other two curves show an addition peak between the Ge004 and the Si004. This extra peak is due to a tensile strained  $\text{Si}_{1-x}\text{Ge}_x$  layer grown on top of the relaxed pure Ge. Both samples B2, and B3 (as will be discussed later) have almost the same Ge fraction ( $x = 0.79$  for B2 and  $0.75$  for B3), but have a different degree of tensile strain. As the 004 symmetric reflections project only the perpendicular lattice parameter variations, the different degree of tensile strain on these  $\text{Si}_{1-x}\text{Ge}_x$  layers (samples B2, and B3) is seen as movement of the  $\text{Si}_{1-x}\text{Ge}_x$  peaks towards the Si substrate. Figure 4a-b shows a typical 2D-RSM around the 113 asymmetric reciprocal lattice point for sample B2 and B3. Three different peaks are observed in both 2D-RSMs. These are the Si113, Ge113, and the  $\text{Si}_{1-x}\text{Ge}_x$ 113 peaks. In a 2D-RSM plotted in reciprocal lattice units the vertical alignment of the substrate and a layer peak demonstrates qualitatively the degree of relaxation. Qualitatively, and as was observed for sample B1, here the alignment of the Si 113 and the Ge 113 along the  $\omega/2\theta$  scan direction indicates a high relaxation level [9]. Indeed the extracted relaxation factors for the Ge113 peaks for both B2 and B3 were found to be close to unity, indicating fully relaxed buffer layer. However, the  $\text{Si}_{1-x}\text{Ge}_x$  113 peaks for both B2 and B3 (Fig. 4a, b) do not lie in the same straight line joining the Si113 and the Ge113 peaks. This indicates that the two tensile strained  $\text{Si}_{1-x}\text{Ge}_x$  layers ( $x = 0.79$  for B2 and  $x = 0.75$  for B5) are not fully relaxed with respect to the underlying Ge epitaxial layer. Indeed this was consistent with the extracted parameters. With the Ge113 layer peak as the



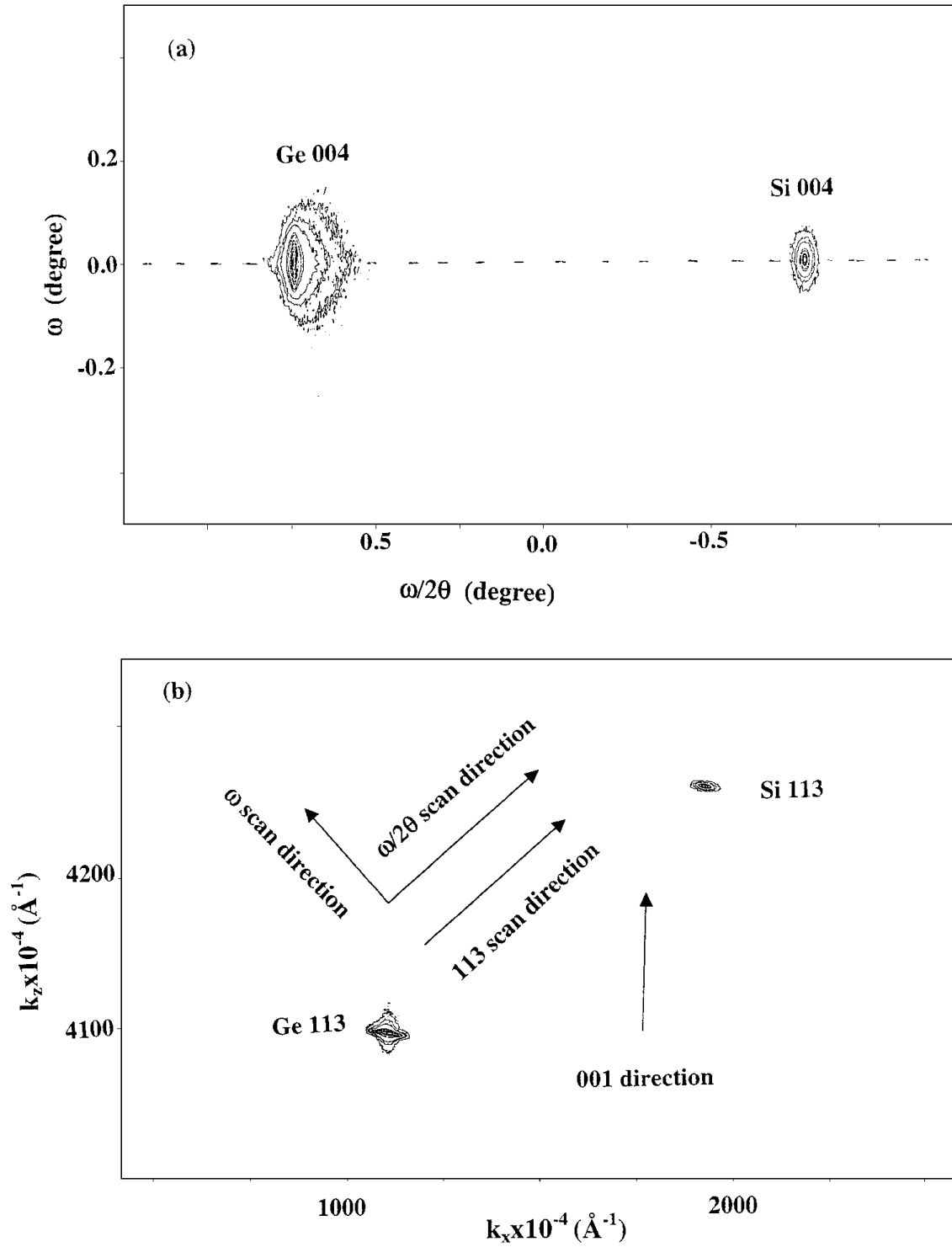
reference, these two layers are partially relaxed. Extracting the Ge%, lattice parameters and relaxation factors, was performed as described above [12]. For sample B2, which was grown with a lower Si flux but at the same growth thermal budget as B3, the Ge fraction was found to be  $x = 0.798 \pm 0.005$ , and the relaxation factor (with respect to the Ge layer) was found to be  $r = 0.274 \pm 0.002$ . The parallel and perpendicular lattice parameters were  $5.6485 \pm 0.0001$  Å, and  $5.5839 \pm 0.0001$  Å, respectively. The misorientation was below the measurement accuracy ( $\pm 0.0001$  degree). While for B3, which was grown with twice much Si flux as B2, the detected Ge fraction was  $x = 0.750 \pm 0.005$ , and the relaxation factor estimated was found to be  $0.404 \pm 0.002$ . Although, both B2 and B3 were grown with the same thermal budget, the relaxation factor observed for B3, is comparatively much higher than the relaxation factor resulted for B2 as the Si flux is increased. The lattice parameters for B3 were  $5.6386 \pm 0.0001$  Å, and  $5.5724 \pm 0.0001$  Å for the parallel and the perpendicular directions, respectively.

The estimation of threading dislocation is a rather complicated task, especially for a system with a large mismatch, and the absent of the knowledge of the actual type of threading dislocations in the heterostructure, as in the present samples. We have attempted to estimate the linear density of misfit dislocations at the interfaces. This linear misfit density of network dislocations was estimated from the jump of the in plane lattice parameters at the interface. We obtained for the first interface between the Si substrate and the fully relaxed Ge first epitaxial layer  $1 \times 10^{-6} \text{ cm}^{-1}$  for edge dislocations and  $2 \times 10^{-6} \text{ cm}^{-1}$  for 60-degree type dislocation. For the second interface between the fully relaxed epitaxial Ge layer and the tensile strained  $\text{Si}_{1-x}\text{Ge}_x$  (for both samples B2 and B3) the linear dislocation density was comparatively lower than the value estimated for the first interface. The estimated values of this upper interface for B2 were  $6 \times 10^4 \text{ cm}^{-1}$  and  $1.2 \times 10^5 \text{ cm}^{-1}$  for the edge and 60-degree type of dislocations, respectively. For sample B3 the corresponding estimation was  $1.1 \times 10^5 \text{ cm}^{-1}$  and  $2.2 \times 10^5 \text{ cm}^{-1}$  for the edge and 60-degree type misfit dislocations, respectively. Hence this preliminary qualitative assessment of the threading dislocations density for the tensile strained  $\text{Si}_{1-x}\text{Ge}_x$  over grown on fully relaxed epitaxial Ge on Si001 have shown that the adapted approach have resulted in an improvement of the upper tensile strained  $\text{Si}_{1-x}\text{Ge}_x$ /fully relaxed Ge interface compared to the lower fully relaxed Ge/Si001 interface. In addition and for B3, the threading dislocation density is higher than for B2. The full estimation of the 3D-dislocation density for these structures is an on-going work to be finished.

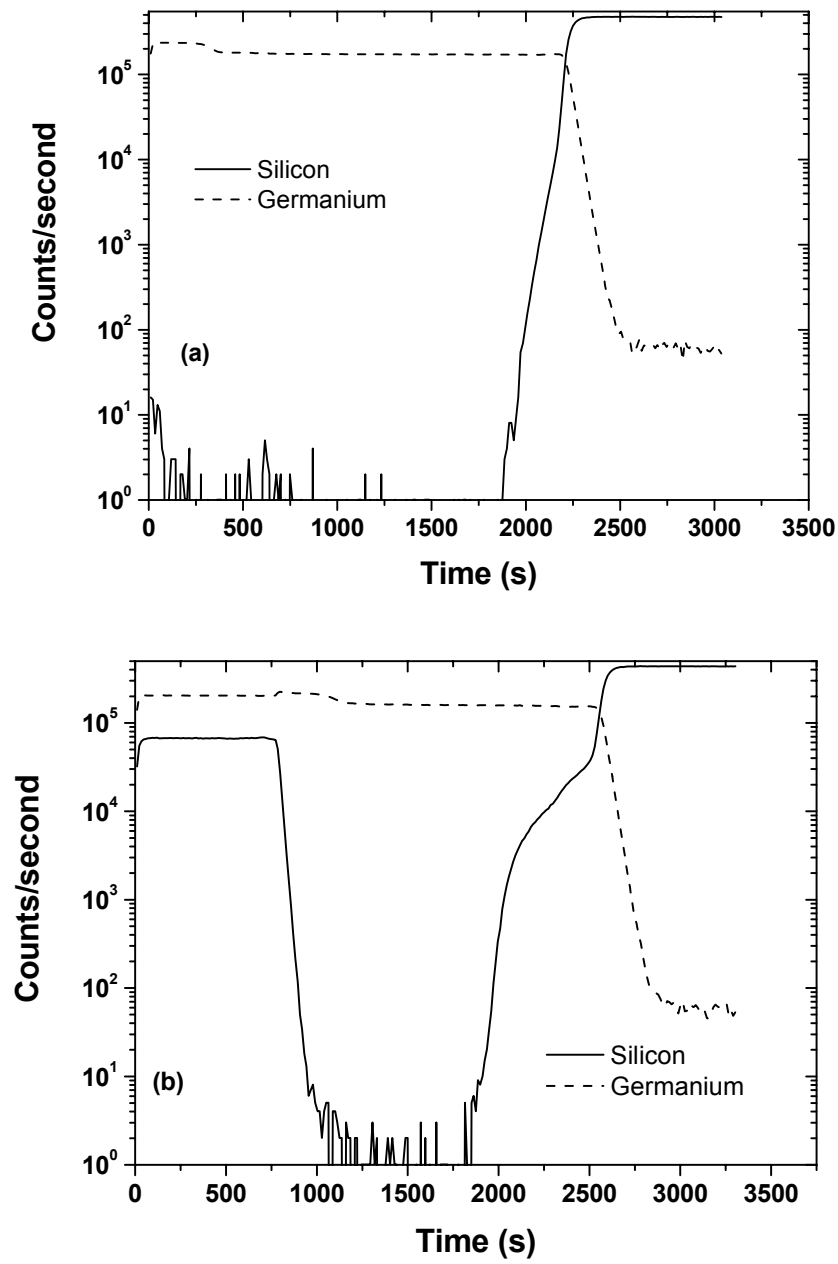
## **Conclusion:**

In summary CVD tensile strained grown  $\text{Si}_{1-x}\text{Ge}_x$  layers with different Ge fraction ( $x = 0.79$  and  $0.74$ ) grown on fully relaxed high quality Ge layers on Si001 is demonstrated. Using high-resolution x-ray diffraction, both rocking curves and triple axis two-dimensional mapping we characterized the strain relaxation, the exact Ge fraction, and estimated the lattice parameters. By growing the tensile strained  $\text{Si}_{1-x}\text{Ge}_x$  at a slightly higher temperature compared to the fully relaxed Ge epitaxial initial layer, and the variation of the Si flux, we can tune the degree of tensile strain in the layer. From an initial estimation of the linear misfit dislocation density at the interface we obtained a lower density of the misfit dislocation at the upper interface compared to the lower interface. This implies that the adapted approach is indeed in the right direction towards reduction of dislocation densities of the final top tensile layers.

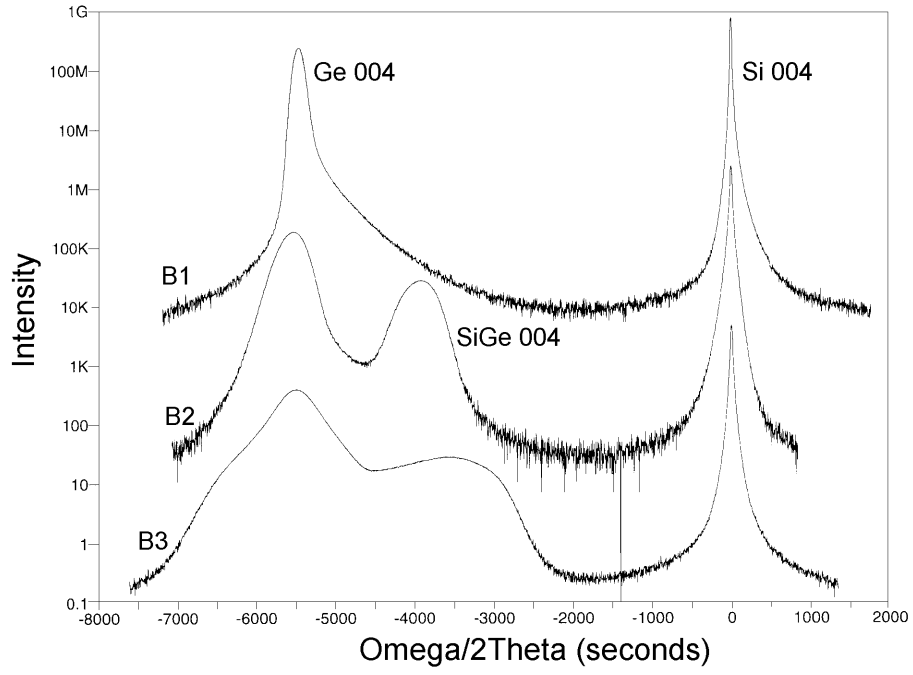
## Figures



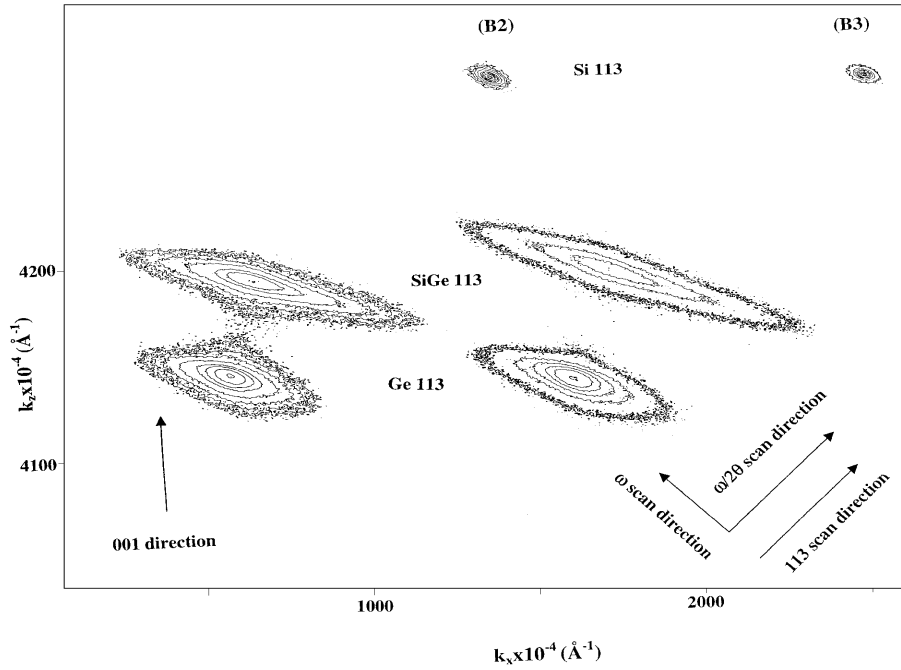
**Figure 1:** Shows a typical two-dimensional x-ray maps around the (a) symmetric 004 reciprocal lattice point in angular unit axis (and), and (b) around the asymmetric 113 reciprocal lattice point in reciprocal  $1a$  of the reference sample B1.



**Figure 2:** Secondary ion mass spectrometry (SIMS) of (a) reference sample B1, and (b) B2.



**Figure 3:** The 004 high resolution rocking curve of all three samples B1, B2, and B3.



**Figure 4:** Show a typical two-dimensional x-ray reciprocal space maps around (a) the asymmetric 113 reciprocal lattice point for sample B2, and (b) the asymmetric 113 reciprocal lattice point for sample B3.

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# Paper V

Hydrogen Passivation of Nitrogen Acceptors Confined  
in CdZnTe Quantum Well Structures





# Hydrogen passivation of nitrogen acceptors confined in CdZnTe quantum well structures

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The deactivation of nitrogen acceptors confined in Cd<sub>0.96</sub>Zn<sub>0.04</sub>Te/Cd<sub>0.86</sub>Zn<sub>0.14</sub>Te quantum well structures by hydrogen (deuterium) have been investigated by optical spectroscopy. Hydrogen (deuterium) was incorporated into the samples by annealing them in an atmosphere of hydrogen and cadmium. The annealing temperature and annealing time were varied to determine the optimum condition at which the maximum passivation is achieved without causing structural degradation. The emissions related to nitrogen acceptors were monitored in low-temperature photoluminescence measurements in order to deduce the passivation effect. The results indicate that hydrogen can effectively neutralize the nitrogen acceptors in cadmium zinc telluride quantum well structures. It is estimated that as much as 90% of the nitrogen acceptors can be passivated by this method. © 2001 American Institute of Physics. [DOI: 10.1063/1.1388569]

## INTRODUCTION

II–VI compound semiconductors such as CdTe, ZnTe, CdZnTe, and CdHgTe have a wide variety of uses. They are well known for their photovoltaic applications<sup>1,2</sup> and are seen as good candidates for detectors in the medium infrared spectral region, gamma ray, and x ray.<sup>3–5</sup> The interband transitions in quantum well (QW) structures are now being studied to exploit their potential as tuneable coherent light sources and new types of bistable modulators<sup>6</sup> in the blue green spectral range, i.e., they are used as blue-green light emitting diodes and lasers. It is found that they are ideally suited for this<sup>7,8</sup> provided that the strain between different layers is optimized.<sup>9</sup> The CdZnTe heterostructures are also studied for their ability to act as passive waveguides<sup>10</sup> at wavelengths in the transparent region to show optical confinement characteristics.<sup>11</sup> The fabrication of these devices involves a number of process steps, some of which involve exposure to an atmosphere of H<sub>2</sub>, and hence, incorporation of hydrogen into the device. The passivation effects of H<sub>2</sub> in semiconductors are its ability to neutralize the shallow/deep charged impurities/defects.<sup>12–14</sup> In addition to the study of impurity passivation, it is also a good tool to understand the fundamental behavior of a semiconductor. In passivation studies, it is found that hydrogen can form complex molecules with impurities and other dopants.<sup>12</sup> Hydrogen passivation on II–VI compound semiconductors is not well understood due to the difficulty in incorporating hydrogen to this class of semiconductors.

There are reports on the hydrogen passivation of impurities in bulk CdTe and ZnTe materials.<sup>15,16</sup> Hydrogen passivation leads to a complete disappearance of the excitonic peak due to the residual acceptor or/and a decrease in the

peak intensity of the emissions related to shallow impurities.<sup>15,16</sup> The deep levels in CdTe and ZnTe are unaffected by hydrogen. However, hydrogen can passivate the deep levels in CdZnTe and CdHgTe.<sup>12,17</sup> There have been no investigations reported in literature, in which the hydrogen passivation of impurities has been studied in CdZnTe quantum well structures. There are several reasons for this lack of investigations, first, hydrogen is difficult to introduce into II–VI QW structures without causing degradation of the structures, second, the hydrogen passivation effect is more difficult to be characterized due to limited doping volume, and third, there is very limited investigation on shallow impurities confined in II–VI quantum well structures in general.<sup>18</sup>

In this report, we have used photoluminescence (PL) as a tool to characterize the effect of hydrogen passivation on nitrogen doped CdZnTe single QW structures grown by molecular beam epitaxy (MBE). This is an attempt to learn the passivation effects on MBE grown CdZnTe QW structures using PL. D<sub>2</sub> was incorporated into CdZnTe QW structures by annealing. An optimum temperature range for maximum passivation with least structural degradation is suggested.

## SAMPLE AND EXPERIMENT

Nitrogen doped Cd<sub>0.96</sub>Zn<sub>0.04</sub>Te/Cd<sub>0.86</sub>Zn<sub>0.14</sub>Te (CZT) QW were grown in a MBE system. The growth temperature was optimized at 300 °C. The substrates were (001) CZT with 12% Zn concentration. By controlling the CdTe–ZnTe flux, the correct alloy concentration was obtained. The nitrogen doping was done using a dc plasma nitrogen source. Nitrogen acceptors were introduced at the center region of the well layer. An optimization of the Zn concentration was also necessary for obtaining a desired level of nitrogen dop-

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ing. Typical growth rates were  $\sim 0.6$  monolayers per second for the barrier and 0.5 monolayers per second for the well.

The samples used were single QW structures with acceptor doped in central region of the well layers. The barrier layer for the single QW is approximately 1000-Å-thick CZT (with a nominal 14% Zn) layer. The samples are center doped with a moderate nitrogen concentration (nominal  $5 \times 10^{17}/\text{cm}^3$ ), the doping region is of 9.7 Å thickness, i.e., 3 monolayers (ML). The well layer is a CZT (4% Zn) alloy with nominal thickness of 40 ML (130 Å). Further details about the samples are given in Ref. 18.

For hydrogen passivation studies, two similar groups of samples were chosen, one has slightly higher doping than the other. Since hydrogen and deuterium show a similar passivation effects, and deuterium is easier to characterize by secondary ion mass spectroscopy, we chose to use deuterium gas in this study.

The samples were sealed in quartz ampoules filled with 0.8 atmosphere  $\text{D}_2$  and a small amount of Cd. Deuterium incorporation was done by annealing these quartz ampoules. Two different conditions were used during annealing. The first set of sample was annealed at five different temperatures for 3 h. The second set of samples was annealed at 350 °C for three different times. This helped in optimizing the annealing time and temperature.

Hydrogen passivation was studied using the photoluminescence technique by carrying out the PL studies in a low temperature cryostat at 4.2 K. Rocking curves from high resolution x-ray diffraction (HRXRD) measurements were also used to analyze the structural changes that happened during annealing.

## RESULTS AND DISCUSSION

Figure 1 shows the PL spectra of the as-grown CZT sample at three different excitation densities measured at 4.2 K. The emissions for the CZT quantum well dominate the PL spectra.<sup>18</sup> As the excitation density increases, we found an increase in the intensity of the peaks. The intensity of the dominating transitions at about 1.60 eV in the PL spectra shows a significant increase with respect to the excitation density. This emission is related to the transition between the free electrons and holes bound to the acceptors (FB).<sup>18</sup> It is also seen that the LO phonons accompany the FB transitions with an energy separation of  $(21 \pm 0.5)$  meV.<sup>18</sup> The excitonic transition around 1.658 eV is from the  $\text{Cd}_{0.88}\text{Zn}_{0.12}\text{Te}$  substrate. The details regarding the origin of each emission are given elsewhere.<sup>18</sup> The relative increase in the intensity of the FB transition, LO phonon replicas and the *N*-acceptor bound excitons (BE) (labeled as  $A^0X$ ) is found to depend on the laser power. At higher laser power, the presence of the *Y* line and the free exciton (FE) is observed. The *Y* line is attributed to the  $X^-$ .

Figure 2 corresponds to the PL spectra from the as-grown sample (shown in Fig. 1) and the samples after different deuterium treatments at the laser excitation density of  $P_3$ . Three deuterium treated samples were annealed at 280, 320, and 350 °C for 3 h at the same deuterium gas pressure. The spectra illustrate change of the PL emission intensity with

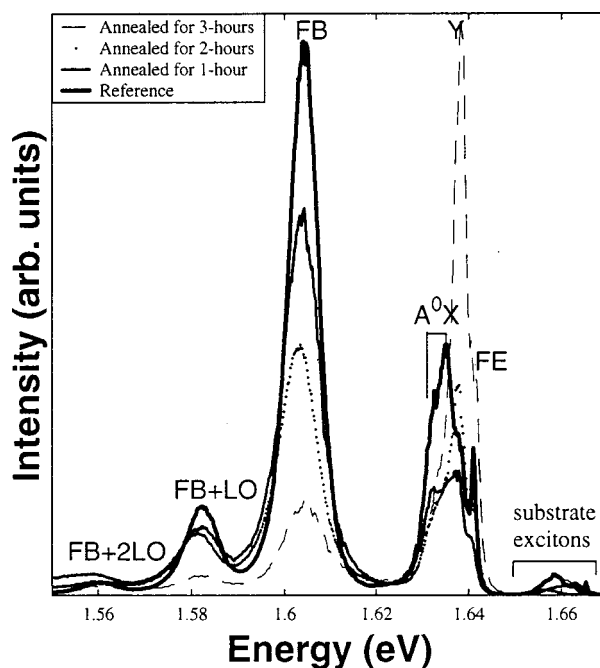


FIG. 1. The photoluminescence spectra of the as-grown CZT sample at three different excitation densities,  $P_1 = 1.1 \text{ W/cm}^2$ ,  $P_2 = 5.5 \text{ W/cm}^2$ ,  $P_3 = 19.5 \text{ W/cm}^2$ . The measurements are taken at 4.2 K.

respect to the annealing temperature. In the as-grown sample the FB transition dominates the PL spectrum. Once deuterium was introduced in the sample, the intensity of the FB transition decreases and the excitonic transitions labeled as FE and *Y* increases. As the annealing temperature increases, the transitions related to the nitrogen acceptors, such as FB, FB+LO phonon replicas and  $A^0X$ , are found to be suppressed. A significant increase in the intensity of the *Y* line is

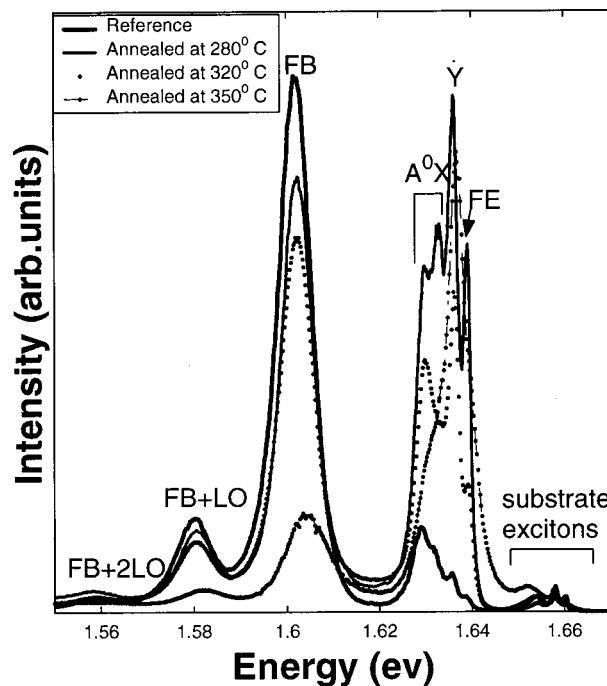


FIG. 2. PL spectra from the as-grown sample and the passivated samples at the laser power density  $P_3$ , measured at 4.2 K.

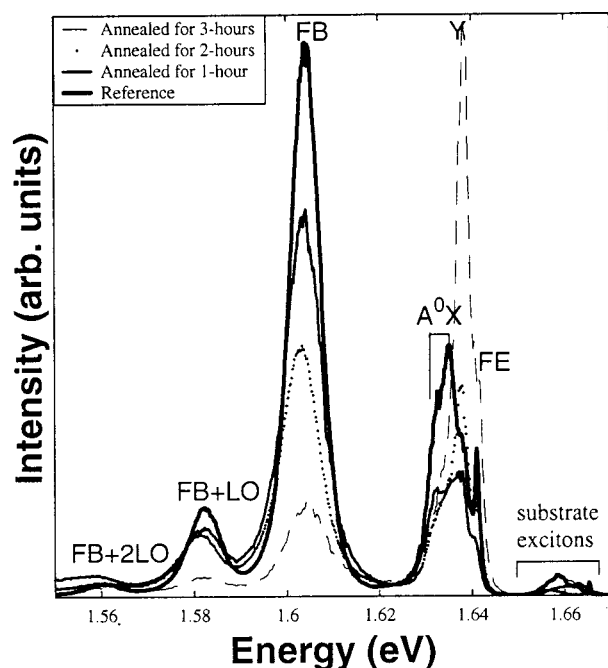


FIG. 3. PL spectra of the as-grown sample and the passivated samples annealed at three different duration times at temperature of 350 °C, measured at 4.2 K and the laser power density  $P_3$ .

observed in the sample annealed at 350 °C, whereas the nitrogen acceptor related transitions show a strong suppression. The significant enhancement of the  $Y$  line and FE line compared to  $A^0X$  indicates that the deuterium atoms deactivate a large percentage of nitrogen acceptors. This proves that nitrogen acceptors become passivated by deuterium. In the PL data of the deuterium-passivated samples, we found that the double lines corresponding to the acceptor BE are both passivated. This further confirms our earlier interpretation,<sup>18</sup> i.e., they are the excitons bound to the center and edge  $N$  acceptors, labeled as the  $A^0X$  and  $A^0X''$  corresponding to the acceptors at or near the well/barrier interface, respectively. From the PL emissions, we can see that the QW structure is not significantly influenced by annealing at temperature below 320 °C. However, in the sample annealed at 350 °C, the transition energies of the FB,  $Y$ , and FE show a slight blueshift. This fact indicates that the elements in the barrier layers and well layer start to interdiffuse.

In order to study the effect of annealing duration, Fig. 3 shows the spectra of the sample annealed at 350 °C for three different annealing duration times. The decrease in the PL intensity of the FB and FB+LO peaks and the subsequent increase in the  $Y$  line and FE transitions are related to the increase in the annealing time. A strong increase in the intensity of  $Y$  line and FE is observed for the sample annealed for 3 h. Thus, 3 h of annealing at 350 °C is found to be the optimized annealing condition for obtaining a significant passivation without a major degradation in the QW structure.

It should be noted that for those samples annealed above these temperatures that are discussed, i.e., at 450 and 550 °C, there is a strong degradation of the QW structure. The emissions from the well are hardly detectable from those samples.

TABLE I. Percentage of passivation achieved at different temperatures and different annealing duration times.

Set	Annealing temperature (°C)	Annealing duration time (h)	Estimated percentage of passivation
1	280	3	60%
1	320	3	80%
1	350	3	90%
1	450	3	No emission observed
1	550	3	No emission observed
2	350	1	12%
2	350	2	30%
2	350	3	90%

This is due to the strong interdiffusion of Zn atoms between the barrier and well region.

The degradation of the QW structure due to the annealing was also observed from the HRXRD rocking curves. The HRXRD rocking curves is consistent with the conclusion from the PL data, which shows that the QW structure is not significantly influenced by an annealing at temperature below 350 °C. It should also be pointed out that the samples annealed at the same temperature but with Ar gas show no passivation effects.

It is very difficult to exactly estimate how much nitrogen acceptors were deactivated by the deuterium, since the PL measurements is not a direct measurement of absorption and so cannot directly provide the information of impurity concentration. Nevertheless, we can use the relative PL intensity between the FB transition and the BE transition to estimate the concentration of the active nitrogen acceptors,<sup>19</sup> using the following expression:

$$N_{\text{acc}} = A \frac{I_{\text{FB}}}{I_{\text{BE}}} + N_{\text{CR}},$$

where  $N_{\text{acc}}$  and  $N_{\text{CR}}$  are the acceptor concentration and the critical acceptor concentration.  $I_{\text{FB}}$  and  $I_{\text{BE}}$  are the integrated PL intensity of the FB and BE transitions associated with the acceptors. Parameter  $A$  is a factor that depends on the excitation power and remains a constant in our case, since the excitation density is kept at a constant level for all measurements. The PL intensity of both the BE and FB emissions are obtained by deconvoluting the measured PL data. The estimated percentage of passivation is given in Table I. The uncertainty of the estimated value is about 10% of the deduced value. The results show that the sample annealed for 3 h at 350 °C gives about 90% deactivation of nitrogen acceptors.

In summary, we have presented a study on the deuterium passivation of nitrogen acceptors confined in CZT QW structures. Hydrogen (deuterium) was incorporated into the samples by annealing them in a deuterium atmosphere. The emissions related to nitrogen acceptors were monitored in low-temperature photoluminescence measurements in order to deduce the passivation effect. The results indicate that hydrogen can effectively neutralize the nitrogen acceptors in CZT QW structures. From our study, we can conclude that annealing at a temperature of 350 °C for 3 h is an optimized condition in order to achieve a high level of passivation without significant structural degradation.

## ACKNOWLEDGMENTS

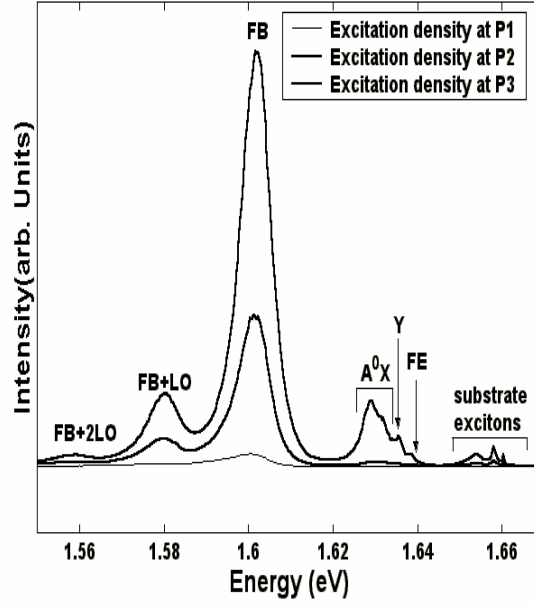
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## Errata for Paper V

Paper V: Figure 1 is wrong in the publication (A. P. Jacob et. al., J. Appl. Phys., Vol.90, No.5, 1 September 2001).

The correct figure is;



**FIG. 1:** The photoluminescence spectra of the as-grown CZT sample at three different excitation densities,  $P1=1.1 \text{ W/cm}^2$ ,  $P2=5.5 \text{ W/cm}^2$ ,  $P3=19.5 \text{ W/cm}^2$ . The measurements are taken at 4.2 K.

# Paper VI

Hydrogen Passivation of Self Assembled InAs  
Quantum Dots





# Hydrogen passivation of self assembled InAs quantum dots

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A systematic study on the hydrogen passivation of nonradiative centers in InAs quantum dot's grown on GaAs substrates is presented. The samples used in this study were grown by molecular beam epitaxy. The structures contain an  $\text{In}_x\text{Ga}_{1-x}\text{As}$  insertion layer between the InAs quantum dots layer and the GaAs cap layer. The thickness and In concentration of the  $\text{In}_x\text{Ga}_{1-x}\text{As}$  are varied to achieve the emission wavelength at 1.3  $\mu\text{m}$ . The samples after the  $\text{H}_2$  plasma treatment show a significant increase of the photoluminescence intensity. The experimental results show that the quality of the InAs quantum dot structures does not degrade after the hydrogen ( $\text{H}_2$ ) plasma treatments. The enhancement of the photoluminescence intensity from the InAs quantum dots is thought to be due to the passivation of nonradiative centers like defects in the structures. High resolution x-ray diffraction rocking curves are used to correlate photoluminescence results.

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## INTRODUCTION

Today, applications oriented studies on quantum dots are mainly concentrated towards the fabrication of quantum dot (QD) lasers.<sup>1,2</sup> In comparison with the two dimensional quantum well lasers, it has been shown that quantum dot based lasers have lower threshold current densities, can operate at higher temperatures, and has higher gain characteristics.<sup>3–6</sup> The experimental study has demonstrated that stronger luminescence is achieved in dots structures than in quantum wells of similar composition at room temperature. Room temperature lasers based on QD structures have already been fabricated by a number of research groups.<sup>7,8</sup> Selecting a semiconductor material and the methodology with which it is fabricated into a quantum dot depends on the application that the QD is to be used for. Self assembled quantum dots, for example, grown by the S-K growth method, are very promising due to low density of defects and high efficiency of luminescence emission at room temperature. The properties of these islands strongly depend on the growth conditions such as the molecular beam fluxes, substrate temperature, thickness of cap layer, growth rate and growth temperatures of the quantum dots.

Quantum dots made of III–V materials like InAs/GaAs and InGaAs/AlGaAs alloy combination seem to be the most promising candidates for immediate industrial applications, since the emission wavelength from InAs QDs can be tuned to 1.3  $\mu\text{m}$  which is a key wavelength for fiber optic communication networks. These InAs islands formed on GaAs can replace structures based on InP that are presently at use in communication networks. It is necessary to replace InP sub-

strates because they suffer from low temperature instability in threshold currents, difficulty in fabrication and are also very expensive. Another advantage in replacing InP is that high reflectivity distributed Bragg reflector mirrors can be grown in GaAs system for vertical cavity surface emitting lasers (VCSELs). These VCSELs can operate at 1.3  $\mu\text{m}$ . Thus InAs QDs grown on GaAs substrates hold promise for communication lasers with high temperature stability.

Several reports have been published on the postgrowth processing of a quantum dot. Most of these studies are concentrated on the high temperature annealing properties and stability.<sup>9</sup> Postgrowth thermal annealing at higher temperatures in now used as a means of tuning the lasers to different wavelength. Tuning of quantum dots to the desired wavelength could be achieved because of the interdiffusion that takes place at elevated temperatures, i.e., annealing treatment induces a blueshift in the emission energy and also a narrowing of the linewidth.<sup>10</sup> Though the luminescence wavelength is changed, there is also a pronounced decrease in luminescence intensity due to the increase in nonradiative centers.<sup>11</sup> Similar to quantum well structures and bulk materials the QDs structures also contain nonradiative defects, which strongly influence the optical gain of laser performance at room temperature.

Hydrogen plays an important role in passivating interfacial defects like dislocations in heteroepitaxial layers.<sup>12</sup> In optical devices dislocations lead to nonradiative areas and hence higher threshold and shortened device lifetimes. Hydrogen incorporation can lead to a reduction in the number of these non radiative centres and thus can increase the luminescence efficiency. Le Ru *et al.*<sup>13</sup> have shown that low temperature annealing of the InAs QD in an atmosphere of hydrogen increases the luminescence intensity. They have introduced hydrogen in to the samples through the plasma

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TABLE I. A detailed description of different InAs QD samples used in this study

Sample	InAs QD (ML)	InGaAs QW (ML)	In content
A	3.5	0	0.4
B	3.5	7	0.4
C	3.5	10	0.4
D	3.5	30	0.2

passivation technique. R. Leon *et al.*<sup>14</sup> have observed that a relatively moderate proton dose can slightly increase the intensity of luminescence emission. A detailed study of the influence of hydrogen in the quantum dots is needed to be done as hydrogen is an intentional as well as an unintentional impurity during the fabrication of a group III–V device. Normally hydrogen can be incorporated in III–V material at temperatures below 300 °C.

In this article, we have performed a systematic study on the effect of hydrogen passivation of the InAs QDs by optical spectroscopy for four different InAs QD structures. These four quantum dot samples vary in their emission energy because of the varying thickness of the insertion layer  $\text{In}_x\text{Ga}_{1-x}\text{As}$  between the InAs QDs layer and the GaAs cap layer and the communication wavelength of 1.3  $\mu\text{m}$  can be achieved. Incorporation of hydrogen into these QDs is done through hydrogen plasma treatment at two different temperatures for different time scales. Optical characterization of these QDs is done by room temperature photoluminescence (PL) measurements. Structural changes due to annealing were studied on these QDs by high resolution x-ray diffraction (HRXRD).

## EXPERIMENT

The samples for these studies are grown using an EPI930 solid source molecular beam epitaxy system. The substrates for the growth of QDs are semi-insulating (001) GaAs. The substrate temperature was maintained at 510 °C during the growth of InAs layer. A buffer layer of GaAs of approximately 50 nm was grown prior to the growth of 3.5 ML growth of InAs layer. After every 0.1 ML of InAs growth, a growth interruption for 2 s was allowed under a continuous flow of As. For sample A, a cap layer of approximately 200 nm GaAs was grown. For samples B–D, an  $\text{In}_x\text{Ga}_{1-x}\text{As}$  QW layer was first grown prior to the 200 nm GaAs cap layer. The important difference between all the four samples is in their  $\text{In}_x\text{Ga}_{1-x}\text{As}$  layer. A detailed description of the samples is given in the Table I and Fig. 1.

Atomic hydrogen was introduced into the samples by a dc plasma technique. The samples were mounted on a heater block which can control the sample temperature  $T_s$  with an accuracy of 2 °C, and placed 10 cm downstream from the plasma with a bias voltage of 300 V. Both the pressure of the plasma and the bias voltage were kept at constant, while a systematic study was done by varying both the treating temperature and duration time. The samples were kept at a substrate temperature of 250 and 150 °C for various times ranging from 2 h to 15 m. We have also done thermal annealing of these samples in argon gas at a temperature of 250 °C at

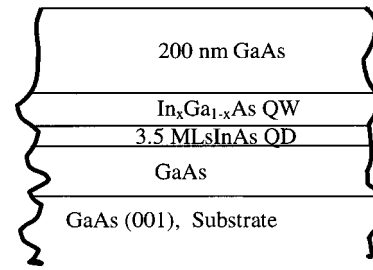


FIG. 1. Cross-sectional view of InAs QD structure.

various time scales to check the effect of annealing. An  $\text{Ar}^+$  laser line was used as the excitation source for room temperature PL measurements. The emissions were detected by a liquid nitrogen cooled Ge detector.

HRXRD rocking curves are used to study the structural evolution of these low dimensional heterostructures. We have employed a multi-crystal high resolution Philips Extended X-pert material Research Diffractometer, equipped with a computer-controlled motorized goniometer. This diffractometer enables the optimization of the scattering angles with angular step sizes down to  $1.0 \times 10^{-3}$  deg for the angles of incidence and reflection, and step sizes down to  $1.0 \times 10^{-2}$  deg for the angles of rotation around the surface normal and around the in plane horizontal directions. A four crystal Ge (220) Bartels monochromator is used to collimate the Cu tube x-ray incident beam with a divergence of 12 arcsec, and for secondary optics, the rocking curves were collected using a slit with a width of 0.5°.

## RESULTS AND DISCUSSION

Figure 2 shows the PL spectra of the four QDs samples used in this study. The PL peaks correspond to the room temperature emissions from the quantum dots. Two PL peaks are observed from each QDs sample and they are labeled as *E1* and *E2*. Peak *E1* corresponds to the ground state emission of the quantum dots. The weak emission (*E2*) near the

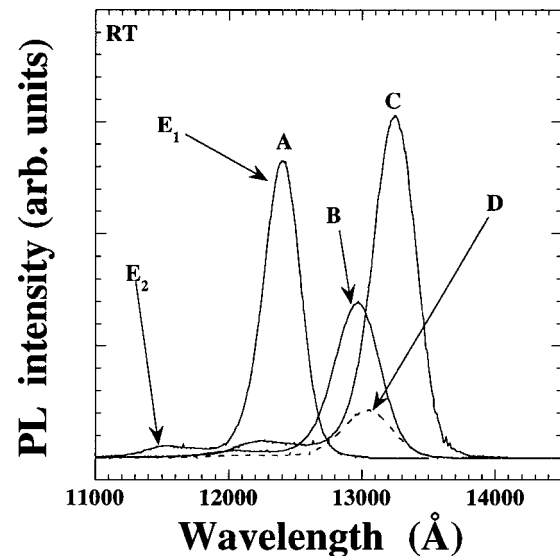


FIG. 2. Room temperature PL spectra of samples A – D.

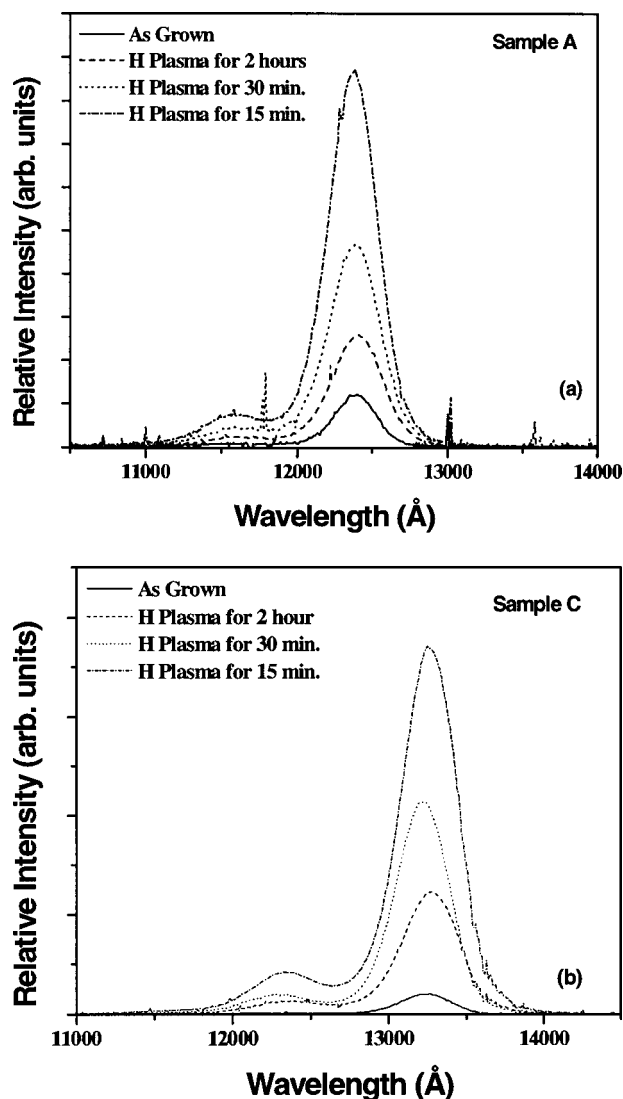


FIG. 3. (a) and (b) Room temperature PL spectra of the as-grown and the passivated samples treated at 250 °C for plasma exposure duration of 120, 30 and 15 min for samples A and C, respectively.

ground state is the first excited state of the QD. Thus,  $E1$  and  $E2$  correspond to the first and second confined electron states in the QD, respectively. The luminescence peaks at 1.24, 1.295, 1.33, and 1.305  $\mu\text{m}$  correspond to the  $E1$  emission for samples A, B, C, and D, respectively. Upon comparing the first three samples A, B, and C, we find that as the thickness of the InGaAs insertion layer increases the emission wavelength increases, i.e., it shows a redshift in its energy. The sample covered with pure GaAs gives an emission wavelength of 1.24  $\mu\text{m}$ . For a thickness of 7 ML, a luminescence wavelength of 1.3  $\mu\text{m}$  is achieved. But as the thickness is increased to 10 ML, the wavelength has increased to 1.33  $\mu\text{m}$ . For sample D, by keeping the In concentration around 20% and by varying the InGaAs thickness we could also achieve the 1.3  $\mu\text{m}$  emission. It is thus found that by properly manipulating the thickness of the InGaAs layer and In concentration, one can easily achieve the critical communication wavelength emission of 1.3  $\mu\text{m}$  from an InAs QD.

Figure 3 shows a typical PL spectrum of the hydrogen passivated samples. The sample temperature during the hy-

drogen plasma treatment was done at a temperature of 250 °C. The duration time of hydrogen plasma exposure of these samples are for 15, 30, and 120 min. The samples exposed to hydrogen clearly show an increase in its luminescence intensity. Since the position of the PL peaks does not shift, the hydrogen plasma treatments at the temperatures and duration times used here do not cause any degradation of the structural quality of these samples. It should be noted that both the peaks  $E1$  and  $E2$  increases in intensity. The significant increase in the luminescence intensity after hydrogen incorporation is due to the fact that there is suppression of the nonradiative recombination centers after the hydrogen incorporation. These nonradiative centers are the defects that are present in the QD interfaces, GaAs barriers, and the InGaAs QW region. It is well known that defects can be passivated by hydrogen.<sup>15</sup> All the samples studied here give similar results, the only difference is the amount of luminescence enhancement that the hydrogen passivation could bring upon. Similar results were also obtained for the samples treated at 150 °C. In order to confirm our conclusion that the PL enhancement is due to the hydrogen passivation of nonradiative centers, thermal annealing effects of these samples were also studied by annealing them in an argon atmosphere at a similar temperatures for different time periods. Since the PL intensity of the samples thermally annealed in an argon atmosphere does not change significantly, we can conclude that the phenomenon observed in hydrogen plasma exposed samples are solely due to the hydrogen passivation effects.

Figures 4(a)–4(d) compare the integrated intensity of emission for all the samples at two different temperatures at various durations of the hydrogen treatment. All these samples give similar kinds of characteristics. By comparing the figures, one can find that an annealing at 150 °C for 15 min gives the maximum luminescence intensity in all these samples. Samples A, B, and C show a similar trend in both the annealed temperatures (250 and 150 °C) at all annealing durations. The samples annealed at 250 °C have lower intensity compared to 150 °C for the same duration of H plasma exposure. Among the plasma exposed samples, the lowest luminescence intensity is for the one exposed at 250 °C for 2 h. At a plasma exposure duration of 15 min, we find that samples A, B, and C have increased their integrated luminescence intensity by 1 order of a magnitude while sample D by a factor of 5. Thus it is a significant improvement for the sample without any structural degradation and could be exploited during the processing of lasers. So the increase in intensity is due to the decrease in the nonradiative centers. The nonradiative centers can be of the form of defects in either interfaces of the quantum dots or the quantum well ( $\text{In}_x\text{Ga}_{1-x}\text{As}$ ) insertion region. Reducing the number of these nonradiative centers means that hydrogen could passivate these defects. From the spectrum, we can also see a gradual decrease in the luminescence intensity as the duration of  $\text{H}_2$  plasma exposure increases. In the case of sample D, the luminescence intensity has decreased to the level of the as-grown sample for an exposure time higher than 30 min. This decrease in intensity seen in all the samples after a prolonged plasma exposure is due to surface damage. This

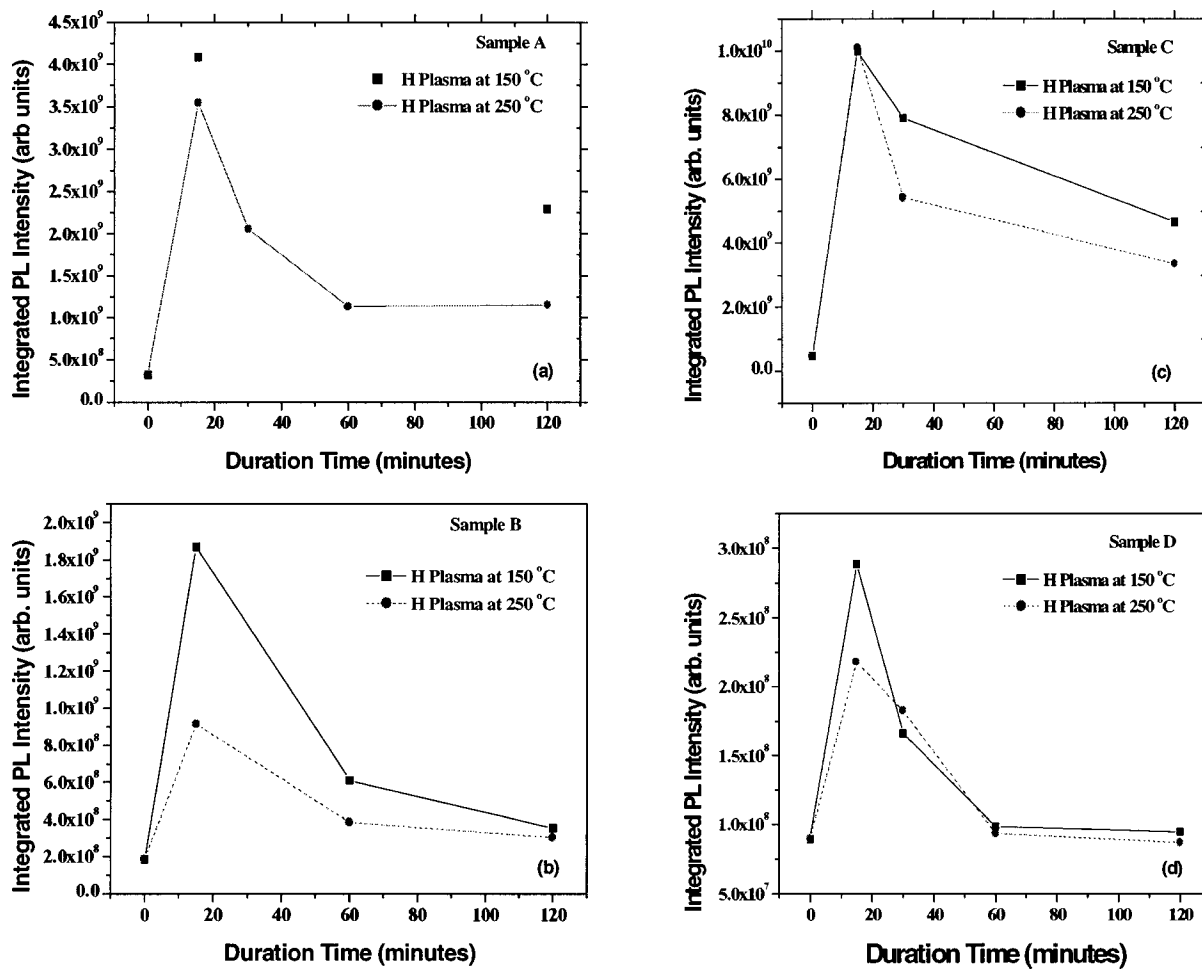


FIG. 4. (a)–(d) comparison of the integrated photoluminescence intensity for the plasma passivated samples A–D.

can be explained by: (1) surface damage causes more scattering of light. It can also increase the absorption of light on the surface. This reduces the effective excitation intensity. (2) Since surface recombination is nonradiative, prolonged exposure to plasma changes the surface state density. Surface state density is proportional to the surface recombination velocity. The surface recombination velocity  $V_S$  is defined as the number of carriers recombining on the surface per unit area per unit time per unit volume of excess bulk carriers. Also, an increase in surface density can increase the width of the surface depletion region which increases  $V_S$ .  $V_S$  is the highest when the surface Fermi level is at the center of the midgap in this region. Thus, highest values of  $V_S$  are obtained when both surface Fermi level and energy of the trap lie at the midgap. An increase in  $V_S$  decreases PL intensity.<sup>16,17</sup> Another point to be noted is that the increase in luminescence intensity of these hydrogen passivated samples depends on the excitation power. The experimental results show that the luminescence intensity can vary from a factor of 12 at low excitation to a factor of 2 at higher excitation. This is due to the fact that as the excitation power increases the number of carriers also increases. These carriers are captured by nonradiative centers in the GaAs barrier region and the GaAs surface and also by the InAs QDs. This can create competition between the InAs QDs and the nonradiative cen-

ters in the rest of the region. Radiative recombination in the QDs is dependent on the factors like the capture cross section of the QDs, the distance of the InAs QDs from the generated carriers, etc. Also, H<sub>2</sub> plasma exposed samples show less dependency on the temperature indicating the passivation of nonradiative centers.<sup>18</sup>

Figure 5 shows the x-ray diffraction spectrum of sample A, as grown, simulated curve of the as grown sample, the hydrogen plasma exposed at 250 °C for 2 h and 150 °C for 15 min. The simulations are done in accordance with the Takagi–Taupin theory<sup>19</sup> where the structures are assumed to be fully strained and non distorted. Both the simulated curves and the experimental rocking curve of the asgrown samples shows the presence of thickness fringes on both the low and high angle sides of the substrate peak. These fringes are caused by the phase shift between the diffracted waves from the upper GaAs cap layer and the lower GaAs substrate which are separated by the InAs dots layer, and the lattice mismatch between InAs and GaAs is about 7%. The effective phase shift depends on the product between the strain and thickness.<sup>20,21</sup> The presence of these fringes is attributed to the high structural quality with sharp interfaces among the quantum dots, buffer layer, and the cap layer. It should be noted that the simulation shows an excellent agreement to the experimental rocking curve of the as grown sample. In



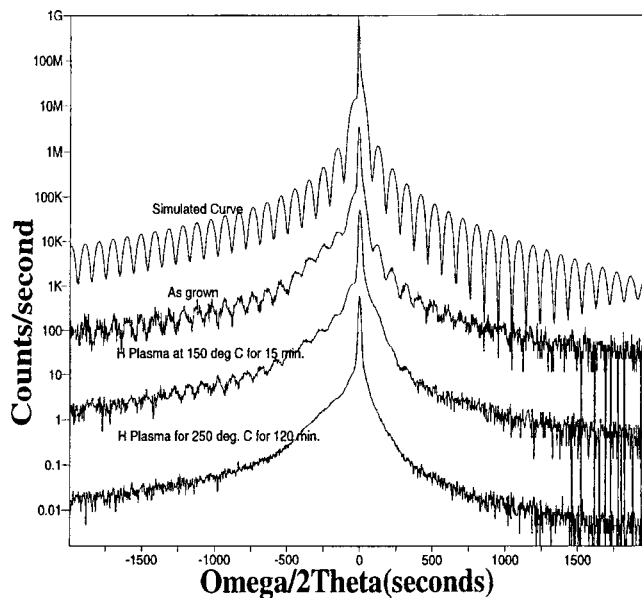


FIG. 5. High resolution X-ray diffraction rocking curve of sample A. The simulated, as grown, and the hydrogen plasma exposed samples are shown.

Fig. 4, the sample annealed at 150 °C for 15 min shows the same features as that of the as grown sample, but the one annealed at 250 °C for 2 h shows a complete disappearance of the fringes. This disappearance of the fringes is due to the fact that the plasma treatment has bombarded away some of the GaAs cap layer creating small craters. The sample annealed at 150 °C for 2 h also retains much of its thickness fringes. This shows that there is not much damage caused to the surface of this sample. This retains the fact that this sample has higher PL intensity compared to the 250 °C sample annealed for the same time. We also find a faster disappearance of the fringes for samples annealed at 250 °C for the same time of annealing compared to the samples annealed at 150 °C. This shows that degradation on the GaAs surface occurs faster for those samples exposed to plasma at higher temperatures. Though the fringes are absent for the sample exposed to plasma at 250 °C for 2 h, the possibility of In diffusion into GaAs layer at these temperatures is very low. This can be verified from the energy position of the InAs QDs PL emission spectrum since there is no change on the InAs QDs emission wavelength. Similar results were also obtained for all the other samples. Therefore the decrease in the PL spectral intensity with increase in the time of the hydrogen treatment is due to the surface damage, and this conclusion is consistent with the XRD results.

## CONCLUSION

We have done a systematic study of H-plasma treatments on InAs QDs by varying temperature and duration of treatment. We have seen that hydrogen can passivate nonradiative centers in InAs QDs. We have found that hydrogen plasma exposure at a low temperature for a shorter duration gives the maximum enhancement in the luminescence. We have also seen that even though the plasma exposure is done at a low temperature, a prolonged exposure can in fact influence the quality of the surface of the sample.

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# Paper VII

Room Temperature Luminescence from  $\text{ZnSe}_{1-x}\text{Te}_x$   
( $x < 1\%$ ) Epilayers Grown on (001) GaAs





**Room temperature luminescence from  $\text{ZnSe}_{1-x}\text{Te}_x$  ( $x < 1\%$ ) epilayers  
grown on (001) GaAs**

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**Abstract**

Photoluminescence experiments have been performed to systematically study the effect of thermal processing on  $\text{ZnSe}_{1-x}\text{Te}_x$  ( $x < 1\%$ ) epilayers. Our results show that,  $\text{ZnSeTe}$  epilayer under proper post growth thermal annealing can emit light in the visible range of 5500-7000 Å at room temperature. Thus by systematically processing these samples, they could be used for II-VI laser diodes that can operate at room temperature. Hydrogen passivation study done on these samples confirms the previous reports that the broad band emission is related to isoelectronic defect, i.e., excitons bound to the Te clusters.

**Introduction**

Among the wide band gap materials,  $\text{ZnSe}$  compound semiconductors are of potential importance due to the blue-green light emission [1].  $\text{ZnSeTe}$  epilayers are used as potential ohmic contacts for  $\text{ZnSe}$  materials [2]. The advantage of using  $\text{ZnSe}_{1-x}\text{Te}_x$  is that they can be made both p-type and n-type depending on the concentration of Te. Low resistivity n-type or p-type contacts can be fabricated by varying the  $x$  concentration in the range  $0.5 \leq x \leq 0.6$ , respectively. Apart from this, they are also seen as a potential

candidate used as the active layer for light emitting diode structures [3]. Bulk  $\text{ZnSe}_{1-x}\text{Te}_x$  had been of fundamental importance since Te in these material acts as an isoelectronic center. Surprisingly, very low concentration of Te ( $x < 0.1$ ) gives a very broad band luminescence. This is in contrast to normal isoelectronic impurities that give narrow luminescence bands.

In this article, we have presented photoluminescence measurements on Argon and deuterium annealed  $\text{ZnSe}_{1-x}\text{Te}_x$  ( $x < 1\%$ ) epilayers. We have found that by systematically annealing these samples potentially valuable room temperature luminescence emission can be obtained in the range between 5500 to 7000 Å. To the best of our knowledge, this is the first time that such investigation has ever been reported. We propose that by systematic thermal processing of these samples, light emitting devices of potential visible energy emission can be fabricated. Annealing in  $\text{H}_2$  atmosphere also confirms the previous results that the broad band emission is due to excitons bound to Te clusters and not due to charge defects.

## Experiments

$\text{ZnSe}_{1-x}\text{Te}_x$  epilayers were grown on GaAs (001) substrates using an EPI 620 molecular beam epitaxy system. EPI 40 cc low temperature cells were used for evaporation of the elemental solid sources: Zn, Se and Te. The cell temperature of Zn was fixed at 300 °C, while the cell temperatures of Se and Te ranged from 178 to 162 °C and from 230 to 310 °C, respectively. The growth rate was about 0.3-0.4  $\mu\text{m}/\text{h}$ . During the growth, reflected high energy electron diffraction was used to monitor the process of epitaxial growth. The  $\text{ZnSe}_{1-x}\text{Te}_x$  layer with the aimed Te concentration of less than 1% and thickness of 0.5  $\mu\text{m}$  was grown.

Annealing this sample was done in commercially available furnaces with a temperature variation of less than 2 °C. The samples were first sealed in quartz ampoules filled with 0.8 atmosphere  $\text{H}_2$  and  $\text{Ar}_2$  gas. The samples were annealed at 300 °C and 350

°C for 3 hours. Some of the samples annealed at 300 °C were again annealed at 350 °C for 3 hours. Table 1 gives a brief outline on the annealed samples used for this study.

Photoluminescence spectra was measured in a temperature range from 5 K to room temperature, using the 514.5 nm line of Ar<sup>+</sup> laser as the excitation source. The PL signal from the sample was dispersed by a double grating monochromator (0.85 m disperse length and 0.1 nm spectral resolution) and then detected by a photomultiplier detector.

## Results and Discussions

Figure 1 shows the PL spectrum of the as grown sample at 5 K and 77 K. The broad band emission in the figure is identified as the exciton bound to two or more isolated Te clusters, (X/Te<sub>n</sub>) [4,5]. The corresponding energy at 5 K is around 2.63 eV. This is found to have a blue shift as the temperature is increased to 77 K. Also, the intensity of this band starts decreasing and is finally quenched at 100 K. The other energy bands found at 5 K is due to the excitonic emission bound to single Te atoms (X/Te). At 77 K, the band around 2.76 eV corresponds to the free exciton emission. The free exciton (FE) emission is not observable at 5 K, but becomes dominant at higher temperature and even at 200 K, they can be observed.

The Te concentration in our sample can be derived from the following relation [6],

$$E_g(x) = xE_{ZnTe} + (1-x)E_{ZnSe} - bx(1-x) \quad (1)$$

where the band gap energy of ZnTe ( $E_{ZnTe}$ ) and ZnSe ( $E_{ZnSe}$ ) are 2.4 eV and 2.82 eV respectively. “b” is the bowing parameter and is 1.23 eV.  $E_g(x)$  is the band gap energy of ZnSe<sub>1-x</sub>Te<sub>x</sub>. These energy values correspond to a temperature of 4K. Since we could only observe the free exciton emission at 77 K, and the concentration of Te in our ZnSe<sub>1-x</sub>Te<sub>x</sub> sample is so small, the free exciton energy at 4K can be estimated by using the following relation that is deduced from ZnSe material [7],

$$E_g = E_g(4K) - 4 \times 10^{-4} \frac{dE}{dT} \times T \quad (2)$$

The free exciton energy obtained at 77 K is around 2.76 eV. By using the above equation, the free exciton energy corresponding to 4 K can be derived as 2.788 eV. Since the concentration of Te is assumed to be small, we take the bound exciton energy value of 18 meV for ZnSe for converting the free exciton energy value into band gap energy. Thus the band gap energy for our sample at around 4 K is 2.806. By using this band gap energy value in the equation (1), we find that the Te concentration is around 0.9% ( $x = 0.009 \pm 0.001$ ). This is consistent with the aimed value of less than 1%. The value deduced from the PL measurement is also confirmed by using the high resolution X-ray rocking curves. Figure 2 gives the measured and simulated x-ray rocking curves for 100 % relaxed and 100 % strained layer with 1% Te concentration. Our sample with the above concentration is found to be slightly strained. The X-ray rocking curve simulations are done using Takagi-Taupin theory [8].

Figure 3 gives the photoluminescence spectra at 5 K for the as grown sample and the sample annealed at various temperatures in Ar atmosphere. We find that the intensity of the broad band (2.63 eV) decreases in the annealed samples (Sample A, B and C). This means that the intensity of this peak depends on the time and temperature used for annealing. Higher temperature and prolonged time of annealing gives additional peaks and this can be seen in the samples B and C and these are the samples annealed at 350 °C for 3 hours and (300 + 350) °C for 3 hours each. These additional peaks are located at 2.255 eV and 1.95 eV. These additional peaks could be due to defect complexes that are generated upon annealing.

Normally, broad band emissions are visible only when impurities or defects are present. Since hydrogen is famous for neutralizing defects and dopants in II-VI materials [9], we have also studied the effect of hydrogen passivation in these samples. Hydrogen annealed samples gives similar results as that of Argon annealed samples. From this result, we could also confirm the previous reports that these broad band emission corresponds to the isoelectronic Te bound excitons.

Figure 4 gives the PL spectra of the as grown and the annealed samples at 200 K. It is seen that there is not much of difference in the PL spectrum for the as grown sample and the sample annealed at 300 °C. It is to be noted that the FE emission can still be seen at 200 K for the as grown sample. The difference between the as grown and the sample A (annealed at 300 °C for 3 hour) can only be found at lower temperatures. After annealing at higher temperature, i.e., for the sample B (annealed at 350 for 3 hour), and C (annealed at 300 + 350 oC for 3 hr each) it is seen that two peaks starts dominating. The emission found at 2.17 eV and 2.22 eV respectively for samples B and C. corresponds to the Cu-defect complex emission (Cu-green) and they can be compared to the emission observed from the annealed ZnSe heterostructures[10]. The emission around 2 eV and 1.96 eV respectively for samples B and C corresponds to the emission from self assisted centers [10]. As the temperature and time of annealing is increased, the self assisted centers starts dominating and is clearly seen from the figure.

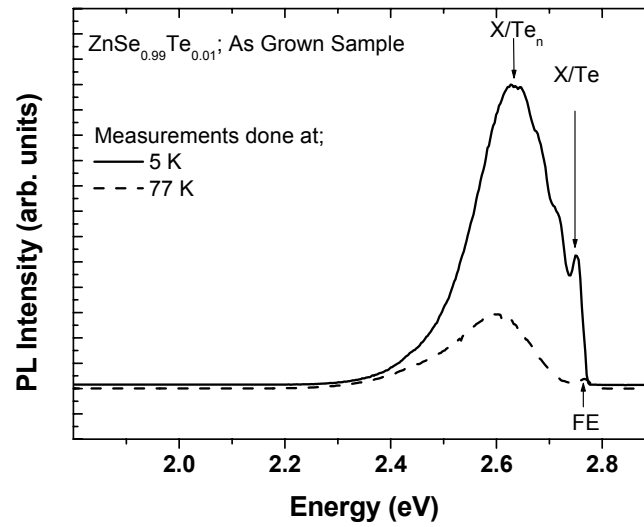
Figure 5 shows the room temperature and 200 K PL emission from the sample C. The Cu green emission which is observed at 200 K is very much diminished and the self activated centers dominates at the RT. This emission is around 1.95 eV. The free exciton emission (2.68 eV) can still be found in the sample even at room temperature and this confirms that the epilayer is still of good quality.

## Conclusion

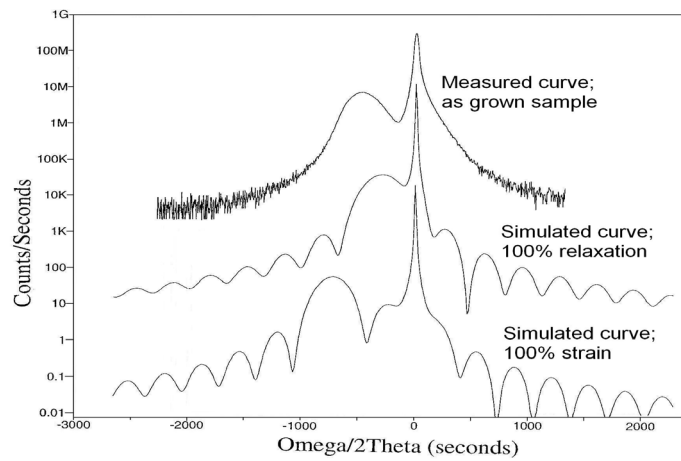
We have done thermal processing experiments on  $\text{ZnSe}_{1-x}\text{Te}_x$  with  $x < 1\%$ . Hydrogen passivation studies done on these samples confirm the previously obtained results that the broad band emission at 2.6 eV is due to the Te bound excitons. For the first time, our studies show that proper thermal processing of these samples can give room temperature emission around yellow region. We propose that precise thermal processing of these samples could be used for fabricating room temperature lasers in the visible region.

**Table I:** The  $\text{ZnSe}_{0.99}\text{Te}_{0.01}$  epilayer was annealed in Argon gas at 0.8 atm pressure at different temperature for 3 hour as listed in the table.

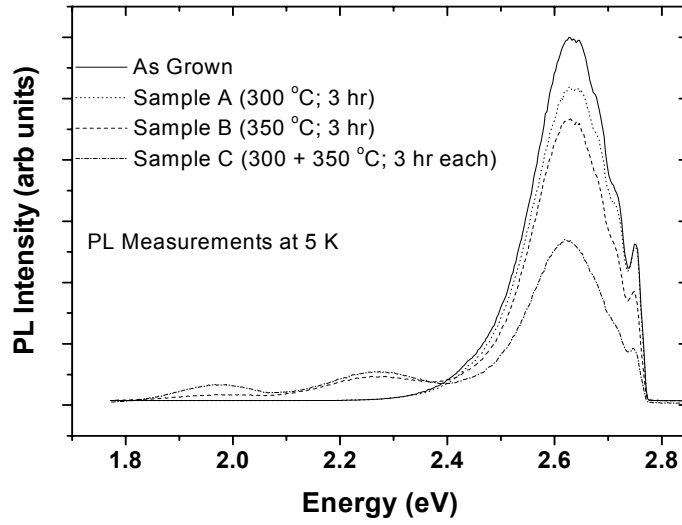
Sample	Temp. of annealing ( $^{\circ}\text{C}$ )
A	300
B	350
C	300 + 350



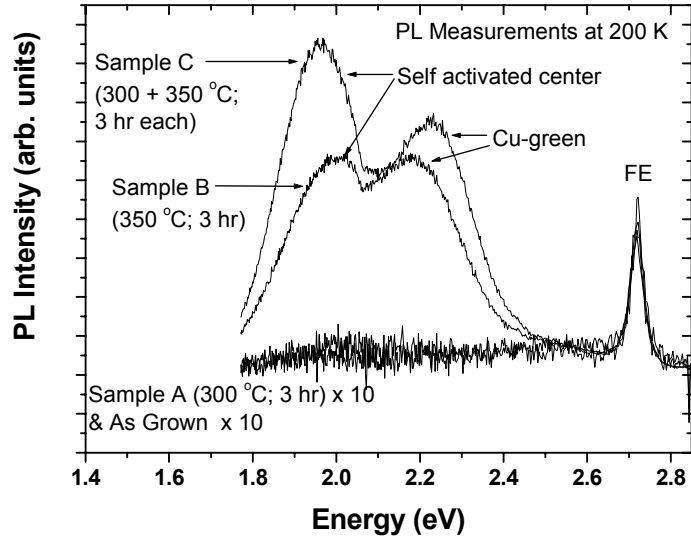
**Figure 1:** PL spectra at 5 K and 77 K of the  $\text{ZnSe}_{1-x}\text{Te}_x$  ( $x < 1\%$ ) as grown samples.



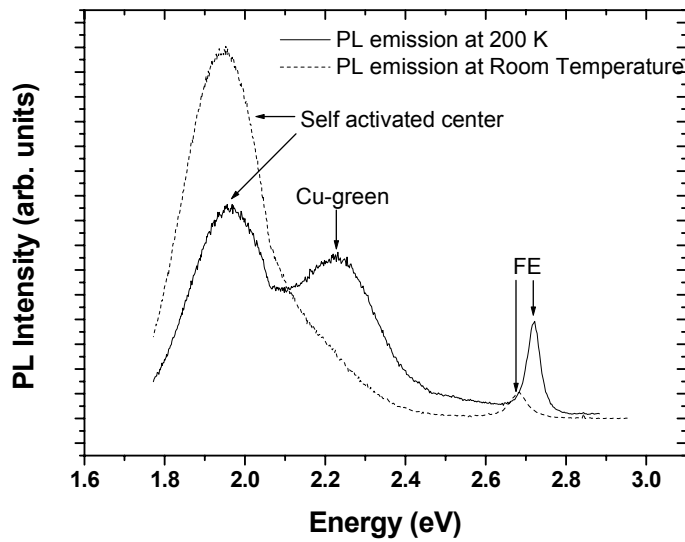
**Figure 2:** High resolution X-ray diffraction rocking curves (004 symmetric reflection) of the as grown sample, Measured, Simulated with 100 % relaxation, Simulated with 100 % strain.



**Figure 3:** PL spectra at 5 K of the as grown sample and the annealed samples.



**Figure 4:** PL spectra at 200 K of the as grown and the annealed samples.



**Figure 5:** PL spectra of the sample C (300 + 350 °C of annealing for 3 hr each) at 200 K and Room temperature.

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# Paper VIII

Post-Growth Process Relaxation Properties and  
Interlayer Diffusion of Strained  $\text{Cd}_{0.92}\text{Zn}_{0.08}\text{Te}/$   
 $\text{Cd}_{0.83}\text{Zn}_{0.17}\text{Te}$  Quantum Well Heterostructure Grown by  
Molecular Beam Epitaxy



# **Post-Growth Process Relaxation Properties and Interlayer Diffusion of Strained $\text{Cd}_{0.92}\text{Zn}_{0.08}\text{Te}/\text{Cd}_{0.83}\text{Zn}_{0.17}\text{Te}$ Quantum Well Heterostructure grown by Molecular Beam Epitaxy**

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## **Abstract:**

The post growth structural stability regarding relaxation, defect propagation interlayer layer diffusion, and Zn precipitation and/or out diffusion in  $\text{Cd}_{0.83}\text{Zn}_{0.17}\text{Te}/\text{Cd}_{0.92}\text{Zn}_{0.08}\text{Te}/\text{Cd}_{0.83}\text{Zn}_{0.17}\text{Te}$  quantum well (QW) heterostructures grown on (001) oriented  $\text{Cd}_{0.88}\text{Zn}_{0.12}\text{Te}$  substrates at 300 °C by molecular beam epitaxy is investigated. The investigated heterostructures were subjected to post growth thermal treatment in an ambient atmosphere in a temperature range between 280 °C and 550 °C for 3 hours each. We have used high-resolution x-ray diffraction as the main characterisation tool. High resolution rocking curves (HR-RC) as well as the powerful two-dimensional reciprocal space mapping (2D-RSM) was employed in both symmetrical as well as asymmetrical reflections. The results indicate that at a post growth temperature cycle of 350 °C for 3 hours; slight modification of the  $\text{Cd}_{0.83}\text{Zn}_{0.17}\text{Te}/\text{Cd}_{0.92}\text{Zn}_{0.08}\text{Te}$  barrier/QW heterointerface smoothness is affected. This indicates the onset of migration of Zn atoms at this post growth temperature time cycle. At 450 °C, this effect is more pronounced and seen as the complete disappearance of thickness fringes. For higher post growth thermal treatment of 550 °C for 3 hours, high relaxation level accompanied by Zn content reduction is observed. A reduction of the Zn content down to 0.11 fractional value in the thick  $\text{Cd}_{0.83}\text{Zn}_{0.17}\text{Te}$  barrier is attributed to Zn out diffusion and/or Zn precipitation.

## 1. Introduction:

The technological importance of CdTe as detectors [1, 2], solar cells, wave guides and as a better lattice matched substrate for other II-VI materials has prompted a great deal of work on this heterostructure system since the last decade [3, 4]. With the improvement in epitaxial growth techniques, an alloy of CdTe with Zn produces an improved crystalline quality material. By varying the percentage of Zn concentration, the lattice parameter of the material could be manipulated [5]. Modulation doping of this material was also accomplished by the improvement in epitaxy. Confined low dimensional (quantum wells) modulation doped heterostructures were thus developed and this led to both theoretical and experimental fundamental studies on their low temperature exciton dynamics and magneto optic properties [6, 7]. These investigations have also brought in the discovery of a new excitation state in 2-D electron gas: the negative and positive trion in Te based QWs [8].

There have been different investigations using X-ray diffraction technique on some II-VI heterostructures grown on GaAs substrates [9]. However, the growth of II-VI heterostructures on GaAs has not produced high device quality heterostructures, as this heterostructure system may possess a large mismatch of lattice parameters and a difference in thermal expansion coefficient. Today,  $\text{Cd}_{1-x}\text{Zn}_x\text{Te}$  substrates are commercially available in the market. These are used as lattice matched substrates for magneto-optic II-VI structures like CdMgTe, CdHgTe etc. The exploitation of Te based material heterostructures into various optical and electrical devices require a lot of process steps that involves post-growth annealing cycles at various stages. The device characteristics can either decrease or increase depending on the temperature-time cycle. The deleterious impact of annealing in QWs is that it can altogether change the structural characteristics of the material. Specially, for strained heterostructures, an onset of relaxation will lead to a change in the band alignment and hence alter the expected device performance. Thermal annealing can lead to interlayer diffusion between barrier and the well region. The effect of annealing on Cd based ZnSe materials have been studied by techniques like photoluminescence, secondary mass spectrometry and other techniques as

well [10, 11]. There are also investigations on the inter-layer diffusion of CdZnTe heterostructures which was performed by using x-ray diffraction [12].

Both p- and n-type doping are still an active area of research in most of the II-VI materials. This is because an effective doping concentration is difficult to be achieved in them. There are several theories proposed on the doping characteristic of these materials [13-15]. Nitrogen is found as an active p-type doping in both Se based and Te based materials. But theoretical value of doping density contradicts the experimental value that is still not achievable in these heterostructures. One of the possible reasons for this would be the formation of N-H complex because hydrogen based heterostructures are widely used for their epitaxial growth [16]. In ZnSe based materials compensation can take place by the formation of complexes with selenium vacancy [17], formation of nitrogen complex and nitrogen getting compensated through interstitial vacancies [18]. It is established that hydrogen passivation of acceptors can be obtained in these materials by annealing them in hydrogen atmosphere, while de-passivation can also be obtained by annealing them a second time in an inert atmosphere [19]. Also, post growth thermal annealing of as grown heterostructures can activate the acceptors, which are then passivated by hydrogen, thus increasing the acceptor concentration [20-23].

With the sole aim of obtaining hydrogen passivation of the acceptors in strained  $\text{Cd}_{1-x}\text{Zn}_x\text{Te}$  based QW heterostructure, we have performed post-growth thermal treatment on the present heterostructure in an atmosphere of deuterium ( $\text{D}_2$ ) at various temperatures. The non-destructive powerful high-resolution x-ray diffraction (HR-XRD) technique is used as the main characterisation tool. We have used both high resolution rocking curves (HR-RC) and two-dimensional reciprocal space mapping (2D-RSM), to monitor the strain status and the evolution of the structural changes after the post-growth thermal treatment.

## **2. Experimental:**

Nitrogen doped  $\text{Cd}_{0.92}\text{Zn}_{0.08}\text{Te}/\text{Cd}_{0.83}\text{Zn}_{0.17}\text{Te}$  (CZT) QW were grown in a

Molecular Beam Epitaxy (MBE) system. The growth temperature was optimised at 300 °C. The substrates were (001) CZT with 12% Zn concentration. By controlling the CdTe-ZnTe flux, the correct alloy concentration was obtained. Typical growth rates were ~0.6 monolayers per second for the barrier and 0.5 monolayers per second for the well. The samples used were single QW structures. The barrier layer (both bottom and top) for the single QW is approximately 1000-Å-thick CZT (with a nominal 17% Zn) layer. The well layer is a CZT (8% Zn) alloy with nominal thickness of 40 ML (130 Å). The samples were sealed in quartz ampoules filled with 0.8 atmosphere D<sub>2</sub> and a small amount of Cd. The introduction of Cd in the annealed environment was due to compensate any out diffusion of Cd atom thus reducing surface degradation etc [24]. These quartz ampoules were annealed at various temperatures for 3 hours. The samples are labelled CZT-ref, for the as grown sample, CZT-280, CZT-320, CZT-350, CZT-450 and CZT-550. The numbers in this notation refer to the annealing temperature value in degrees C, which were 3 hours for each case.

The present structural evolution study was performed by high-resolution X-ray diffraction measurement. High-resolution rocking curves and two-dimensional reciprocal space mapping were performed on these heterostructures. We have employed a multi-crystal high resolution Philips Extended X-pert material Research Diffractometer, equipped with a computer-controlled motorised goniometer. This diffractometer enables the optimisation of the scattering angles with angular step sizes down to  $1.0 \times 10^{-3}$  degrees for the angles of incidence and reflection, and step sizes down to  $1.0 \times 10^{-2}$  degrees for the angles of rotation around the surface normal and around the in plane horizontal directions. Both double crystal and triple axis configurations were employed. A four crystal Ge (220) Bartels monochromator is used to collimate the Cu-tube x-ray incident beam with a divergence of 12 arcsec, and for secondary optics, the rocking curves were collected using a slit with a width of 0.5 degree. For collecting the 2D-RSMs, the diffractometer was set into the extended configuration and a combination of mirror and a Bartels monochromator was used. The addition of a mirror is necessary as it increases the intensity by at least an order of magnitude while still maintaining a low background noise level.



Traditionally, rocking curves are used to analyse strained/relaxed heterostructures. This analysis is mainly done by the evaluation of the full-width at half maximum (FWHM) of the layer peak. However, the elongation and broadening of the FWHM of a layer can be due to many factors, such as defects, strain and or composition variations, and finite thickness effect. This implies that the FWHM from rocking curves can not be used as an absolute figure of merit due to the difficulty in separating these effects. For triple axis configuration, which is an improvement over the rocking curve configuration, a Ge (220) triple-bounds channel-cut crystal, which gives a divergence of less than 12 arcsec was employed. This reduction of the detector acceptance angle to less than 12 arcsec will imply the reduction of the probing size to similar dimensions and hence the possibility of resolving the different orientation distributions of the diffracted beam, and acquire a two dimensional iso-intensity contours. A two dimensional map is in principle  $\theta$  and  $\theta/2\theta$  coupled scan with an offset in  $\theta$ . A  $\theta/2\theta$  scan probes the variations in the interplanar spacing of a given set of diffraction planes. While a  $\theta$  scan probes the angular variations of a fixed interplanar spacing. Having the combination of these two scan plotted in two dimensions, these contributions can be separated.

### **3. Theory and extraction procedure:**

If we have a heterostructure with a combination of thick and thin layers (as in our present case) then the thick layer (the barrier) contributes to diffracted intensity mainly and give clear individual peaks in double crystal rocking curves. The role of the second thin layer (QW) results in phase shift caused by it for waves scattered by upper thick layer. Hence the lattice parameters and composition of the barriers can be estimated directly from angular positions of the peaks from a HR-RC. To determine the QW composition a simulation of the heterostructure and a fitting to experimental measurement is needed. The simulation procedure adopted here is based on Takagi-Taupin theory (Halliwell et al. J. Cryst. Growth 68, 523 (1984)) assuming unrelaxed nondistorted heterostructure.

Measurement of asymmetrical reflection (115) was used for the determination of the relaxation level in the investigated heterostructure. From  $\theta$  and  $2\theta$  angular position of the corresponding diffraction centres in the acquired 2D-RSM, the relative difference of lattice parameters of an epilayer and substrate ( $(\Delta a/a)_p$  (parallel to surface) and  $(\Delta a/a)_n$  in a surface normal direction) can be deduced. However for relaxed structures there might exist a misorientation between the substrate and the layer as a result arising from the specific dislocation network structure. The value of this misorientation is determined from 2D-RSM of a symmetrical reflection (004) measured at the same azimuth position of the sample as the one used for acquiring the asymmetric 115-reflection. If the misorientation is absent the reflection centres of the layer(s) and the substrate are situated at a line parallel to the surface normal coinciding with the diffraction vector. A deviation of the layer peak from this direction (in  $\theta$ -scale) gives a projection of the misorientation angle on the diffraction plane ((110) in our case). This angle is then subtracted from  $\theta$ -position of the layer rlp in asymmetrical reflection map to obtain a corrected angular position. This corrected value is then used further for the calculation of  $(\Delta a/a)_n$  and  $(\Delta a/a)_p$ . From these lattice mismatches a difference between Zn-content in layer and substrate ( $x_1 - x_0$ ) and relaxation level  $r = \Delta a_p / (a_{x1} - a_{x0})$  where  $a_{x1}$  and  $a_{x0}$  are bulk parameters of CdZnTe with Zn-content  $x_1$  and  $x_0$  respectively, is then obtained. A more descriptive similar procedure can be found in [25].

#### 4. Results and discussion:

We first determined and confirmed the Zn content of the 001 oriented  $\text{Cd}_{1-x}\text{Zn}_x\text{Te}$  substrate. This is done by the measurement of the exact  $2\theta$  position of the substrate peak. Then the lattice parameter is determined and the corresponding Zn content is then derived. We found that the Zn content of the substrate is consistent with the expectation, i.e. 12% Zn fraction.

Figure 1 shows the measured and simulated 004-rocking curve of the as grown sample (CZT-ref). The main layer peak on high angle side of the substrate peak corresponds to reflection from the thick barrier layer and an influence of thin QW-layer

becomes apparent in the intensity distribution on the tail as explained above. The existence of thickness fringes on both low and high angle side shows that the grown heterostructure is of high structural quality with sharp interfaces between the QW, the barrier regions, and the substrate. The simulation was carried out assuming fully strained (unrelaxed) state of the heterostructure. The best fitting of the simulated HR-RC to experimental one (Fig.1a) was obtained for a  $\text{Cd}_{0.88}\text{Zn}_{0.12}\text{Te}$  substrate, a  $\text{Cd}_{0.831}\text{Zn}_{0.169}\text{Te}$  barrier with thickness  $t = 297$  monolayers (for both the top and bottom barrier), and finally a  $\text{Cd}_{0.92}\text{Zn}_{0.08}\text{Te}$  QW with a thickness of  $t = 30$  monolayers. Comparing the rocking curves a and b in figure 1, it is evident that the simulation has fairly reproduced all the main features of the measurement. As the lattice constant of ZnTe ( $a=6.1037\text{\AA}$ ) is smaller than that of CdTe ( $a=6.4825\text{\AA}$ ), the  $\text{Cd}_{0.92}\text{Zn}_{0.08}\text{Te}$  QW is under compression strain while the  $\text{Cd}_{0.821}\text{Zn}_{0.169}\text{Te}$  barrier region is under tensile strain when grown on  $\text{Cd}_{0.88}\text{Zn}_{0.12}\text{Te}$  001 substrate.

Figure 2 shows the 004 HR-RCs of samples annealed at various temperatures, CZT-280, CZT-320, CZT-350 and CZT-450 along with the as grown sample CZT-ref. As can be clearly seen from Fig. 2, a strong presence of thickness fringes still exist up to post-growth thermal treatment of  $320\text{ }^{\circ}\text{C}$  for 3 hours. For post-growth thermal treatment of  $350\text{ }^{\circ}\text{C}$  for 3 hours the fringes become weaker. At  $450\text{ }^{\circ}\text{C}$  they disappear completely although the barrier peak position is not shifted. The fact that the barrier peak has the same angular position implies that the average composition remains unaltered and only slight structural changes have been introduced by this temperature-time cycle.

Figure 3 displays a 2D-RSM of the as grown sample, around the (a) 004 symmetric, and (b) 115 asymmetric reciprocal lattice points rlp-s. It is seen that the substrate and layer peaks lie in a same straight line along the surface normal for both cases (vertically in reciprocal lattice axis units  $k_x$  -parallel to surface and  $k_z$  normal to it). It follows from these maps that there is no any miscut or crystallographic tilts between the substrate and the grown layer(s) and the latter is fully strained. Besides no elongation along the  $\omega$ -scan direction is present in the intensity distribution around both symmetric and asymmetric rlp-s which indicates an absence of any mosaic structure and defects of

dislocation type. The fractional Zn content in the as grown barrier layer extracted from the peak and layer centre position in 115-map was found to be  $0.17 \pm 0.001$ , which is the same value as obtained from the 004-rocking curve (Fig. 2).

To follow the structural evolution of the investigated heterostructures under the post-growth thermal treatment, the symmetric and asymmetric 2D-RSMs of all samples were measured and analysed. The symmetric 2D-RSM (not shown) indicates no tilt between the substrate and layer existed. Figure 4 presents the 115-2D-RSM of the as grown CZT-ref, and the case of four annealed structures as indicated. As it is evident, all the samples presented in this figure are coherent even after post-growth thermal treatment of 450 °C for 3 hours, that follows from the alignment of the  $\text{Cd}_{0.88}\text{Zn}_{0.12}\text{Te}$  substrate and  $\text{Cd}_{0.83}\text{Zn}_{0.17}\text{Te}$  barrier layer peaks along the surface normal. Quantitatively this is simply estimated from the ratio between  $2\theta$  and the  $\theta$  differences of the substrate and the corresponding layer peaks. For all samples, this ratio was found to be constant and equal to  $(1 - \gamma_0/\gamma_h) = 1.47$  (where  $\gamma_0$  and  $\gamma_h$  are the directional cosines of incident and diffracted beams) corresponding to an intensity distribution along the surface normal for 115-reflection. This indicates that all post-growth thermally treated samples (up to 450 °C for 3 hours) remains in their as grown strain state with relaxation factor below the detection level (which is around 0.01%).

In addition it follows from the vertical separation between the layer and substrate peaks in Fig. 4 that the average composition of the barrier layers remains unchanged for post-growth thermal treatment up to 450 °C (the Zn content was found to be  $0.17 \pm 0.001$ ) confirming the results obtained from 004-rocking curves. This fact indicates that there is no considerable diffusion between the layer and substrate as well as out-diffusion from the heterostructure up to a temperature of 450 °C for 3 hours. Nevertheless we can not exclude a diffusion process between the QW and the barrier layers leading to effect on the smoothing of the corresponding interfaces. Note that this may be a reason of disappearance of the thickness fringes in 004-HR RC (see Fig. 2). Besides, following and comparing carefully the evolution of the iso-intensity contours of the substrate and barrier layer peaks in Fig 4a-d, we can see that some slight structural changes have taken place.

Particularly the slight elongation of the low count iso-intensity contours along the  $\omega$ -scan direction of the substrate and layer peaks is observed for sample CZT-450 (Fig. 4d). The origin of this elongation can be attributed to the effect of scattering from locally relaxed regions close to dislocations at initial stage of formation i.e. mosaicity onset.

The post-growth thermal stability of sample CZT-550 has shown a quite different result. Figure 5 represents the symmetric and asymmetric RSMs of this sample. Investigating the angular positions of the substrate and the barrier layer, it is observed from the 004 symmetric 2D-RSM, the fact that both the layer and substrate have the same  $2\theta$  value, while the  $\theta$  position of the substrate is different from that of the layer. However, the corresponding  $2\theta$  positions obtained from the 115 asymmetric 2D maps indicate that the  $2\theta_{\text{layer}}$  is smaller than  $2\theta_{\text{substrate}}$ . Qualitatively this is explained as follows: at post-growth annealing of 550 °C, two processes occurred, relaxation (with layer misorientation with respect to the substrate), and Zn out diffusion and/or precipitation. For more clarification compare figures 5a and 5b together with figure 5c. The relative  $2\theta$  and  $\theta$  peak positions obtained from the 004 2D map indicates that the Zn content of the layer is close to that of the substrate. But from the 115 2D-RSM we see that  $2\theta_{\text{layer}}$  is smaller than  $2\theta_{\text{substrate}}$ . This means that the parallel lattice constant of the layer is larger than that of the substrate and the Zn content in the layer is smaller than in the substrate. The approximated fractional Zn content obtained for the layer in this case was found to be less than 0.11. The difference between this 0.11 and the as grown value of 0.17 is believed to have generated precipitates as indicated by the appearance of diffused scattering in an omega scan (not shown). The other explanation of the Zn concentration reduction after annealing at 450 °C may probably be due to out diffusion of Zn-atoms from sample surface.

## 5. Conclusions:

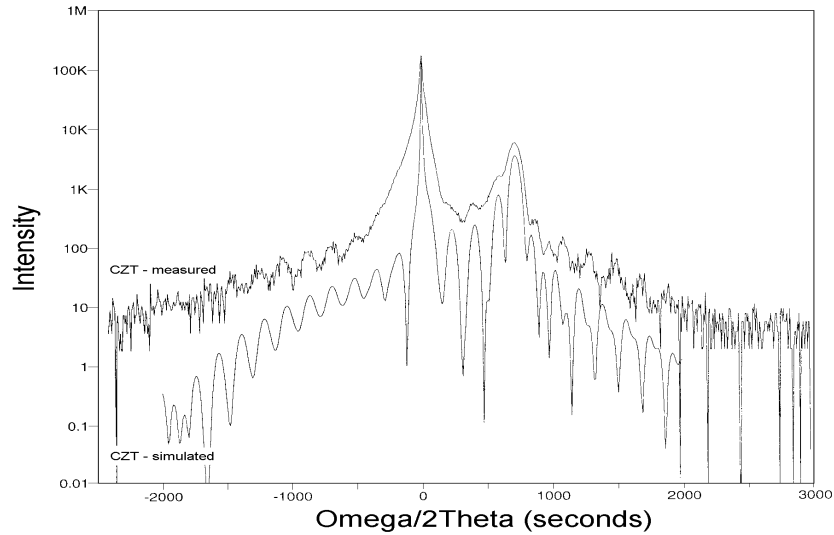
The strain sensitive 2D-RSM tool and HR-RC were employed to investigate the post growth thermal stability of  $\text{Cd}_{0.92}\text{Zn}_{0.08}\text{Te}/\text{Cd}_{0.83}\text{Zn}_{0.17}\text{Te}$  QW heterostructure for samples grown at 300 °C by molecular beam epitaxy. An indication of roughing the

interface and/or interlayer diffusion between the thin QW and the thick barrier layer starts to appear at post growth thermal treatment of 350 °C. However, the thick barrier remains almost in it's as grown state up to a temperature time cycle of 450 °C for 3 hours. Only an indication of slight mosaicity was observed. At post growth temperature annealing of 550 °C for three hours a high relaxation level accompanied by Zn out diffusion and/or precipitation appears very clearly. At this temperature time cycle a reduction of the Zn content down to 0.11 has taken place. The present structural investigation indicates that Zn migration, precipitation and out diffusion in such heterostructures starts to take place at much lower temperature than in  $\text{Cd}_{1-x}\text{Zn}_x\text{Te}$  bulk layers.

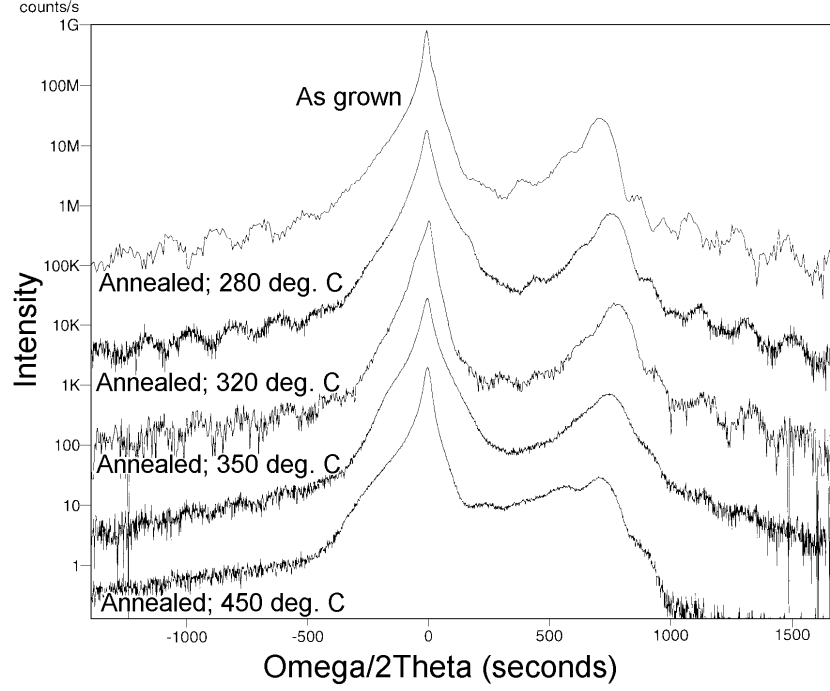
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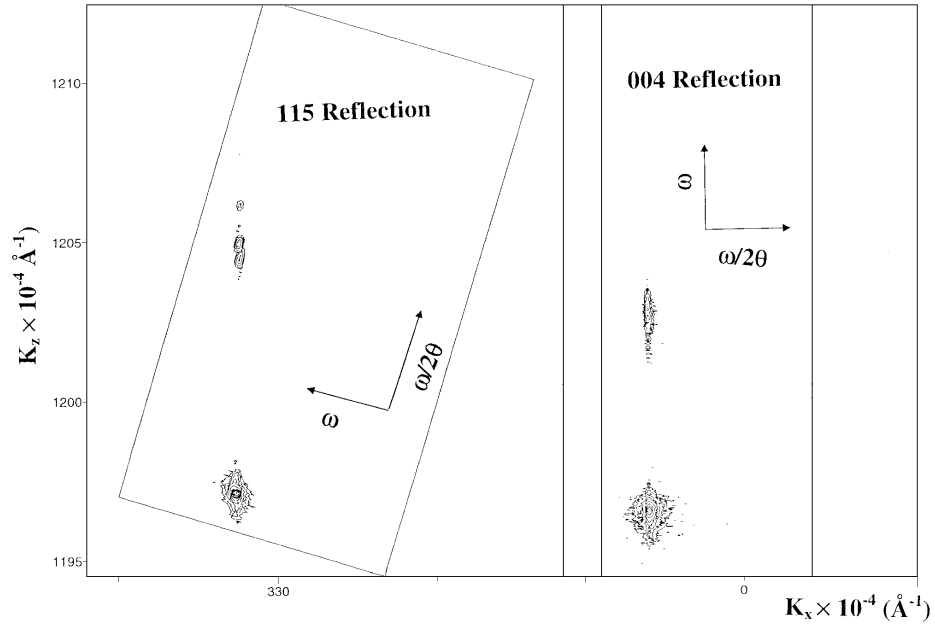
### Figures:



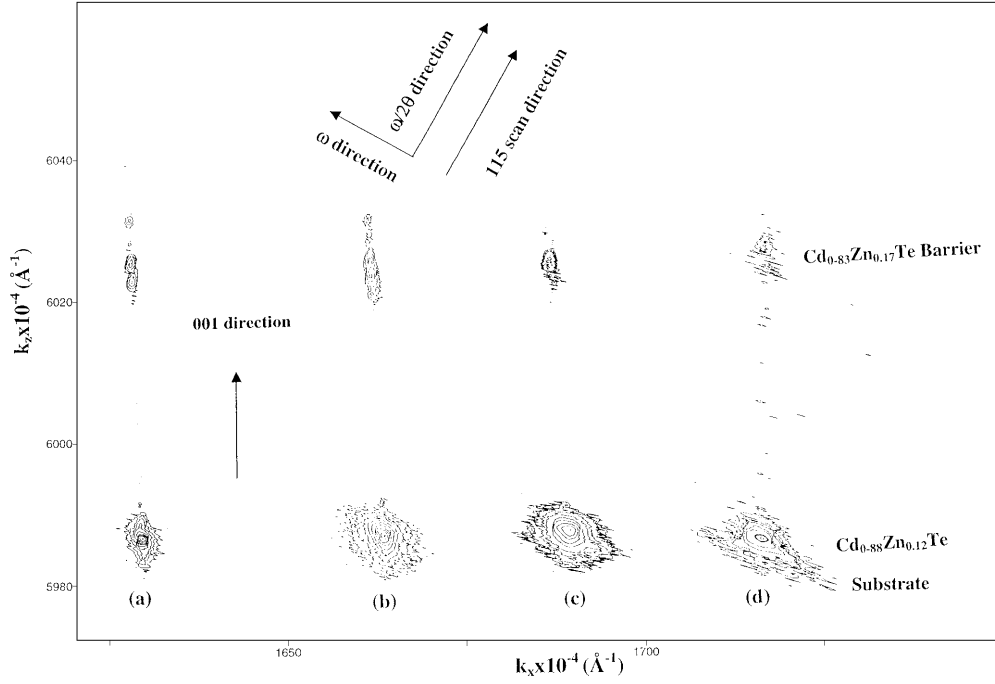
**Figure 1:** The measured (a), and simulated (b) 004 rocking curve of the heterostructure. The simulation parameters were  $\text{Cd}_{0.88}\text{Zn}_{0.12}\text{Te}$  001 substrate, a  $\text{Cd}_{0.831}\text{Zn}_{0.169}\text{Te}$  barrier with thickness  $t = 297$  monolayers for both the top and bottom barrier, and finally a  $\text{Cd}_{0.92}\text{Zn}_{0.08}\text{Te}$  Q.W. with a thickness of  $t = 30$  monolayers.



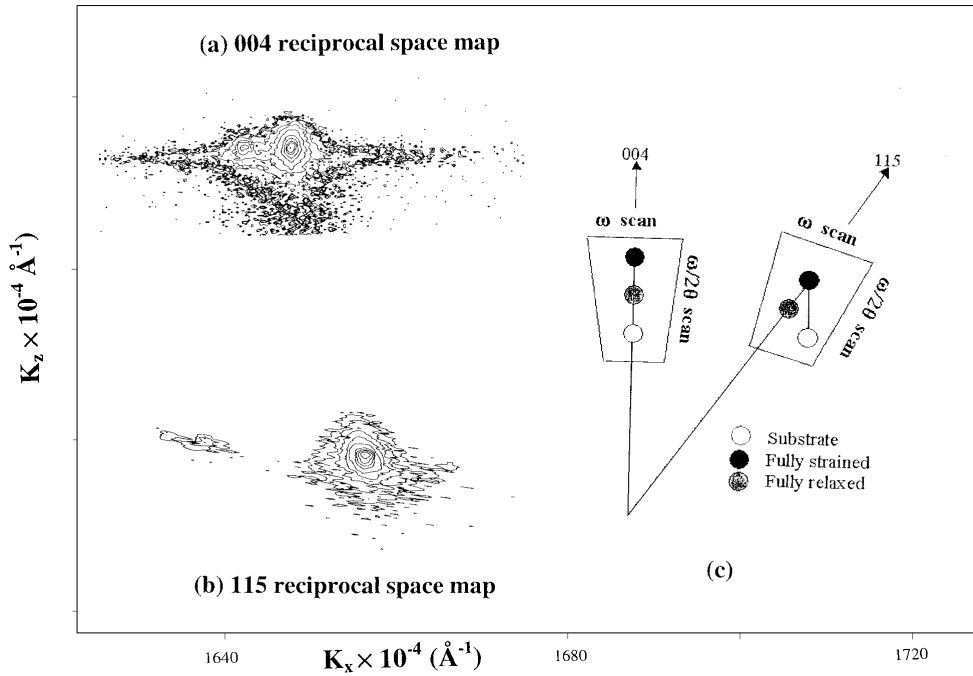
**Figure 2:** The 004 HR-RC of the as grown CZT-ref and the annealed samples up to a temperature of 450 °C for 3 hours each as indicated in the figure.



**Figure 3:** A typical 2D-RSM around the 115 (a), and 004 (b) of the as grown CZT-ref heterostructure both in reciprocal lattice ( $k_x$  and  $k_z$ ) unit axis.



**Figure 4:** A typical 2D-RSM around the 115 asymmetric reciprocal lattice point for the CZT-ref (a), CZT-280 (b), CZT-325 (c), and CZT-450.



**Figure 5:** A typical 2D-RSM around the 004 (a), and the 115 (b) asymmetric reciprocal lattice point of sample CZT-550. The schematic diagram (c) represents the relative



position of a substrate and epitaxial layer in a symmetric 004 and asymmetric 115 2D-RSMs. For fully tensile strained and fully relaxed cases are shown when no misorientation between the layer and the substrate exists. The trapezoid represents the area mapped in reciprocal space.

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