Addressing modes of ferroelectric liquid crystal displays

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ABSTRACT

The paper discusses some aspects of the construction of multiplexing waveforms for ferroelectric liquid crystal devices. Conventional addressing methods are opposed to more recent ones, where time overlap of the selection waveforms and asymmetries between initial and final switching slopes are extensively utilized. A general classification of addressing modes is presented and representative addressing schemes are discussed in detail. A new "Split Writing (SW)" addressing scheme is proposed.

Keywords: SSFLC, ferroelectric liquid crystals, matrix addressing, multiplexing, displays

INTRODUCTION

Most of the Surface-Stabilized Ferroelectric Liquid Crystal (SSFLC) applications require switching of many display elements, so-called pixels. Only in very small displays, like indicators, each pixel can be driven directly. Instead, the electrodes in a typical SSFLC display device form a matrix. The area where a row and a column electrode overlap forms a picture element. Such a pixel experiences a superposition of voltage sequences supplied to both its electrodes. An image can than be created by sequentially applying selection waveforms to the row electrodes while supplying adequate data waveforms simultaneously to all the columns.

The design of such waveforms - an addressing scheme - is not a trivial task. The aim is to reach as short selection time as possible and a good optical contrast. The overall dc content in the applied waveforms has to be zero to avoid degradation of the cell. The addressing should also be flicker-free and reasonably insensitive to variations in temperature and cell thickness.

CONVENTIONAL ADDRESSING SCHEMES

Early multiplexing schemes were based on a simple assumption that switching occurs when a pulse of critical voltage-time product is applied to a pixel.[1] Moreover, it was intended to be completed within the row selection time. Since each switching pulse requires a dc-compensating counter pulse, this approach resulted in four-five slot schemes[2,3] or a two-slot two-field addressing[4] (the expression "two-field" meaning that two complete addressing runs have to be performed to write the whole picture). The total time necessary

to address each row was thus much longer than the switching time of the liquid crystal material.

Such long line-addressing times resulted in slow refreshing of the liquid crystal screen (low frame rate). A first approach to improve the addressing speed was to simplify the selection sequence. Instead of creating dc-compensated waveforms capable of switching the pixel up or down, the pixel was first erased (switched to one chosen state) and than either written (switched to the opposite state) or not. The number of required time slots was thereby reduced to two. A problem was still to ensure good erasing. In the GEC-scheme[5] it was solved by making the amplitude of the erasing pulse larger. The resulting asymmetry was then compensated by a small dc-offset between the selections.

Maltese *et al* proposed[6,7] that the same effect could be achieved at no cost by extending the addressing sequence over the non-selected rows and eventually alternating selection polarity for consequtive frames. The erasing pulse was made three-slots wide[8] "borrowing" two time slots from the preceding selection sequence. This addressing scheme was practically implemented in a simplified version N31, where "N" stands for "normal" mode, and was further improved by reducing the erase pulse to two slots (N21).[8] The LETI-Bari N21 addressing scheme was fast enough to allow demonstration of grey-shade video pictures on a small display.[9]

At this point it is convenient to introduce a concept of the "control window" for each line, defined as

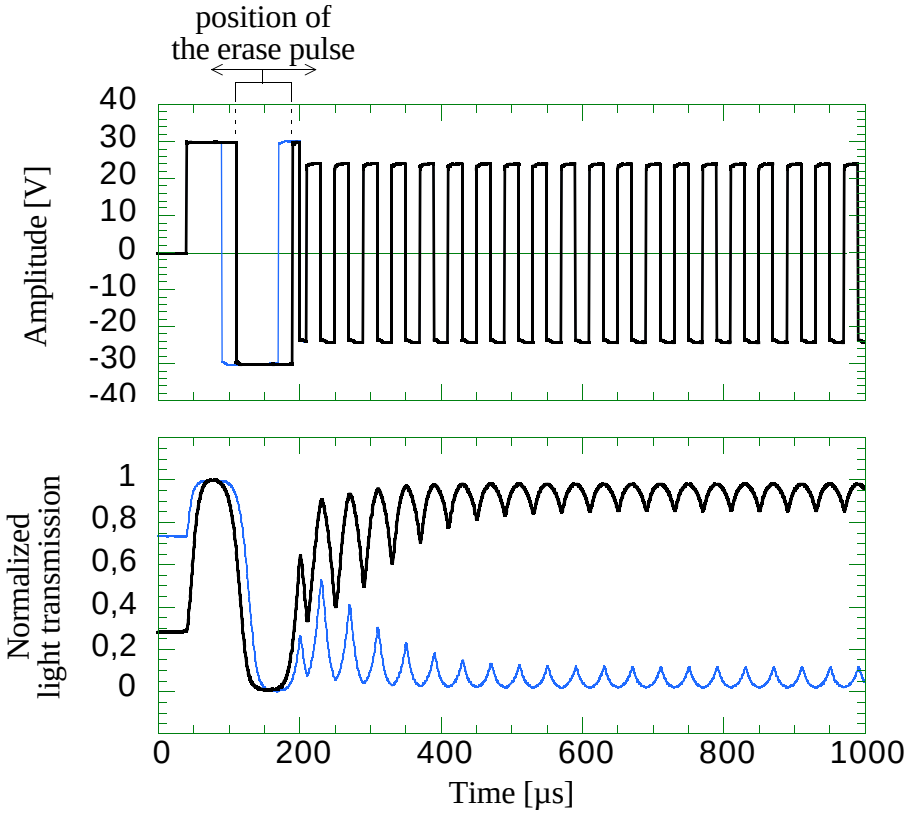

Figure 1. A hf square wave completes the switching process (polymer aligned cell filled with ZLI4655/000 mixture). Partial switching achieved by varying the position of the erasing pulse. The optical response is normalized so it spans between 0 and 1.

the time period when the data intended for the desired pixel appear on its column electrode.

In the N21 scheme (cf. summary of addressing schemes in Figure 9) the superposition of the selection waveform before and during the first half of the control window with the data waveform produces a large pulse capable of switching the pixel into one state, say black, independently of the data outside the control window and the initial state of the pixel. Within the control window the amplitude of generated pulses depends on the supplied data. Thus, the pixel can either be switched to the white state or remain in the black state. The selection waveform is unbalanced and has to be inverted every frame to assure dc-compensation. Blanking occurs to the white and black state alternatively and the action of the data is reversed.

Further experiments revealed that a multiple erase sequence provides better separation from an initial state of the pixel and eliminates the necessity of the frame reversal.[8]

The addressing schemes discussed above are usually referred to as “low voltage” or “normal” modes. Their essential feature is the saturation in the response to the driving voltage before the writing pulse in the selection sequence. The final state of the pixel is controlled solely by the area of the writing pulse.

THE CROSSTALK

The superposition of data and selection waveforms inevitably produces, during non-selection time, so-called crosstalk pulses. These pulses were considered “disturbing” and efforts were made to reduce them. On the other hand, since the crosstalk pulses cannot be avoided, one should instead look for the way of using them. If well designed, the crosstalk pulses generate a dielectric torque which enhances the optical contrast by forcing the liquid crystal director into a position of higher optical extinction than the relaxed states.

A simple experiment, presented in Figure 1, shows that the dielectric torque can also be used to complete the switching process, thus allowing the shortening of the switching pulse itself.[10] Here a three-pulse, dc-balanced sequence of constant amplitude and total length was applied to an SSFLC test cell. The position of the erase pulse was shifted within the sequence in order to alter the width of the writing pulse. It allowed

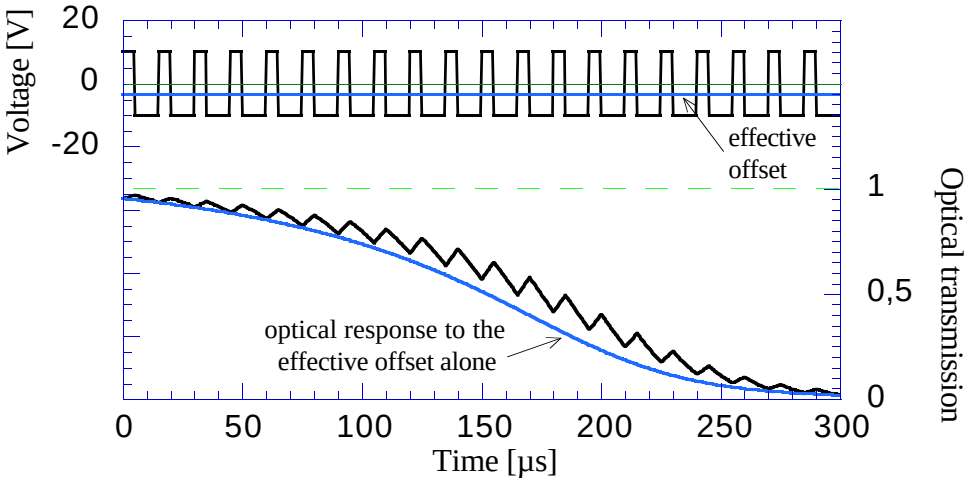

Figure 2. The effect of a long series of unbalanced data segments (simulation, ratio 2:1, ZLI4655/000 liquid crystal cell).

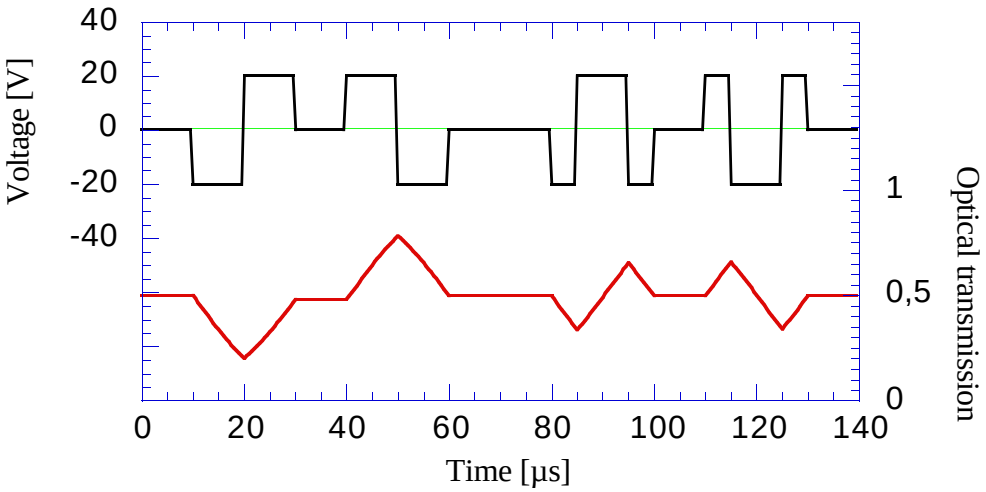

Figure 3. The optical response to different data waveforms (ZLI4655/000-cell, simulated). The 'crosstalk compensated' data waveforms (at right) do not affect the average state of the cell.

to obtain a well-controlled partial switching, which was than subjected to a high-frequency square wave.

As can be seen in Figure 1 the action of hf-voltage improves the switching threshold as it decreases the difference between the pulse after which the switching is completed by the dielectric torque and the pulse after which the liquid crystal director is totally forced back to the initial state.

During the scanning of a large display, each pixel experiences a crosstalk voltage for most of the time. It is thus important that the light transmission is not influenced by the actual data supplied to the column. A first, quite obvious requirement is that each data segment has to be dc-balanced - otherwise an offset stemming from long groups of the same data would cause switching, as shown in Figure 2.

Even if dc-balanced, the crosstalk pulses affect the momentary light transmission through the pixel. By correct design of the data sequence the average state of the pixel can be kept constant. In Figure 3 a typical data sequence consisting of a pair of pulses of opposite polarity (shown at left) is compared with the "crosstalk compensated" data sequence[6,15,16] (at right). Here a compensation pulse is divided in halves and placed at the beginning and end of the sequence.

BIPOLAR VS. MONOPOLAR SWITCHING PULSES

Figure 4 presents the optical response to the application of a bipolar and a monopolar switching pulse. It can be clearly seen that switching from a relaxed state is significantly shorter than switching from the saturated state in the sense that it requires a shorter writing pulse. This difference can be utilized in designing addressing schemes.

Examination of the switching trace during the first half of the bipolar pulse suggests that this part of the pulse could be shortened without changing its effect. It is obvious that diminishing or removing the

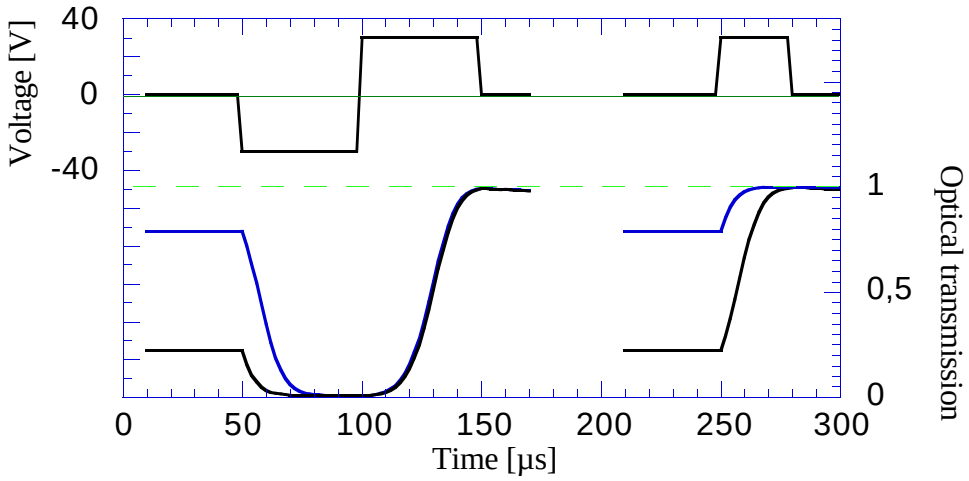

Figure 4. Bipolar versus monopolar switching (ZLI4655/000-cell, simulated). Bipolar switching requires longer writing pulse than the monopolar one. Initial optical transmission correspond to the relaxed black and white states, respectively.

counter pulse disturbs the dc-balance, but this can easily be compensated within the erase sequence preceding in time the writing pulse.

FAST ADDRESSING MODES

As the erasing sequence can be overlapped in time with the process of addressing other rows, one could also try to "borrow" some time from the neighboring control windows to construct the writing pulse. In such a case the control window would be shorter than the writing pulse. The threshold effect discussed so far was related to the area of the writing pulse. Obviously it is not possible, using a short control window, to sufficiently differentiate this area. We need thus to look for another effect which could be utilized.

We know that the biaxial dielectric torques counteract the switching in its initial stage and accelerate it in its final stage. So, if the area of the writing pulse is of an intermediate size between the switching and non-switching one, increasing or decreasing this effect during part of the writing pulse should produce the required difference in the optical response. This consideration makes up the base for new, fast addressing modes.

The control window of addressing should thus be placed where the effect of the biaxial dielectric torques is strongest, i.e. at the beginning or at the end of the switching slope. In the first case we get a so called "hampered writing" mode and in the second case - "stopped writing" mode.[11] These modes were originally discovered at higher amplitudes of selection waveforms, where the asymmetries in switching slopes caused by dielectric effects are most prominent. They were therefore often referred to as "high voltage" modes,[7,12,13,14,15] although they can be utilized also at quite moderate voltage levels.

The three basic addressing modes are schematically presented in Figure 5a-c. Recent investigations[17] show that the control window in the "hampered" addressing mode does not necessarily have to be placed at the very beginning of the writing pulse. In fact, a stronger hampering effect can often be achieved if the

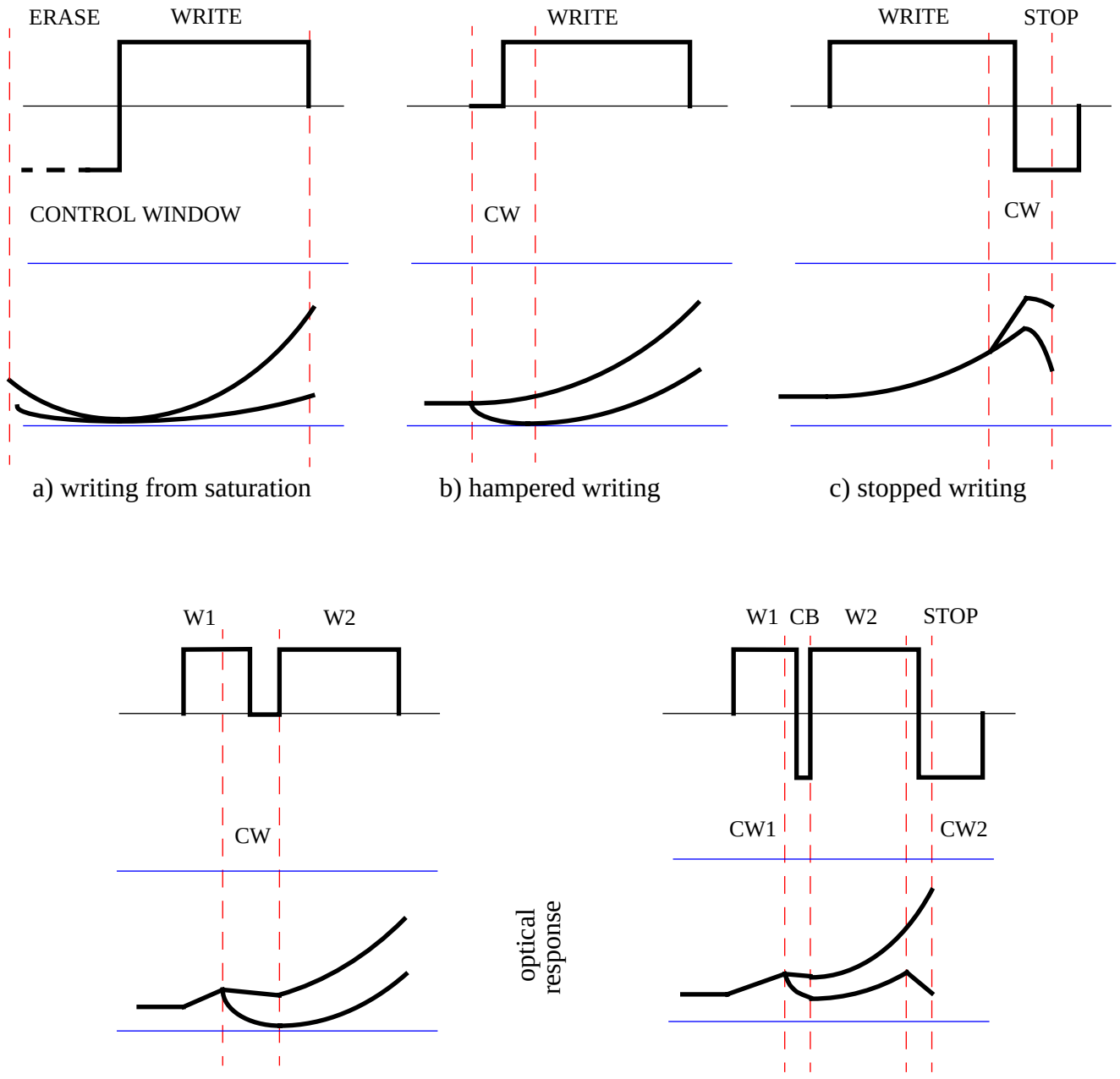

Figure 5. Proposed classification and essential features of addressing modes. The two traces in the optical response correspond to the effect of the data applied during the control window (CW). The switching is completed by the action of the crosstalk pulses (not shown). Figures a–c) present the basic addressing modes and d,e) present their variations discussed in this paper.

switching is allowed to start a short time before the control window. As sketched in Figure 5d, the writing pulse is split in two parts with the control window in between.

Obviously, it is possible to combine the presented addressing modes. Figure 5e shows a mixed mode, where the control window is split in two parts. The first one causes the hampering effect in the initial stage of switching and the other - the acceleration effect in its final stage. Both control sub-windows are much shorter in this case and extremely fast addressing has been recently reported[17] using this method.

In the following paragraphs we present addressing schemes representative for fast addressing modes. Our experiments have been performed using a dedicated LCD Waveform Generator of a new design, which has been described elsewhere.[18] This generator has eight channels capable of pulse amplitudes up to ±100 V at slew rate of 330 V/μs. It is controlled by a Macintosh computer with extensive software including on-line simulation of the optical response of the SSFLC cell. The simulation is based on the tilted-layers uniform-director model,[19] which, despite its simplicity, has proven capable of reproducing the behaviour of all known addressing methods. It has also been successfully used to calculate their operating regions. Not all parameters of the liquid crystal material, required by the model, can be found in the literature. In order to obtain missing parameters and adjust the entire set to the properties of the cell, we made a special series of experiments, where we both measured and simulated the delay time, the rise time and the slope of the optical response, and also the evolution of the field-on equilibrium states in a number of test cells.[20]

STOPPED WRITING MODE

An example of the "stopped writing" mode is the "Pause-Superfast" PS3 addressing scheme.[14,15] The addressed pixel is erased some time before the writing pulse, which is terminated by a stop pulse. The control window overlaps the end of the writing pulse and the beginning of the stop pulse. The "crosstalk-compensated" data waveforms are used.

Figure 6 presents the optical response of one pixel in a polymer aligned test cell filled with the Merck SCE8 low spontaneous polarization ferroelectric liquid crystal mixture. The amplitude of the selection waveform is 25 V and the data waveform – 13 V. The obtained slot time is 38 μs (at 28°C), which equals 152 μs line addressing time. The SCE8 is a relatively slow liquid crystal mixture and the same addressing scheme applied to a Merck ZLI 4655/000 cell at 40°C resulted in only 12 μs line addressing time with 42 V and 24 V amplitudes of selection and data waveforms, respectively.[14]

HAMPERED MODE – SPLIT WRITING PULSE

A new addressing scheme which should have a broad range of use is presented in Figure 7. It is of the hampered mode, but with a split writing pulse. In the figure it has been applied to the same cell as subjected to the PS3 scheme in Figure 6.

In the "Split Writing" (SW) addressing scheme the writing pulse is divided in two parts with an interruption in between. The "crosstalk-compensated" data waveforms are used. The control window overlaps the first writing pulse, the interruption period and the beginning of the second writing pulse. Prior to the writing sequence, the pixel is erased and allowed to relax to its ac-stabilized state. The first writing pulse initiates the switching, so that it reaches a more sensitive part of the slope. During the interruption the switching is, depending on the supplied data, either allowed to continue in a smooth way or counteracted. As can be clearly seen, the dielectric torques generated during the control window differ significantly in

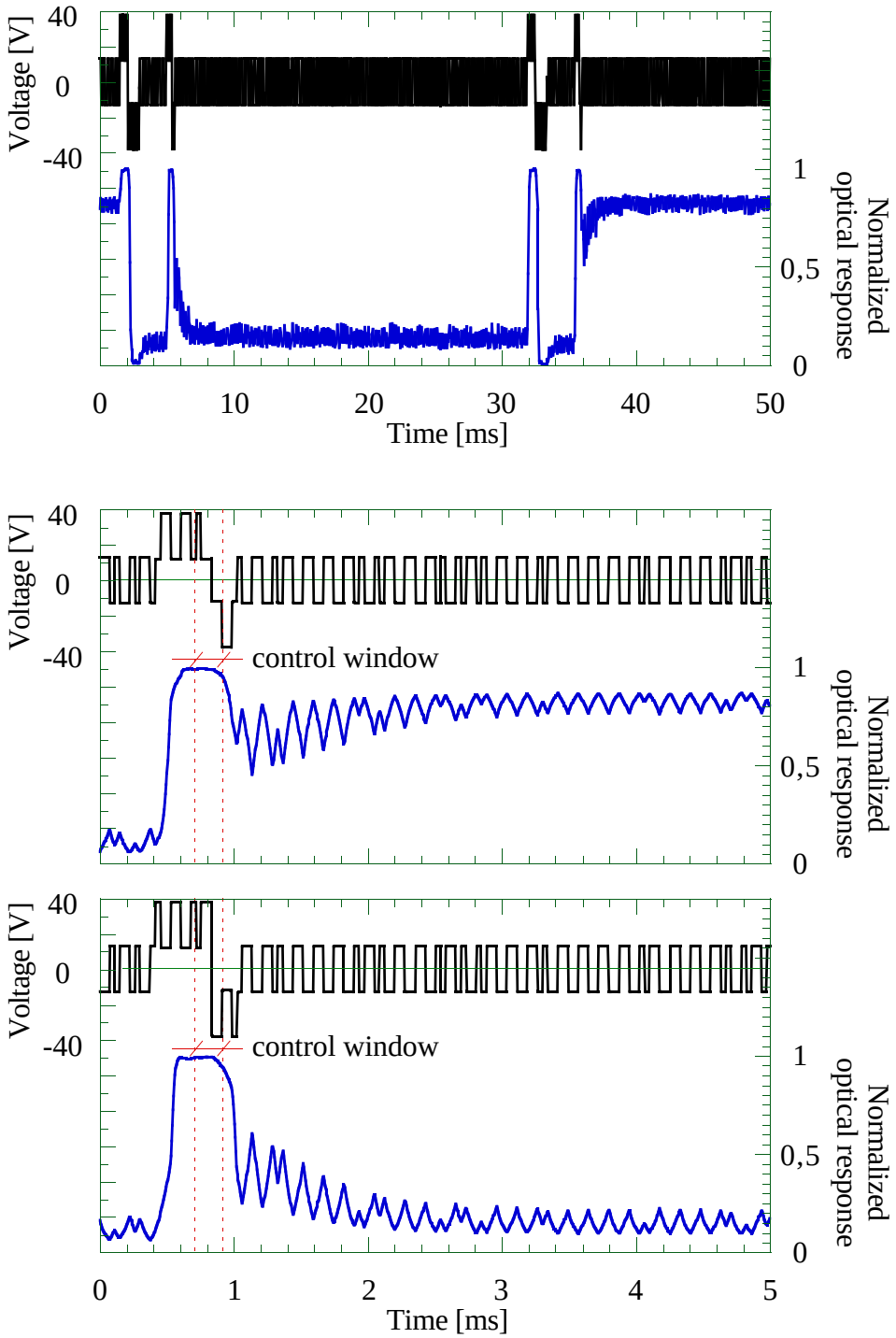

Figure 6. Stopped writing mode - PS3 addressing scheme applied to an SCE8-cell at 28°C. Amplitudes of selection and data waveforms are 25V and 13V, respectively. Line addressing time is 152 μs. The top diagram presents the optical response of one pixel in a 200-row display. Below – its magnified parts showing the control window and the effective writing pulse in case of the up and down switching, respectively.

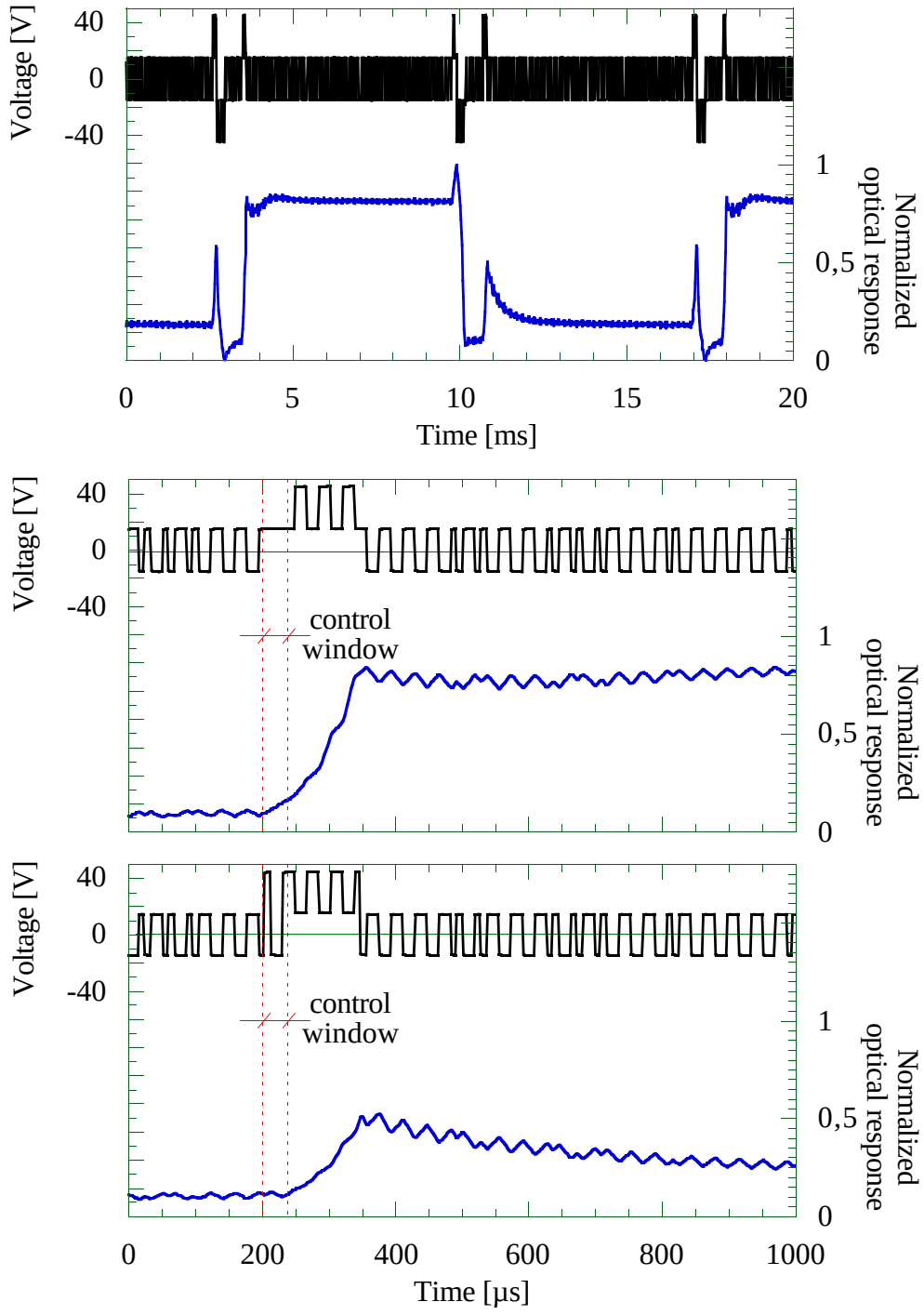

Figure 7. Hampered mode - the Split Writing Pulse (SW) addressing scheme applied to the SCE8-cell at 25°C. Amplitude of the selection waveform is 30V and data – 15V. Line addressing time is 36 µs. The top diagram presents the optical response of one pixel in a 200-row display. Below – its magnified parts showing the control window and the effective writing pulse in case of the up and down switching, respectively.

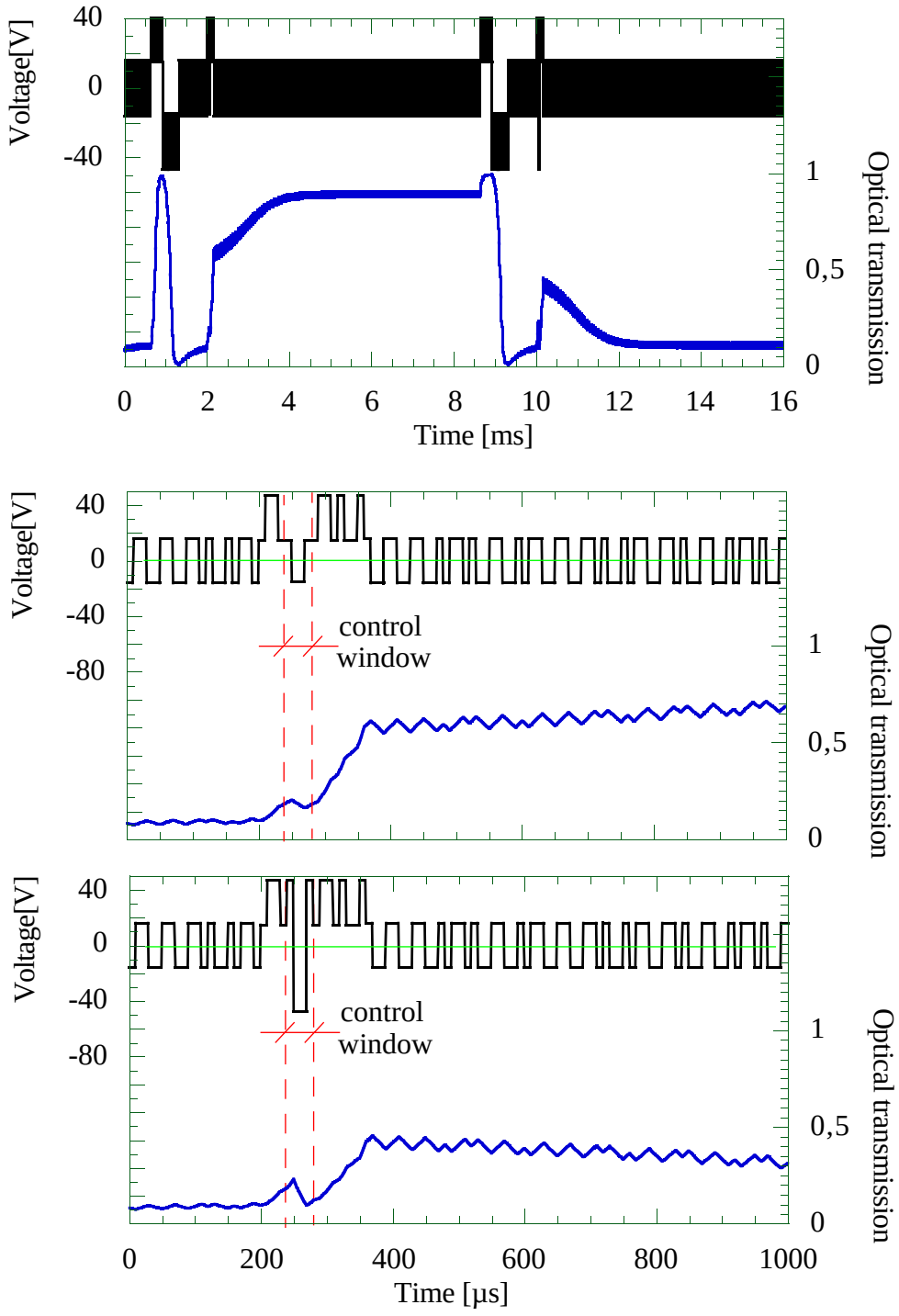

Figure 8. Split writing with “Callback” pulse, hampered mode - simulation of the “Rome” (ROM) addressing scheme using parameters corresponding to the SCE8-cell at 30°C. Amplitudes of the selection and data waveforms are 31V and 16V, respectively. Line addressing time is 40 µs. The top diagram presents simulated optical response of one pixel in a 400-row display. Below – its magnified parts showing the control window and the effective writing pulse in case of the up and down switching, respectively.

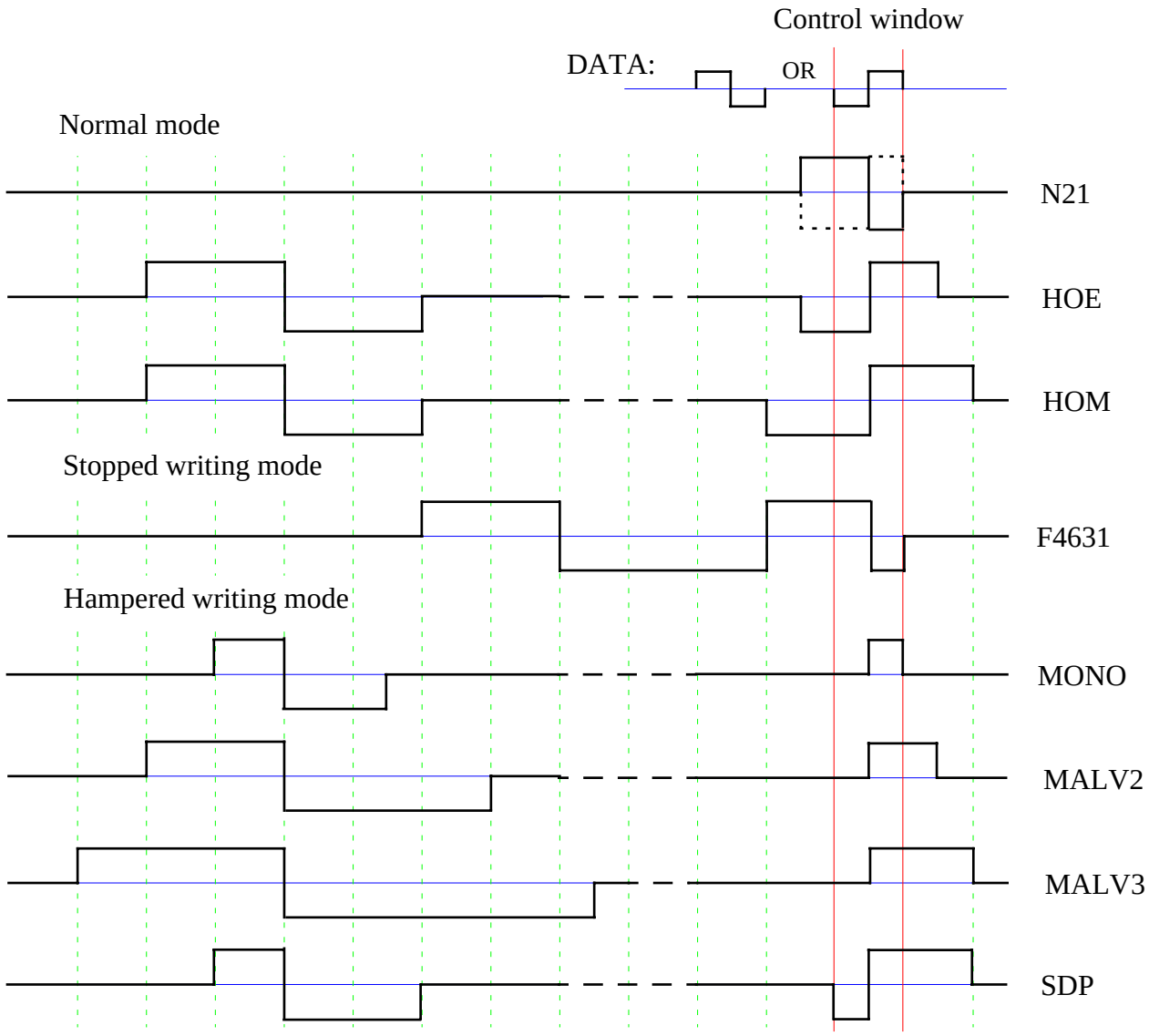

Figure 9. Sketch of the selection waveforms used in the addressing schemes having bipolar pulses in data waveforms.

both cases (up and down switching). The switching continues during the second writing pulse, but if it was counteracted in its initial stage, it cannot reach a level from which it could be completed by the action of crosstalk pulses and is instead forced back to the original state.

At 25°C and with the amplitudes of 30 V and 15 V for the selection and data, respectively, the line addressing time obtained by this scheme was 36 µs. The size of the writing pulse and the placement of the control window (i.e. how large part of the first writing pulse it overlaps) may be adjusted for other liquid crystal materials and cell parameters.

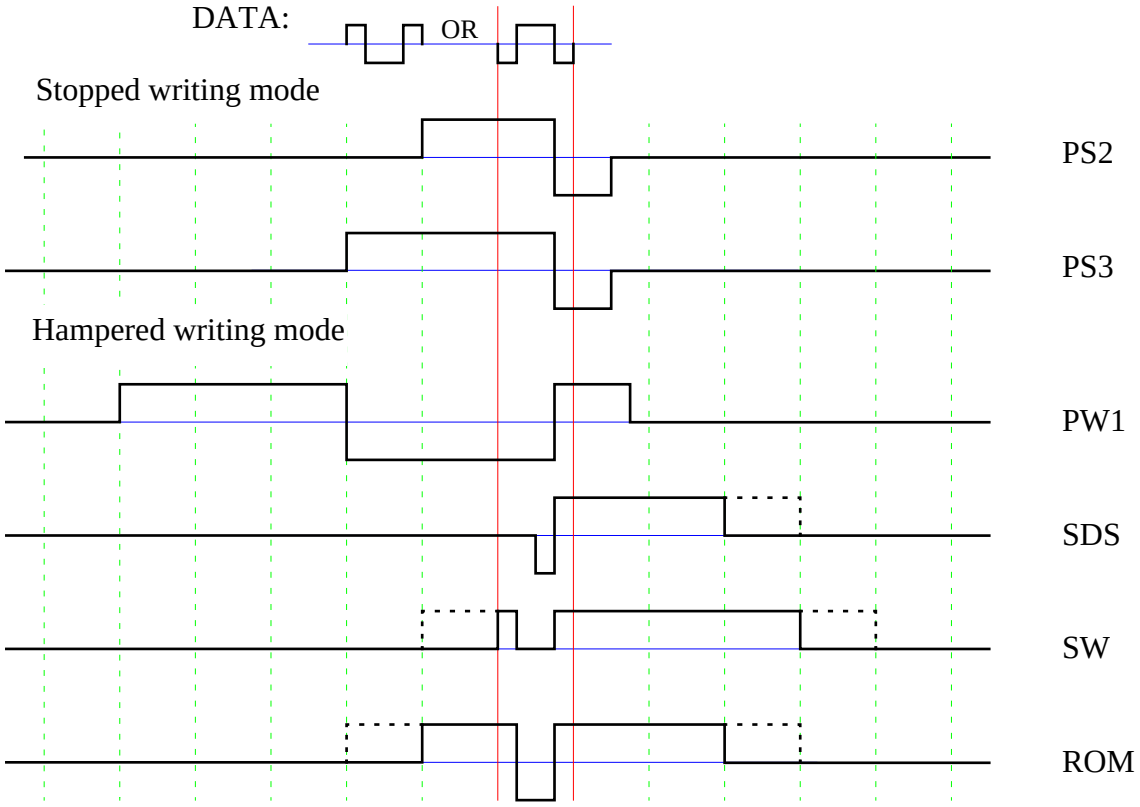

Figure 10. Sketch of the selection waveforms used in the addressing schemes having ‘crosstalk compensated’ pulses in data waveforms. Dotted lines in SDP, SW and ROM schemes mean that the corresponding pulse length can be adjusted to suit the cell properties. The dc-compensate/erase sequences are not shown.

HAMPERED MODE – CALLBACK PULSE

The recently published family of “Rome” addressing schemes[17] utilizes a “Callback Pulse” placed after the beginning of the switching slope. The switching is initiated equally for both possible data waveforms and then interrupted by a sequence containing a pulse of opposite polarity. The switching trace falls towards the initial level by an amount depending on the size of the “callback” pulse, which is defined by the data within the control window. Afterwards the switching is resumed, but due to significant difference in the new “initial” state it can either be completed or falls back to the erased state. As opposed to the SW scheme, this mode utilizes an additional effect of the reversed ferroelectric torque to make the slope interruption more effective.

Figure 8 presents the simulated optical response of a “Rome” scheme[17] using parameters corresponding to the SCE8-cell. The size of the first and second part of the writing pulse has been tuned for the best performance in the simulation.

CONCLUSIONS

It may be convenient to classify the addressing modes in several categories:

- *Normal* or *Writing After Saturation* mode, where the **area** of the writing pulse controls the final state of the addressed pixel,
- *Hampered Writing* mode, where switching is controlled by the dielectric effects in its **initial** stage,
- *Stopped Writing* mode, where switching is controlled by the dielectric effects in its **final** stage.

Figures 9 and 10 outline a choice of addressing schemes. Schemes like Seiko,[4] GEC,[5] N21,[7] HOE,[21] HOM[24] (normal mode), F4631[19] (stopped mode), JOERS/Alvey,[12] Monopolar,[22] Malvern-2, Malvern-3[23] and SDP[24] (hampered mode) use the conventional data sequence consisting of a pair of pulses of opposite polarity. Improved, crosstalk compensated data sequence is instead used in PS2 and PS3[15] (normal mode), PW1,[14] SDS,[24] SW and ROM[17] (hampered mode). The dc-compensate-erase sequences preceding in time the selection periods are omitted in Figure 10.

Both hampered and stopped writing modes are significantly faster then normal modes. They also generally produce better contrast due to larger stabilizing effects stemming from the dielectric torque. Experience shows that the hampered writing modes allow wider regions of operation, and the stopped writing modes can be used with liquid crystals having higher spontaneous polarization.

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