TABLE OF CONTENTS

ABSTRACT

The present thesis deals with the electronic addressing of Surface-Stabilized Ferroelectric Liquid Crystal (SSFLC) displays. Basically, this means to investigate how a certain information can be produced serially in the shape of long square pulse waveforms and transferred to a high resolution SSFLC matrix, via the specific linear electro-optic response exhibited by this material, to form a desired image on the screen at any time. To accomplish this, the thesis also includes the actual construction of the necessary hardware and software.

The work combines various aspects and approaches. Since the SSFLC does not react on the rms values of the pulse, the starting point was to correctly analyze how to use the polar ferroelectric interaction, with its unconventional threshold characteristics and memorized states, in order to write a dynamic picture in black and white, corresponding to the digital nature of the optical states. After demonstrating a virtually unlimited multiplexability due to the bistability of the SSFLC, the conflicting aspect of producing grey shades was also considered. In the early addressing schemes consideration was mainly given to the ferroelectric interaction, which is permissible as long as the applied voltages are low. The dielectric interaction, which is quadratic in the field, was mainly seen as a disturbance. Gradually, however, with the general recognition of the importance of the chevron local layer structure as well as the high values of the dielectric biaxiality, the dielectric interaction has been included in the analysis, resulting in a variety of possible new addressing schemes characterized by a much higher writing speed. In order to test these unorthodox or speculative schemes it was necessary to design and build a new type of electronic waveform generator. This work has been a major part of the thesis and resulted in an advanced electronic instrument distinctly different from the commercially available equipment and ideally suited for research on the addressing of all kinds of liquid crystal displays.

The dedicated waveform generator has the special ability to instantaneously vary different parameters in an applied waveform, without disconnecting the display, allowing immediate observation of the change in optical response. It has been used for comparing practically all known drive schemes with each other and with some very new ones, on three reference cells fabricated with different well-characterized FLC materials. The evaluation of their performance gives guidelines for future materials in combination with future drive schemes.

1 INTRODUCTION

The history of liquid crystals dates back to 1888 when the Austrian botanist Friedrich Reinitzer observed two melting points in cholesteryl benzoate.[1] Two years later Otto Lehman, Heinrich Hertz's successor on the physics chair in Karlsruhe, realized that a new state of aggregation was involved and called it "liquid crystal".

Practical applications started more than seventy years later, in the middle of the 1960's, initiated in research groups of some of the biggest american industrial corporations. James Fergason at Whestinghouse experimented with nematics and cholesterics and found that they were suitable as electric field and temperature indicators.[2] At the Second International Conference on Liquid Crystals in 1968, George Heilmeier of RCA presented a liquid crystal display based on dynamic scattering. The following years brought the Guest-Host and phase change displays.[3]

A major breakthrough occurred in 1971, when Wolfgang Helfrich and Martin Schadt at Hoffmann-LaRoche in Basel reported on the electro-optic properties of the Twisted Nematic (TN) structure,[4] which became the most successful technology for small liquid crystal displays. However, the contrast and viewing angle wane with increasing number of picture elements. In order to cope with this problem, the research on active matrix liquid crystal displays started to accelerate, resulting in quite impressive, but still small and expensive, TV and computer screens. They compete on the lap-top computer market with screens based on the Supertwisted Nematic (STN) structure[12] as first described by Terry Scheffer and Jürgen Nehring of Brown Boveri (Switzerland) in 1984.

Today's display devices utilizing nematic liquid crystals seem to be near the physical limits of performance and further efforts are mostly aimed at developing more sophisticated high-performance materials and a technology for making the necessary active substrates, in sufficiently large size, for screens of A4 and possibly larger.

A very different area of research was opened in 1974 by Robert Meyer.[6] He predicted that a chiral smectic C liquid crystal phase (C*) can exhibit ferroelectric behavior and went on, with his co-workers, to investigate the properties of this first polar liquid crystal. In 1980, Noel Clark and Sven Lagerwall described a structure in which this liquid crystal can be poled and, therefore, the ferroelectric character of the C* phase appears: the Surface-Stabilized Ferroelectric Liquid Crystal (SSFLC) structure.[7] As a result of their work it became clear that the bulk state of smectic C* is not truly ferroelectric (it is actually antiferroelectric), because its macroscopic polarization is zero and it cannot exist in different states with different polarization direction. However, when the helical symmetry, characterized by the bulk, is broken by surface action, macroscopic domains appear with a nonzero polarization which can point in two opposite directions. This is not only interesting from a pure physics point of view, but immediately leads to the potential of a new electro-optic effect characterized by bistability. The discovery of SSFLC initiated intense research, both basic and applied, in this field.

The construction of practical devices utilizing the SSFLC structure requires a suitable technique of controlling the electro-optic behavior of each display element - the addressing methods. These are on a much higher level of complexity than in the case of the nematic liquid crystal devices. The essential difference is that nematics respond to the root-mean-square (rms) value of an applied electric field, while ferroelectrics exhibit a polar response and bistability. The size and resolution of SSFLC displays are, in practice, limited only by the technology of producing a dense and low-impedance electrode pattern. This and the superior viewing angle gave rise to fantastic prospects of future applications. However, the switching speed, in spite of being several orders of magnitude faster than in nematics, is still one of the main obstacles on the way to large high-definition television screens. Another challenge is the generation of necessary grey shades from a structure that essentially produces either black or white optical states. Finally, both structural and dynamic properties of SSFLCs turned out to be extremely complex.

The rate at which a picture can be drawn on an SSFLC screen does not depend solely on the switching speed of the liquid crystal material. Significant improvements can be achieved by properly designing the electronic driving signals – the display addressing schemes. The *Chalmers* addressing scheme[Paper I], used to demonstrate for the first time a dynamic pattern on a SSFLC matrix display in 1987, required five times longer period to switch all pixels in a line than would be necessary for switching one display element in the direct way. This time interval was reduced in the recently developed *Split Writing* scheme[Paper X] to nearly one fourth of the cell's switching time.

The present thesis deals with electronic addressing of ferroelectric liquid crystal devices. The important physical properties and mechanisms are discussed. Design, real operation and computer simulation of addressing schemes are presented and a general classification of addressing methods is proposed. Finally, the construction of a specially designed Waveform Generator, dedicated to liquid crystal research and used throughout this work, is described.

2

FERROELECTRIC LIQUID CRYSTALS

2.1 Ferroelectricity in Liquid Crystals

The *nematic* is the least ordered liquid crystal phase. Here the rod shaped molecules tend to align in one direction. The average direction of molecular long axis is denoted the director **n** (see Figure 1). On lowering the temperature below a certain point a new ordering may begin to take place, leading to a one-dimensional periodicity along **n**. The molecules tend to assemble in layers and are no longer free to float around in three dimensions. The coupling between the layers is weak, so these can slide over one another quite easily. This phase, called *smectic A*, is the simplest periodic liquid crystal phase. At still lower temperature, the structure may reduce its symmetry as the molecules begin to tilt within each layer and the liquid crystal enters the *smectic C* phase.

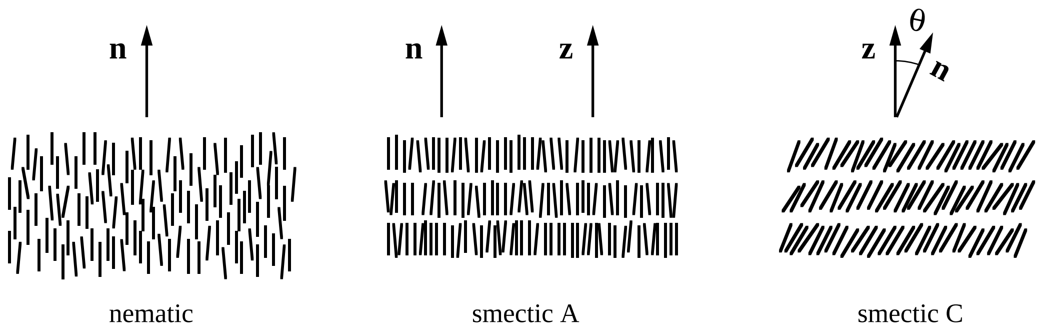


Figure 1. Molecular organization in the nematic, smectic A and C liquid crystal phases. The average direction of the molecular long axis is denoted by **n**; **z** is the layer normal and θ is the tilt angle.

If the molecules are chiral, then the nonuniform angular distribution of molecular orientation along their long axis, characteristic of a tilted smectic, produces an average net dipole moment of the layer and, thus, a local spontaneous macroscopic polarization (dipole moment per unit volume or charge per unit surface)

$$\mathbf{P}_S = P_0\, \mathbf{z} \times \mathbf{n} \qquad (1)$$

The director **n** and polarization $\mathbf{P}_S$ are locally coupled, but otherwise free to rotate, with the constraint that **n** preserves its angle relative to **z**. The molecules have therefore collectively a sort of conical freedom around the layer normal.

In the bulk, the spontaneous polarization $\mathbf{P}_S$ is only a local property, not a macroscopic or bulk property. The chirality constrains the director **n** to twist around the layer normal **z** on the surface of the cone with the apex angle 2θ, thus, forming a helix along **z**. The periodicity (pitch) of the helix is lying typically in the range of 100-5000 smectic layers. In such a configuration, the rigid coupling of $\mathbf{P}_S$ and **n** cancels the overall polarization, as can be seen in Figure 2.

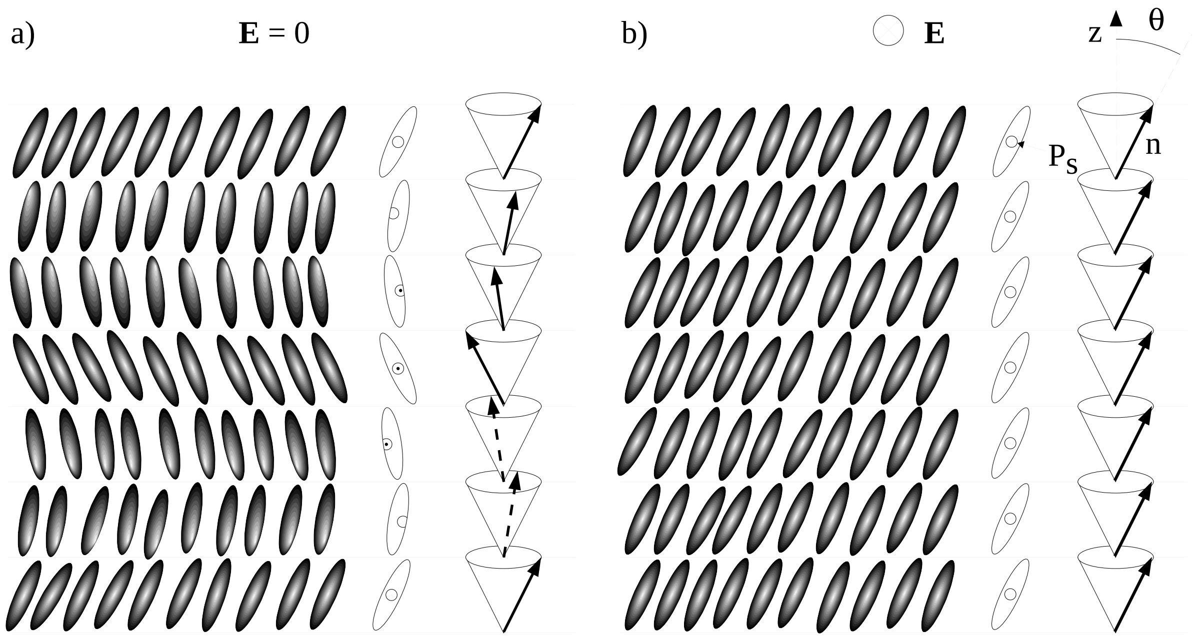


Figure 2. Helicoidal smectic C* structure. a) The director **n** is tilted by an angle θ with respect to the layer normal **z**. Each smectic layer possesses an electric dipole density (polarization) perpendicular to the director and parallel to the layer. The chirality generates a helicoidal structure and the director precesses from one layer to the other, which also turns the direction of the polarization $\mathbf{P}_S$. After the full turn (one helical pitch) the net polarization is cancelled. b) If the helix is unwound, for example by external electric field, the precession of **n** is suppressed resulting in an induced macroscopic polarization $\mathbf{P} = \mathbf{P}_S$.

2.2 The Surface-Stabilized FLC Structure

The SSFLC concept[7] exploits the geometry and surface interactions to unwind the helix. This requires a very thin gap in the cell, slightly smaller than the helical pitch, of the order of a micrometer or two.

Figure 3 shows a very much idealized SSFLC geometry. Here, the liquid crystal is sandwiched between two glass plates. The smectic layers are normal to the plates and the boundary conditions on the surface of the plates favor **n** lying in their plane. This preferred orientation and the liquid crystal's constraint of having **n** on the tilt cone, produces two possible positions of **n** at the intersections of the tilt cone with the surface of the glass plates. The spontaneous polarization $\mathbf{P}_S$, being normal to the surface, can then adopt only *up* or *down* orientation. This leads to the appearance of spontaneous domains of uniform polarization, which proves that this

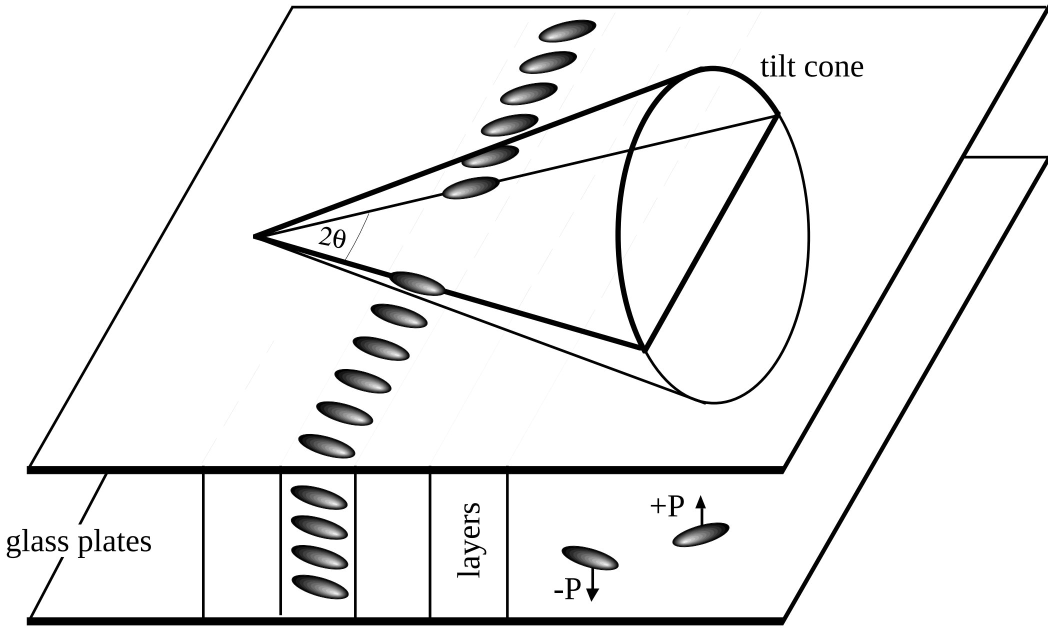


Figure 3. The basic geometry (*bookshelf geometry*) of a surface-stabilized ferroelectric liquid crystal cell structure. The two selected directions of the optic axis correspond to up and down polarization.

structure is ferroelectric. Ideally, the **n** positions should correspond to symmetrically equal energetic minima and, thus, be equally stable. By applying electric fields of different polarity, the orientation of the director **n** can be swapped between two states. This point will be discussed in Chapter *Bistable Switching* (page 15). When going from one state to the other, the threshold energy that has to be overcome, may be explained by the fact that the director has to go out of the surface of the plane or the surface of the cone, or both.

The cell structure is commonly called a *bookshelf geometry*, a designation pointing out that the layers are ordered in a general fashion, as books on a shelf. Typically, they are not strictly perpendicular to the surfaces, but more or less tilted (Figure 4a). The bookshelf geometry can still be used as a simple model, but the real picture is definitely more complicated. As was deduced from x-ray diffraction experiments[22] and texture studies, the layers are most often folded, forming an internal *chevron structure* (Figure 4b). The reason for layers to become inclined is that they become thinner upon cooling from orthogonal smectic A* phase to the C* phase, as the molecules tilt more and more in the layers.

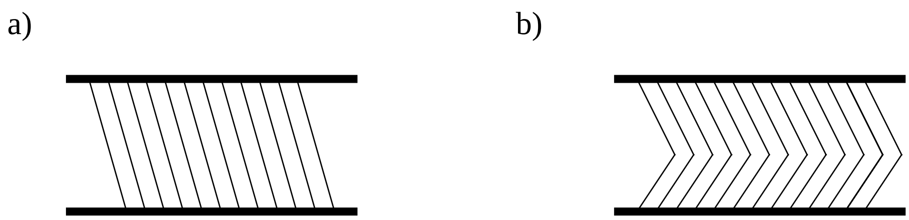


Figure 4. Schematic representation of a bookshelf structure with inclined layers (a) and a chevron structure (b). The chevron kink does not necessarily appear in the middle of the sample.

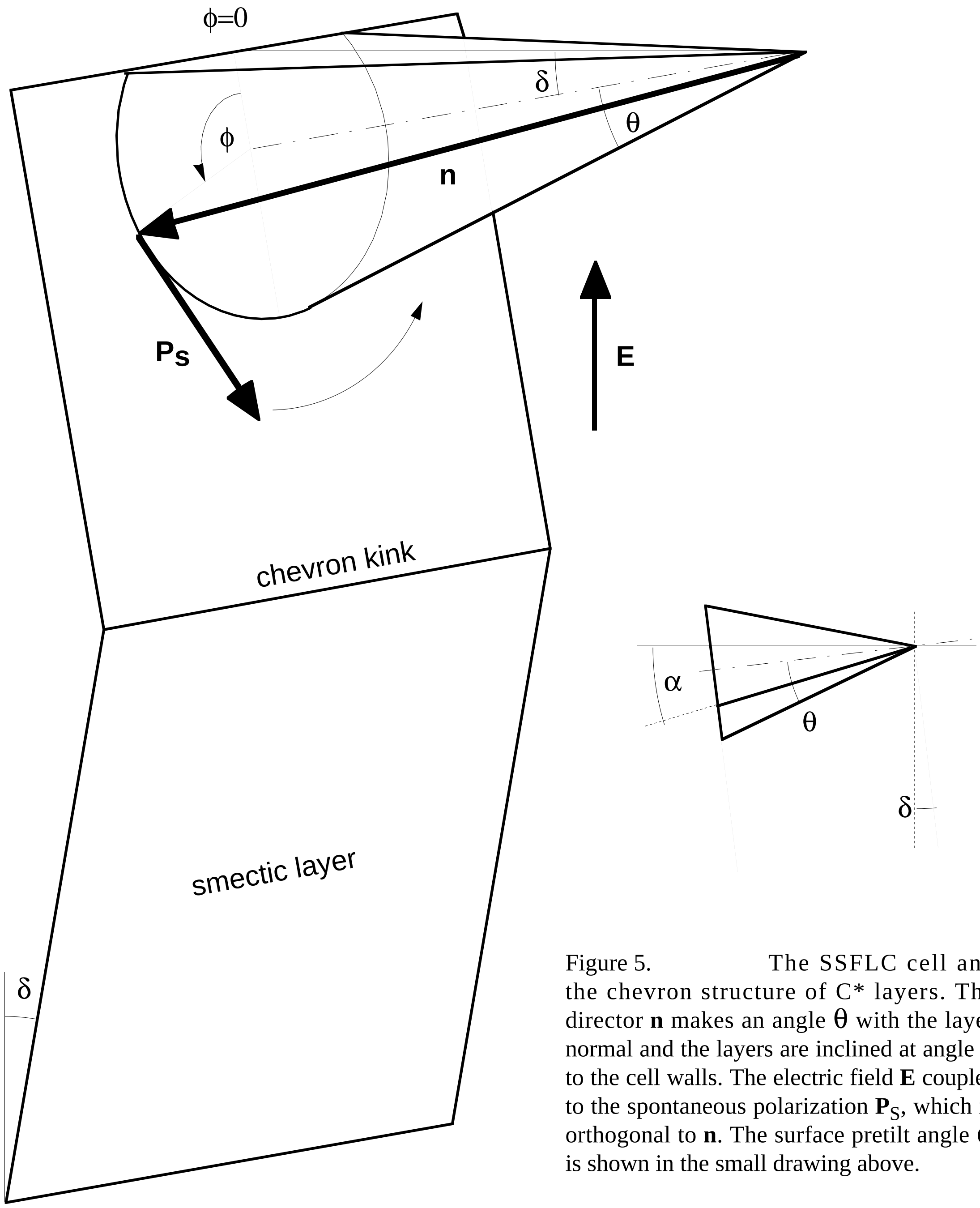


Figure 5. The SSFLC cell and the chevron structure of C* layers. The director **n** makes an angle θ with the layer normal and the layers are inclined at angle δ to the cell walls. The electric field **E** couples to the spontaneous polarization $\mathbf{P}_S$, which is orthogonal to **n**. The surface pretilt angle α is shown in the small drawing above.

A multitude of internal cell structures can, in fact, be realized depending on the layer inclination δ, surface pretilt α and smectic tilt angle θ. The basic chevron structures will be discussed in Chapter 3.3 *Molecular Orientation States* (page 11). In the case illustrated in Figure 5 the director **n** is in a memorized state ϕ. The polarization vector $\mathbf{P}_S$ makes an angle less than 90° to the surface. Its horizontal component provides initial torque when the electric field **E** is applied. It determines which way **n** has to turn around the cone. The direction is inverse in the upper and lower part of the chevron. Since the chevron interface (kink) is sharp on this scale, the molecules on the counter sides of the internal chevron surface block each other's way. This might increase the switching threshold, thus, assisting the bistability.

In an upright bookshelf geometry the desired molecular tilt angle θ is 22.5°. The rotation of **n** is then $2\theta = 45°$ and, consequently, the plane of polarization of the light passing through the device can be rotated by 90°. In the tilted layer or chevron structure the effective optic switching angle is reduced due to the inclination of the ferroelectric cone and, thus, a correspondingly larger molecular tilt angle is desired.

2.3 Biaxiality of the Dielectric Tensor

In uniaxial dielectrics, like liquid crystals in nematic or smectic A phase, the dielectric permittivity tensor is described by an axis parallel to the director **n** ($\varepsilon_{\|}$) and a degenerate axis lying in any direction in the plane perpendicular to **n** ($\varepsilon_{\perp}$), as shown in Figure 6. The dielectric anisotropy $\Delta\varepsilon$ is then defined as:

$$\Delta\varepsilon = \varepsilon_{\|} - \varepsilon_{\perp} \tag{2}$$

However, tilted smectics like C or C*, are biaxial dielectrics and the ε-tensor is described by three principal axes ε_1, ε_2 and ε_3. Choosing the z-axis along the molecular direction, the dielectric permittivity ε_{ij} can be written in the following way:

uniaxial biaxial

$$\varepsilon_{ij} = \begin{bmatrix} \varepsilon_{\perp} & 0 & 0 \\ 0 & \varepsilon_{\perp} & 0 \\ 0 & 0 & \varepsilon_{\|} \end{bmatrix} \quad \Rightarrow \quad \varepsilon_{ij} = \begin{bmatrix} \varepsilon_1 & 0 & 0 \\ 0 & \varepsilon_2 & 0 \\ 0 & 0 & \varepsilon_3 \end{bmatrix} \tag{3}$$

At the phase transition from uniaxial to biaxial (smectic A to C) the director **n** tilts by an angle θ. As can be seen in Figure 6, the parallel component $\varepsilon_{\|}$ for the A phase corresponds to

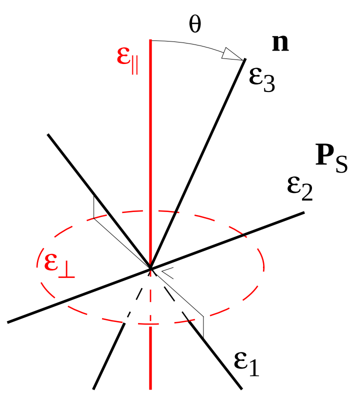


Figure 6. Orientation of the principal axes of permittivity in uniaxial and biaxial phases (Paper VI). In uniaxial systems, the ε tensor is described by one axis $\varepsilon_{\|}$ parallel to the director **n** and a degenerate axis $\varepsilon_{\perp}$ perpendicular to the director and lying in any direction in the plane perpendicular to **n**. In biaxial systems, the ε tensor is described by three principal axes ε_1, ε_2 and ε_3. At the transition from uniaxial to biaxial $\varepsilon_{\|} \Leftrightarrow \varepsilon_3$, $\varepsilon_{\perp}$ splits into ε_2 parallel to $\varepsilon_{\|} \times \varepsilon_3$, and ε_1 perpendicular to the plane containing ε_3 and ε_2.

ε_3 in the C phase. The perpendicular component $\varepsilon_{\perp}$ becomes non-degenerate and splits into ε_1 and ε_2. We can then choose ε_1 perpendicular to ε_3 in the direction of tilt θ, i.e. tilting out of the smectic layer plane by the same angle θ. It gives ε_2 along the direction of the C_2 symmetry axis characteristic of the C* phase. The C_2 axis is also along the spontaneous polarization.

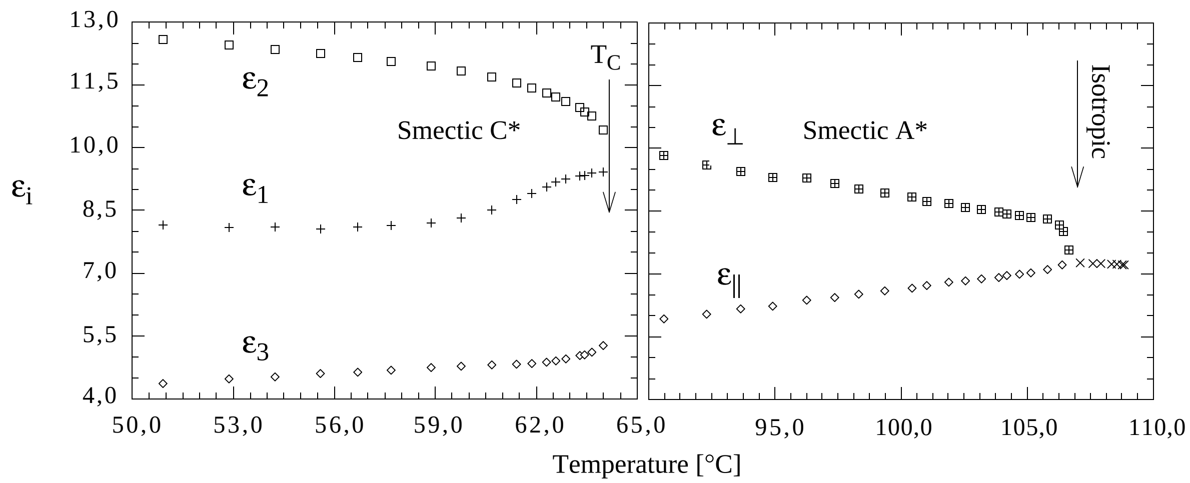


Figure 7. Temperature dependence of the principal components of the dielectric tensor in the isotropic, A* and C* liquid crystal phases. The component $\varepsilon_\perp$ splits into ε_2 and ε_1 at the phase transition from A* to C*. The investigated substance is a single compound obtained from Nippon Mining Co. Ltd., Japan, and the measurements were performed at 100 kHz. (From reference 90).

Figure 7 presents measurements[90] of the temperature dependence of the principal components of dielectric permittivity. The splitting of $\varepsilon_\perp$ when entering the C phase can be clearly seen.

In the tilted smectic the biaxiality $\partial\varepsilon$ can be defined as:[65]

$$\partial\varepsilon = \varepsilon_2 - \varepsilon_1 \qquad (4)$$

and the dielectric anisotropy as:

$$\Delta\varepsilon = \varepsilon_3 - \varepsilon_1 \qquad (5)$$

Figure 7 shows the common behavior in the C phase with $\partial\varepsilon > 0$ and $\Delta\varepsilon < 0$ at frequencies above the ε_3 relaxation. From the point of view of the electro-optic switching behavior of SSFLC devices it is important to know the values and sign of the dielectric torques originating from ε_1, ε_2 and ε_3. It also important to relate the behavior of theses torques to the shape (frequency, amplitude) of the applied electric field since the liquid crystal molecules tend to align the largest permittivity component along the field. A planar orientation would then be promoted by a large ε_2 component (or approximately the difference between ε_2 and ε_1, which is the dielectric biaxiality $\partial\varepsilon$). On the other hand, the ε_1 and ε_3 components try to rise the molecule up. This would be of importance mainly in the initial stage of the switching process.

The measurements show that the ε_3 component is strongly frequency dependent (see Paper VI, for example) and exhibits a relaxation at a relatively low frequency after which its value falls down. In the range of interest, ε_1 and ε_2 are essentially constant. The typical behavior is sketched in Figure 8.

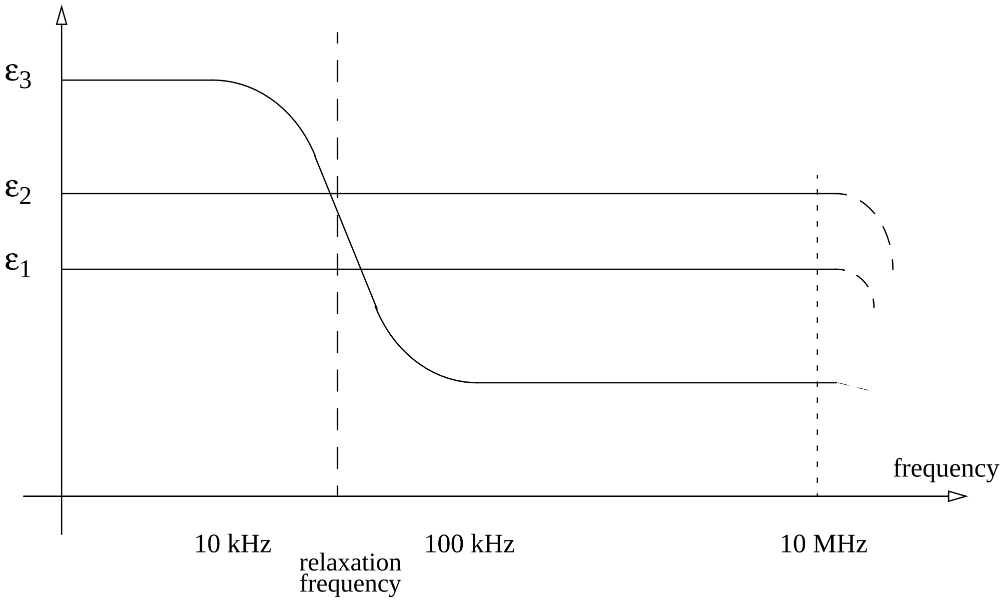


Figure 8. Idealized frequency dependence of the principal components of the dielectric permittivity tensor. The value of the relaxation frequency is a material property strongly dependent on viscosity and varies considerably in different compounds. This point has been discussed in Paper VI. As the present work deals with methods of controlling the electro-optic effects in SSFLC devices, the behavior of the dielectric permittivity tensor at very high frequencies is not relevant.

The role of the dielectric biaxiality in the switching behavior of SSFLC cells will be further discussed in the following chapters.

3 SSFLC Cell Construction

3.1 The Cell Structure

A typical cell is formed by sandwiching a thin layer of a liquid crystal material between two glass plates. The distance, and hence the cell thickness, is controlled by suitable spacers. SSFLC cells are much thinner (1-2 μm) than the nematic ones (6-10μm) which causes some technological problems. The inner surface of the glass plates has a quite complicated structure consisting of transparent electrodes (usually with metallization stripes to reduce the resistance), barrier layers and alignment layers. In the case of a color display this structure includes also a color filter mosaic and a planarization layer. Suitably adjusted polarizers are glued on outer surfaces of the glass plates.

3.2 Alignment Methods

The SSFLC structure involves two symmetrical director orientations, and thus, the methods of aligning the liquid crystal within the sample are not trivial. The first successful technique was shearing, described already in the original Clark-Lagerwall paper.[7] This method is not convenient to implement in industrial conditions. Many different techniques have been developed by different research groups. In the Chalmers laboratory we have tested spacer edge growth,[15] epitaxial growth with magnetic fields,[8] temperature gradient controlled methods[11] and other. We found the shearing technique still most suitable for preparation of small cells for liquid crystal material characterization like measurements of spontaneous polarization. Thicker cells intended for dielectric measurements are aligned by electric or magnetic field. For preparation of experimental displays we use either oblique evaporation or rubbed polymer alignment layers.[85] The latter technique is common nowadays since it is well adapted for industrial processing. Parallel (rather than antiparallel) rubbing is considered the most effective aligning method for practical fabrication of SSFLC displays.

3.3 Molecular Orientation States

The molecular orientation in an SSFLC cell determines on its electro-optic characteristics. There are two basic ways of forming a chevron structure as outlined in Figure 9. They are classified as C1 and C2, respectively.[57,71,79] From simple geometrical considerations one can draw conditions of existence for these orientations with respect to pretilt angle α (see

Figure 5). C1 is allowed for $\theta < \alpha < \theta + \delta$ and C2 if $\alpha < \theta - \delta$ (where θ is the cone angle and δ is the layer tilt). The cone angle θ increases when lowering the temperature, starting from zero at the A to C transition. The C1 orientation can be formed directly after the phase transition and may convert to C2 when θ becomes large enough. Thus, high-pretilt alignment retards the formation of C2. If these two orientations coexist in a sample, one can clearly observe under the polarization microscope hairpin defects, formed when C1 and C2 chevron kinks point inwards, and lightning defects in the counter case.

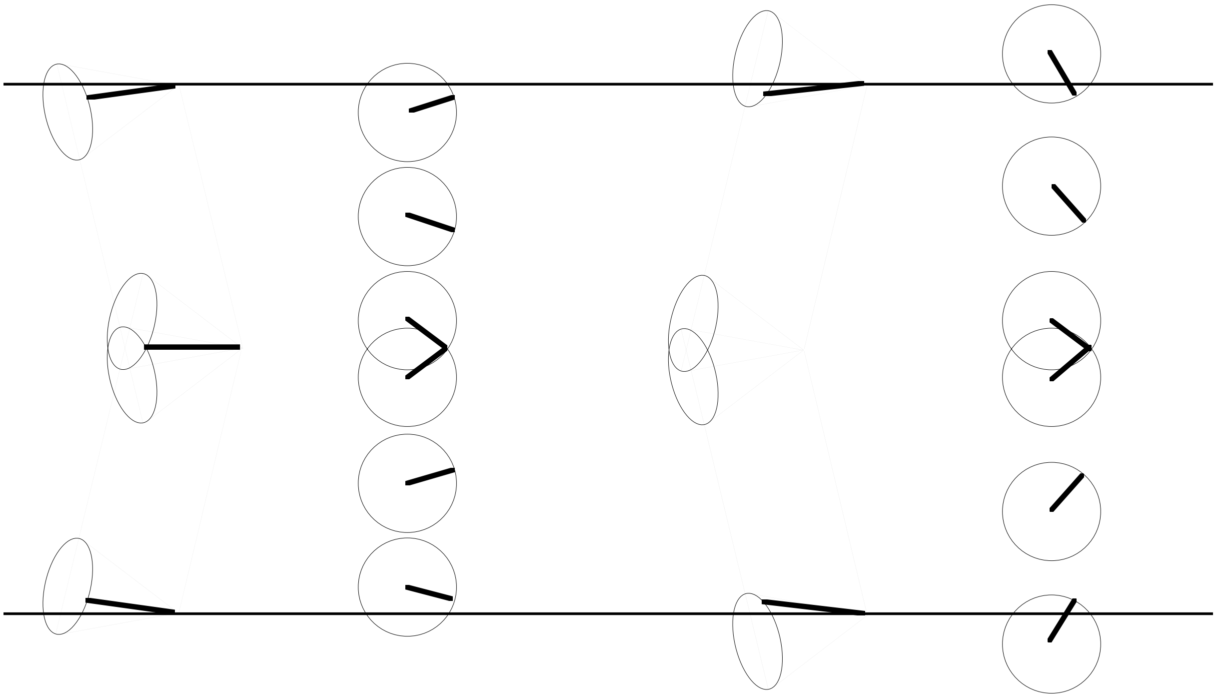


Figure 9. Uniform layer- and director structures formed in a surface-stabilized ferroelectric liquid crystal cell. The (“natural”) C1 structure is formed first upon cooling the sample from the A phase and may convert to C2 as the cone angle grows. C1 produces better optical extinction, but C2 is reportedly less sensitive to mechanical shock. To prevent zigzag defects, it is important to have only one kind of layer structure present in a practical SSFLC device.

Figure 9 shows a uniform (as opposed to twisted) configuration of the director **n**. It has been found[66] that twisted configurations (C1T and C2T) can also exist, in which the director at the bottom surface would be at eight o’clock instead of four o’clock in the C1 configuration of Figure 9. They do not show any light extinction position, which can be understood analyzing the director profiles sketched in Figure 10. The memory angle ϕ_0 of the uniform C1 state (C1U) is larger than that of the C2U, and thus C1 gives better optical contrast. In the C2 structure, on the other hand, as the pretilt angle increases, the difference between uniform and twisted orientations tends to decrease. Finally only one C2 state exists and exhibits extinction positions.

From the point of view of practical display devices it is important to have only one kind of uniform molecular orientation throughout the cell. The C1 has been chosen by Canon Inc.[88] and Matsushita,[62] and the C2 by Sharp Corp.[66]

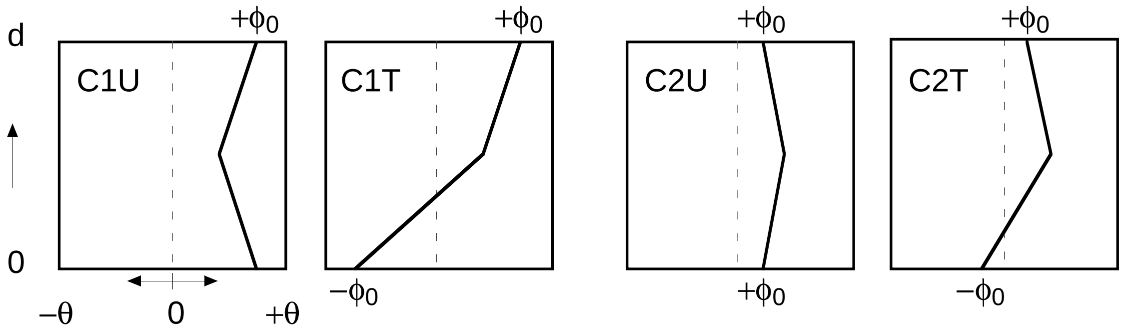


Figure 10. Director profiles for four molecular orientation states in a chevron-SSFLC cell. U denotes the uniform alignment and T the twisted one. (From reference 66.)

3.4 The Black Mask

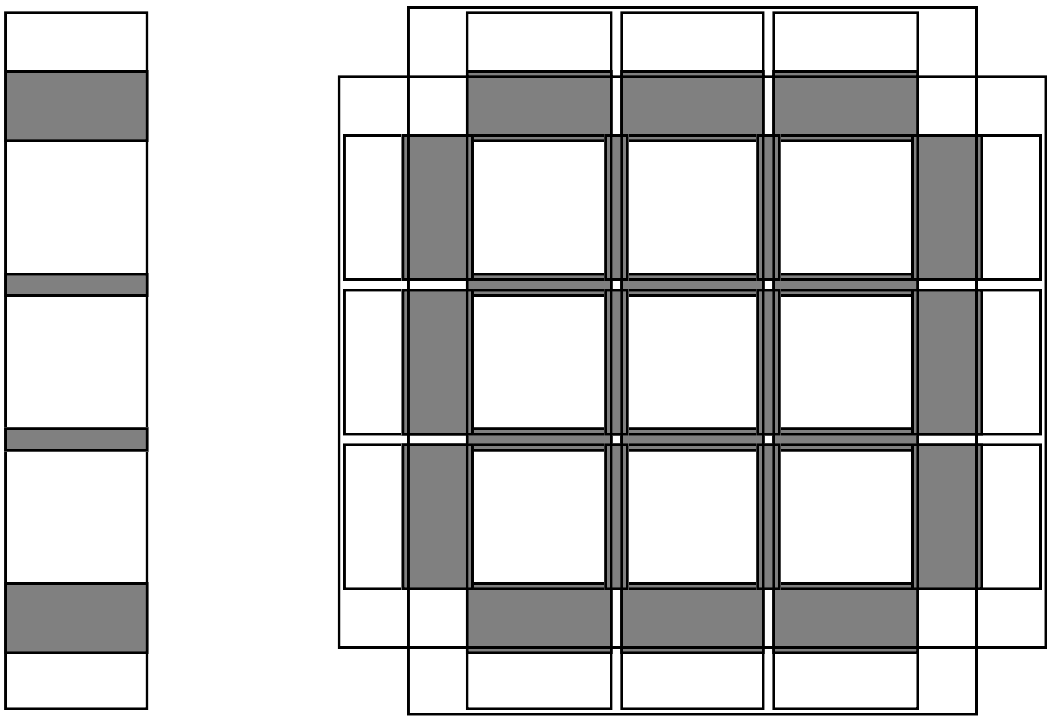
The achievable contrast of any display, liquid crystal as well as a standard cathode ray tube (CRT), is limited by the “leakage” of light in the black state.

In electrically addressed liquid crystal displays there is always a space between the electrodes, since they must be galvanically separated from each other. The light transmittance through such a gap is hard to predict, because the molecules within the gap are constantly influenced by the electric field applied to neighboring pixels. This field is normally too weak to switch the gap area uniformly into either state. Thus, it has a fluctuating greyish appearance.

The use of a light shield over the gap area is quite a straightforward way to deal with this problem. A so called *black mask* may be obtained, for example, by evaporation of a thin (in order not to disturb the alignment) chrome layer. Since chrome is conductive, it cannot be evaporated straight between the electrodes. A simple way to overcome this problem is to place the light shield across the counter electrode instead. This can be done by first evaporating the chrome stripes across the substrate (perpendicular to the planned direction of the electrodes) and then form the electrodes by etching away certain parts of both the ITO and chrome (Figure 11a). When the top and bottom substrates are assembled, the metal stripes cover most of the gap area leaving only small open spaces at the pixel corners (Figure 11b).

As the resolution of a matrix increases, the technological difficulties become more pronounced. The size of the gap becomes comparable with the pixel size. Since the black mask must be somewhat broader than the gap, due to necessary fitting margins, the active area of the display is reduced.

These problems could be avoided if the gap area was reliably held in the black state. The bistability of the FLC invites to such a solution. Wakita *et al* [62] showed that a cell with a very narrow space between electrode lines (3 µm) can be entirely switched black (inclusive gap areas) by repetitive application of bipolar pulses a few times wider than the cell’s switching time. After such an initial procedure, the normal scanning could be performed. The electric field within the space between electrodes, caused by multiplexing, is then considerably lower



a) b)

Figure 11. An example of a black mask: a) one electrode with the light shield pattern; b) assembled 3 by 3 matrix.

and if the bistability is sufficiently strong, the *field-induced black mask* formed in this way does not fade out.

This idea has recently been studied by van Haaren *et al.*[91] They reported that the liquid crystal in the gap area spontaneously aligns with polarization pointing toward the ITO-covered electrode. Consequently one type of gaps, for instance horizontal, tend to be black, whereas the other prefer to be in the bright memory state. One can, thus, take advantage from differences in voltage sequences applied to horizontal and to vertical electrodes and build a gap control sequence into an addressing scheme (these voltage sequences, i.e. the addressing schemes, are presented in Chapter *Multiplexing of FLC Displays* (page 27) and further discussed in the succeeding chapters).

4 Bistable Switching

4.1 Polar Switching

The Surface–Stabilized Ferroelectric Liquid Crystal (SSFLC) structure can be switched between two stable states by application of a voltage pulse of adequate size and polarity. In contrast to the case of nematic liquid crystals, the threshold is here defined by the pulse area, rather than the amplitude alone, and the polarity of the pulse dictates the switching direction. As can be seen in Figure 12, the liquid crystal cell reaches the maximum optical extinction during the switching pulse. When the field is removed, it relaxes to one of the stable states imposed mainly by the action of aligning layers.

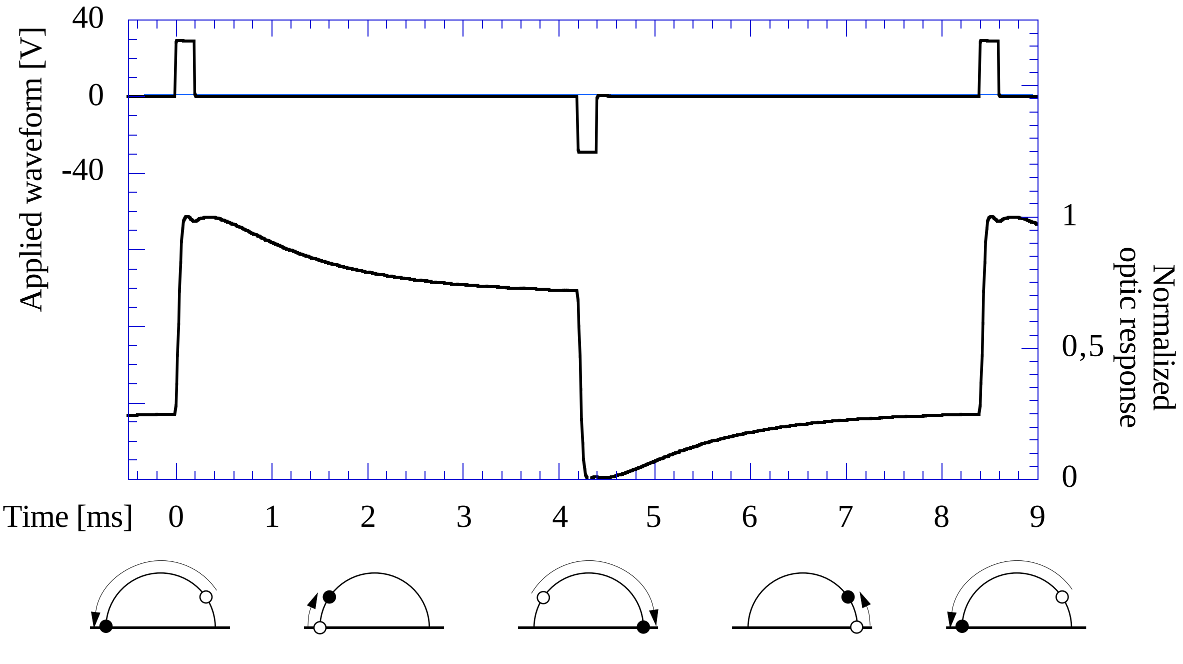


Figure 12. Polar switching of the SSFLC structure. The diagram presents the electro-optic response (lower curve) of an SSFLC-cell, filled with Merck SCE8 ferroelectric liquid crystal, to switching pulses (upper curve) of amplitude ±30 V and 200 μs long. Between the switching pulses the cell is short-circuited and relaxes to a field-free stable state. The liquid crystal director motion around the ferroelectric cone is schematically shown below. Parameters of all test cells used in the present work are given in Chapter *Experimental Cells and Setup* (page 93).

The positions of principal axes of dielectric permittivity related to the director orientations with and without electric field are presented in Figure 13. Applying an electric field induces a reorientation of the director towards the state where the P_S vector (and the ε_2 component of the dielectric tensor) coincides with the field direction. When the field is switched off,

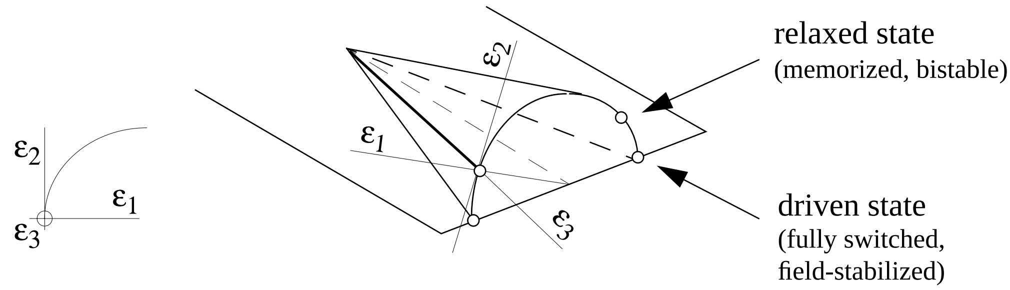


Figure 13. Director orientation in driven and relaxed states.

the director reorients to the surface stabilized state and the optical contrast may be significantly reduced. It would be desirable to maintain the liquid crystal director (and thus the device contrast) in a fully switched position. Keeping a constant voltage across the cell would damage it, as it will be shown in Chapter 4.4 *Ionic Effects and Reverse Electric Field* (page 23). It would also make impossible the multiplexing of SSFLC displays, which is the main subject of this work.

We know that the molecule naturally tries to align the largest permittivity component along the field. If this largest component is ε_2 and the frequency of the electric field is so high that it does not couple with the spontaneous polarization, the molecule will be kept in (or return to) the fully switched state. Such approach is usually called the high frequency (hf) stabilization or, more properly, the ac contrast enhancement.[98] Figure 14 shows the contrast enhancement in the same liquid crystal cell as in Figure 12 obtained by application of a high frequency square wave between the switching pulses. Practical implementation of this effect will be discussed in Chapter *The Crosstalk Field* (page 45).

Experimentally,[55] it has been observed that the hf field induces an electro-optic effect also at the frequency for which $\Delta\varepsilon = 0$, a result which clearly demonstrates the role of the dielectric biaxiality in the hf stabilization. In order to enhance the extinction angle in this case, it is required that $\varepsilon_2 > \varepsilon_1$; i.e. $\partial\varepsilon > 0$. Thus, the hf field couples to $\partial\varepsilon$ such that ε_2 has its maximum contribution in the direction parallel to the field. At field frequencies for which $\Delta\varepsilon$ is negative, it is found[55] that the extinction angle is reduced. This result can not be understood if we assume upright book shelf geometry where positive $\partial\varepsilon$ and negative $\Delta\varepsilon$ should cooperate to increase the contrast of the device. However, in the presence of a chevron structure (or titled bookshelf geometry), which is often the case, a negative $\Delta\varepsilon$ diminishes the extinction angle. Therefore, it is preferable to choose a compound with optimized values of the dielectric anisotropies such that $\Delta\varepsilon$ is slightly negative and $\partial\varepsilon$ is positive and as large as possible. This is of course a non trivial task and demands a delicate chemical engineering work to optimize different physical parameters suitable for device applications.

Paper IV discusses the interaction between dielectric Γ^D and ferroelectric Γ^F torques and relates it to the switching speed and hf stabilization. The dielectric torque is proportional to the square of the applied field and tends to preserve either of the extreme cone positions of the director. This has to be overcome by the ferroelectric torque (linearly proportional to the field)

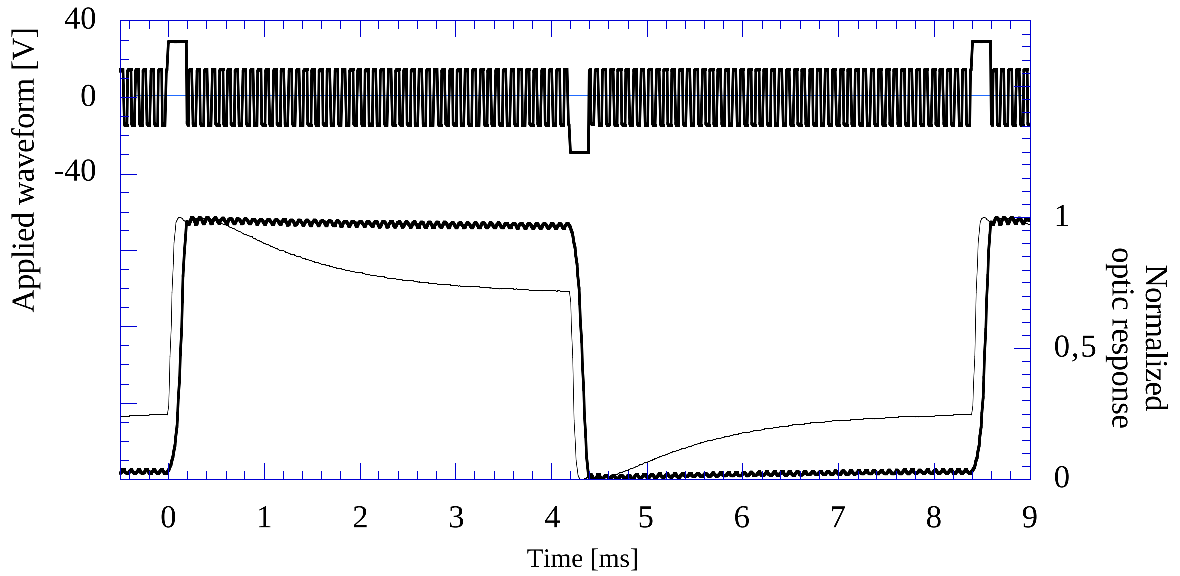


Figure 14. Dynamic stabilizing effect of a high frequency field (15 V, 12.5 kHz) as observed in the SCE8-cell (thicker line). The switching pulses have an amplitude of ±30 V and are 200 μs long. The thin line shows the optic response without hf field (cf. Figure 12).

in order to start the switching process. This competition of the torques causes the initial delay. In the second part of the switching both torques cooperate and the process is accelerated. Theoretically it was deduced in Paper IV that a minimum of the switching time occurs when $\Gamma^D = 0.5\,\Gamma^F$. At the time of that paper it was generally assumed that $\partial\varepsilon$ was small enough to be neglected. Although the experimental data now have to be slightly reinterpreted (Figures 7 and 8a-d in Paper IV present the behavior of dielectric and ferroelectric torques at low and high frequencies measured for different ferroelectric liquid crystal materials), the results are qualitatively correct. The minimum in the τ–V relation (Figure 6 of Paper IV) is exploited in some British addressing techniques which will be discussed Chapter 5.7 *The Minimum Voltage-Time Product* (page 38).

After the switching, in order to stabilize the extreme position, the dielectric torque should be much higher than the ferroelectric one. This can be achieved by proper choice of the amplitude and frequency of the applied electric field. The dielectric anisotropy changes at the ε_3 relaxation and is negative (or more negative than before) above the relaxation frequency (see Figure 8).

4.2 Simulation Model

In order to efficiently analyze electro-optic effects in the SSFLC cells, a suitable mathematical model is required. Several different approaches can be found in the literature,[23,24,52,92] each with its necessary simplifying assumptions. Also Paper IV includes a simple model that does not consider the elastic torque nor dielectric biaxiality. For the present work I have chosen a recent version elaborated by Maltese *et al*.[84] based on the assumption of a uniform director in uniformly inclined smectic layers. The real director structures are thus ignored to simplify the mathematical description of the physical behavior of an SSFLC cell. This model has proven capable of reproducing the main features of the electro-optic response for all known types of switching waveforms (the addressing schemes are discussed in detail in the following chapters). The final equations are simple enough to be integrated with the control software of the experimental instrument described in Chapter *The Waveform Generator* (page 77). With this combined software and hardware it is possible, for example, to manipulate the shape of the driving waveforms while simultaneously observing the simulated optic response on the computer screen and the real one on the oscilloscope.

The chevron layer structure has already been discussed in Chapter 2.2 *The Surface-Stabilized FLC Structure* (page 4). The simulation model we are using considers only the optical behavior in perpendicular view relative to the wall plates with all layers inclined at an angle δ to the viewing direction. This situation is assumed in the model drawn in Figure 15. The threshold effects produced by the interfaces are omitted.

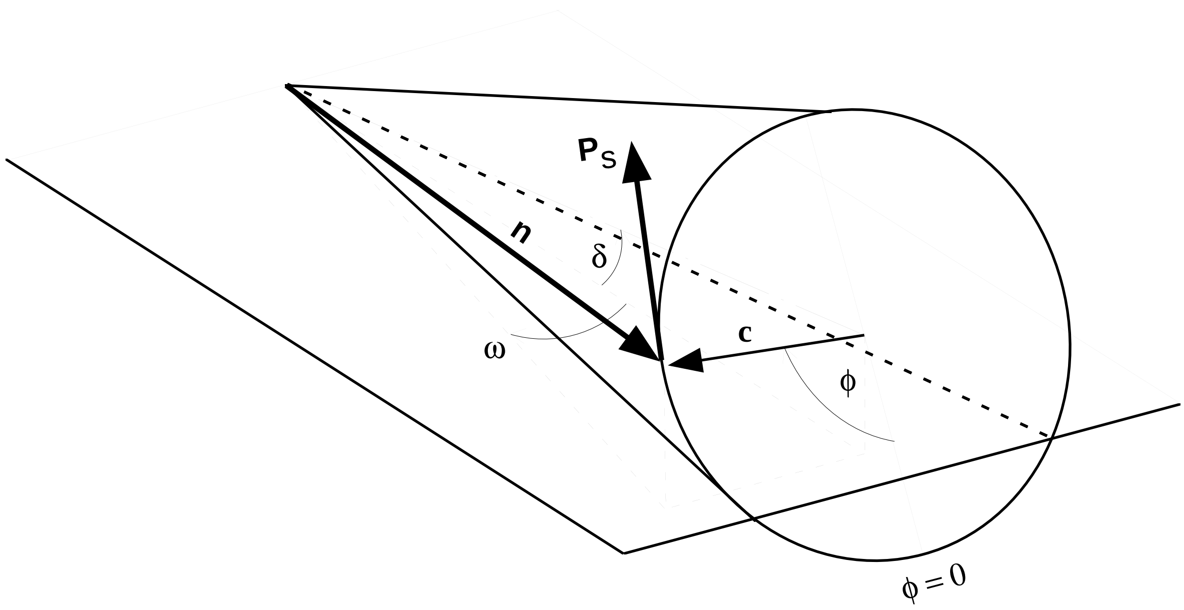


Figure 15. Simplified model of the C* cone at the surface boundary in a cell with smectic layers tilted at angle δ. Rotation of the director **n** around the cone is described by the azimuthal angle ϕ (ϕ=0 at the bottom of the cone). ω is the angle between the projection of the cone axis on the cell surface and the corresponding projection of the director.

If the director is uniform, then the light transmission L(t) through a cell between crossed polarizers, rotated by 22.5° (i.e. π/8) with respect to the cone axis, depends on the instant angle ϕ(t) of director around the cone and can be described by:[84]

$$L(t) = \frac{1 + \sin 4\omega(t)}{2} \sin^2 \frac{\pi \Delta n d}{\lambda} \qquad (6)$$

where the angle ω between the projection of the cone axis on the cell surface and the corresponding projection of the director **n** is related to θ, δ and ϕ(t) by

$$\tan\omega(t) = \frac{\sin\phi(t)\ \tan\theta}{\cos\delta - \sin\delta\ \tan\theta\ \cos\phi(t)} \tag{7}$$

The director position for $\phi = 0$ is on the bottom of the cone. If the thickness d of the cell is chosen to satisfy the halfwave condition ($\Delta n\ d = \lambda/2$) the second factor, modifying the transmission due to optical retardation, is equal to one and can, thus, be omitted:

$$L(t) = \frac{1 + \sin 4\omega(t)}{2} \tag{8}$$

There are four main torques acting on the FLC director during switching – a ferroelectric toque Γ^F responsible for the director movement around the cone, a dielectric torque Γ^D (actually composed of three torques) pushing the director to an extreme position, a viscous torque Γ^V counteracting the movement and an elastic torque Γ^K acting towards one of the relaxed states. In dynamic equilibrium, the balance of these torques,

$$\Gamma^F + \Gamma^D + \Gamma^K + \Gamma^V = 0 \tag{9}$$

can be used to derive the instant angle $\phi(t)$ required in equation (7).

The ferroelectric torque $\Gamma^F = |\mathbf{P}_S \times \mathbf{E}|$ is proportional to the applied voltage V and expressed by

$$\Gamma^F = \frac{VP_S}{d}\cos\delta\cos\phi \tag{10}$$

The dielectric torque has to include the biaxial properties of the dielectric tensor. This can be expressed using an effective dielectric parameter ε_Δ:

$$\varepsilon_\Delta = \partial\varepsilon - \Delta\varepsilon\sin^2\theta \tag{11}$$

In agreement with Jones *et al.*[56] the dielectric torque $\Gamma^D \sim V^2$ is then described by

$$\Gamma^D = \frac{\varepsilon_0\varepsilon_\Delta V^2}{2d^2}\cos^2\delta(\sin 2\phi - 2\cos\phi_v\sin\phi) \tag{12}$$

and equals zero for the limiting angular values $+\phi_V$ and $-\phi_V$ (ϕ at infinite voltage), which can be calculated from:

$$\cos\phi_v = -\frac{\Delta\varepsilon\sin 2\theta\tan\delta}{2\varepsilon_\Delta} \tag{13}$$

In a bookshelf geometry or if $\Delta\varepsilon = 0$, the angle $\phi_V = \pi/2$. In the typical case of chevron cells and negative dielectric anisotropy, ϕ_V is smaller than $\pi/2$.

The viscous torque Γ^V counteracts the change of ϕ and is expressed by

$$\Gamma^V = -\eta_c \frac{d\phi}{dt} \tag{14}$$

where η_c is the rotational viscosity depending on the tilt according to [26]

$$\eta_c = \eta \sin^2\theta \tag{15}$$

Finally, the elastic torque Γ^K is approximated by a function shown in Figure 16 and expressed by[52]

$$\Gamma^K = \frac{\eta_c}{t_R}(\sin 2\phi - 2\cos\phi_0 \sin\phi) \tag{16}$$

where t_R is an observable relaxation time. The elastic torque Γ^K equals zero in the two stable states $\pm\phi_0$ which, by definition, are the two relaxed, or memorized, states.

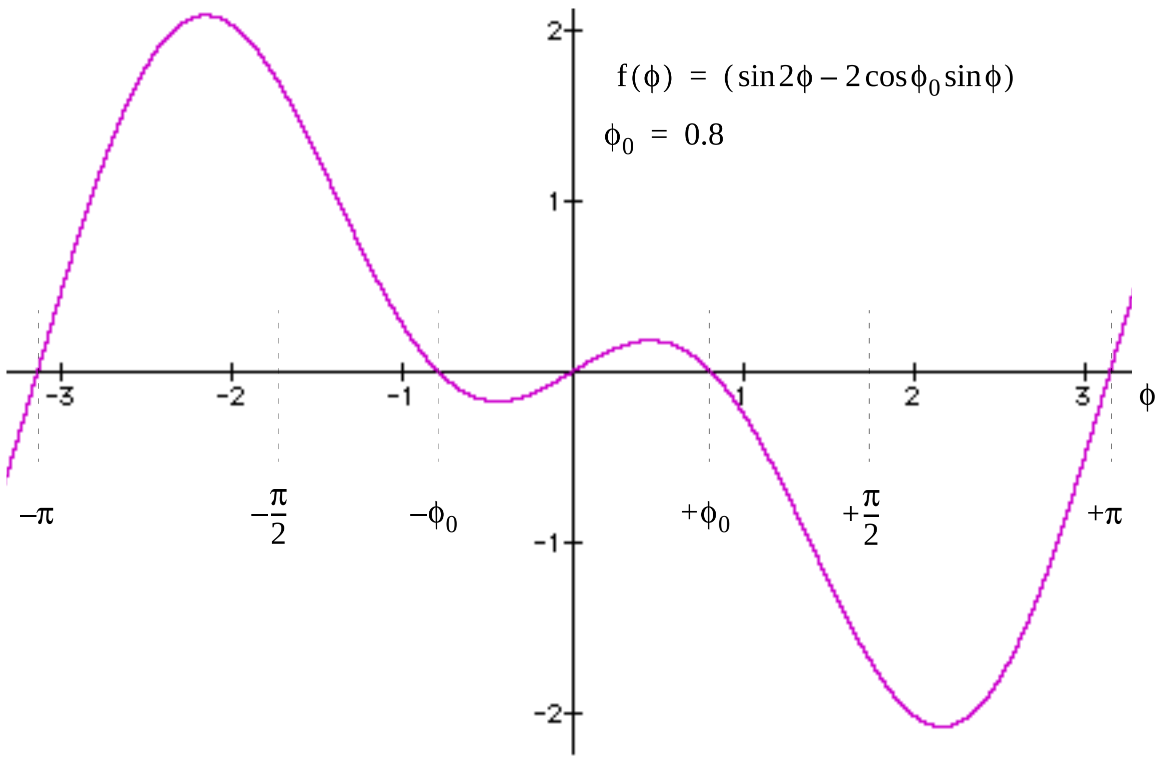


Figure 16. The shape of the function approximating the elastic torque $\Gamma^K \sim (\sin 2\phi - 2\cos\phi_0 \sin\phi)$ drawn for proportionality ratio equal to one and $\phi_0 = 0.8$.

Equation (9), describing the balance of torques acting on the liquid crystal director, then takes the following form:

$$\eta_c \frac{d\phi}{dt} = \frac{VP_S}{d}\cos\delta\cos\phi + \\ + \frac{\varepsilon_0\varepsilon_\Delta V^2}{2d^2}\cos^2\delta(\sin 2\phi - 2\cos\phi_v \sin\phi) + \\ + \frac{\eta_c}{t_R}(\sin 2\phi - 2\cos\phi_0 \sin\phi) \tag{17}$$

To simplify calculations, practical use of the simulation model and comparison of the results, reduced parameters ϕ_V, V_C, t_C and λ are introduced[84] replacing six physical quantities P_S, t_R, d, $\partial\varepsilon$, $\Delta\varepsilon$ and η_c in the equation (17). The limit value ϕ_V for ϕ at infinite voltage has already been described by equation (13). The positive characteristic voltage V_C defined as

$$V_C = \frac{d}{\cos\delta}\sqrt{\frac{2\eta_c}{\varepsilon_0\varepsilon_\Delta t_R}} \tag{18}$$

is related to the hf stabilization effect in the cell. A characteristic time t_C can be defined by

$$t_C = \frac{\eta_c\, d}{P_S V_C \cos\delta} \tag{19}$$

The switching time is inversely proportional to the switching voltage within a voltage linearity range from $V_C/\sqrt{\lambda}$ to $V_C\sqrt{\lambda}$ with

$$\sqrt{\lambda} = \frac{t_R}{2t_C} = P_S\sqrt{\frac{t_R}{2\varepsilon_0\varepsilon_\Delta\eta_C}} \tag{20}$$

such that:

$$V_C\sqrt{\lambda} = \frac{P_S d}{\varepsilon_0\varepsilon_\Delta\cos\delta} \tag{21}$$

The equation (17) takes now the form

$$\frac{d\phi}{dt} = \frac{V}{V_C t_C}\cos\phi + \\ + \frac{V^2}{V_C^2 t_C\sqrt{\lambda}}\sin\phi(\cos\phi - \cos\phi_V) + \\ + \frac{1}{t_C\sqrt{\lambda}}\sin\phi(\cos\phi - \cos\phi_0) \tag{22}$$

In the computer simulation the instant angle $\phi(t)$ is calculated by integrating the above equation using Runge-Kutta algorithm. Feeding the obtained value to equations (7) and (8) gives the instant light transmission through the cell.

The switching behavior of different liquid crystal cells and materials can be compared in a simpler way if the equation (22) is expressed in terms of dimensionless quantities. Introucing a reduced voltage $V' = V / V_C$ and a reduced time $t' = t / t_C$ we have

$$\frac{d\phi}{dt'} = V'\cos\phi\left[1 + (\sin\phi - \cos\phi_0\tan\phi)\frac{1}{V'\sqrt{\lambda}} + (\sin\phi - \cos\phi_V\tan\phi)\frac{V'}{\sqrt{\lambda}}\right] \qquad (23)$$

The effect of high frequency voltage on the rate of change of ϕ can be derived from the dielectric torque and estimated as[93]

$$\Gamma^{HF} = \frac{V'^2}{\sqrt{\lambda}}\sin\phi(\cos\phi - \cos\phi_V) \qquad (24)$$

which is graphically presented in Figure 17. The effect slows down switching in the initial phase, changes sign for ϕ crossing zero (bottom of the cone) and accelerates the switching in the final stage.

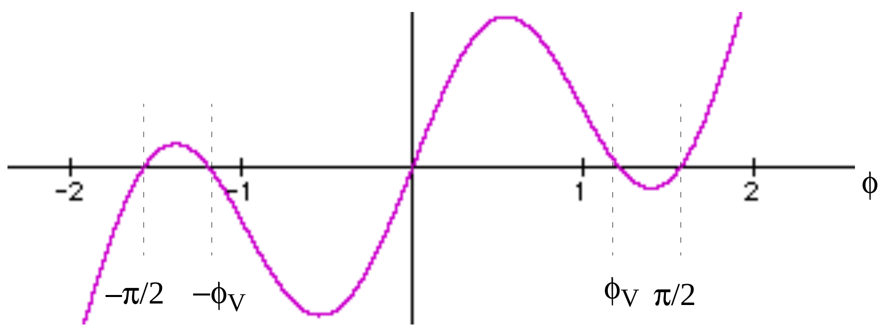


Figure 17. The shape of the function described by equation (24) (for ϕ_V=1,2 rad).

4.3 Bipolar vs. Monopolar Switching

Figure 18 presents the optic response of a cell filled with Merck SCE8 liquid crystal to the application of a bipolar and a monopolar switching pulse, respectively. It is clearly seen that switching from a relaxed state is significantly shorter than switching from the saturated state in the sense that it requires a shorter voltage pulse. A complete threshold characteristics for this cell will be presented later in Figure 32.

Examination of the switching trace during the first half of the bipolar pulse suggests that this part of the pulse could be shortened without changing its effect. It is understandable if one considers it as a monopolar pulse. Reducing the width of both pulses in the bipolar pair leads, however, to a situation where the second pulse becomes too short to have any lasting effect. Reducing only the first part, on the other hand, would lead to a dc bias.

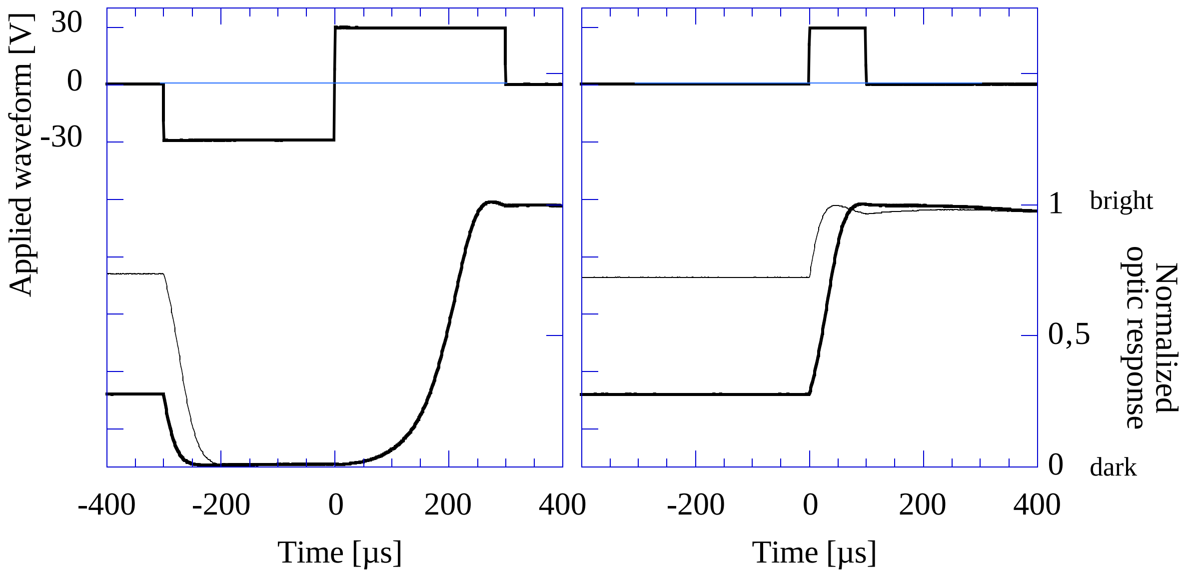


Figure 18. Bipolar versus monopolar switching (SCE8-cell at 24°C). Bipolar switching requires longer writing pulse (300 µs and 30 V) than the monopolar one (100 µs). Initial light transmission levels correspond to the relaxed dark and bright states, respectively. In the left figure the first pulse switches from relaxed bright or dark state to dark field-state (saturated state) and then the second pulse switches up to bright field-state. This state will only slowly relax back to the memorized (relaxed) state.

The difference in the electro-optic response to monopolar and to bipolar pulses has important implications on addressing schemes as discussed in Chapter 5.6 *Leading Pulse Latching* (page 38) and Chapter *Fast Addressing Modes* (page 51).

4.4 Ionic Effects and Reverse Electric Field

The SSFLC simulation model, presented earlier in this chapter, assumes homogeneous switching and neglects all phenomena which might disturb a homogeneous electric field inside the sample. This model, due to its simplicity, serves well for experiments with electronic addressing of SSFLC matrices (discussed in the following chapters) since the expected optic response can be calculated and presented nearly instantly on the computer screen. In reality however, there exist charge carriers in the FLC causing a varying bulk charge density. Concentration of ions in an SSFLCD cell is typically 10^{20} carriers/m^3 or more.[67] (For comparison, currently available very pure nematic mixtures exhibit ion concentration in the order of 10^{17} carriers/m^3.)

Ionic effects were studied by several authors.[25,30,38,45,58,71] Recently De Ley *et al.*,[92,94,58] presented a one-dimensional model which includes the effects of dielectric biaxiality, chevron structure, moving charge carriers and depolarizing fields caused by capacitance of the alignment surface precoated layers.

In SSFLC cells the worst case for the ion effect occurs when all ions have accumulated at top and bottom interfaces with the alignment layers. This situation can be obtained, for example, by applying a medium-amplitude dc-voltage during several milliseconds (e.g. 10 V during 15 ms). The surface charge density is σ and the geometry of the sample is shown in Figure 19. We also limit the calculations to one dimension along the x-axis.

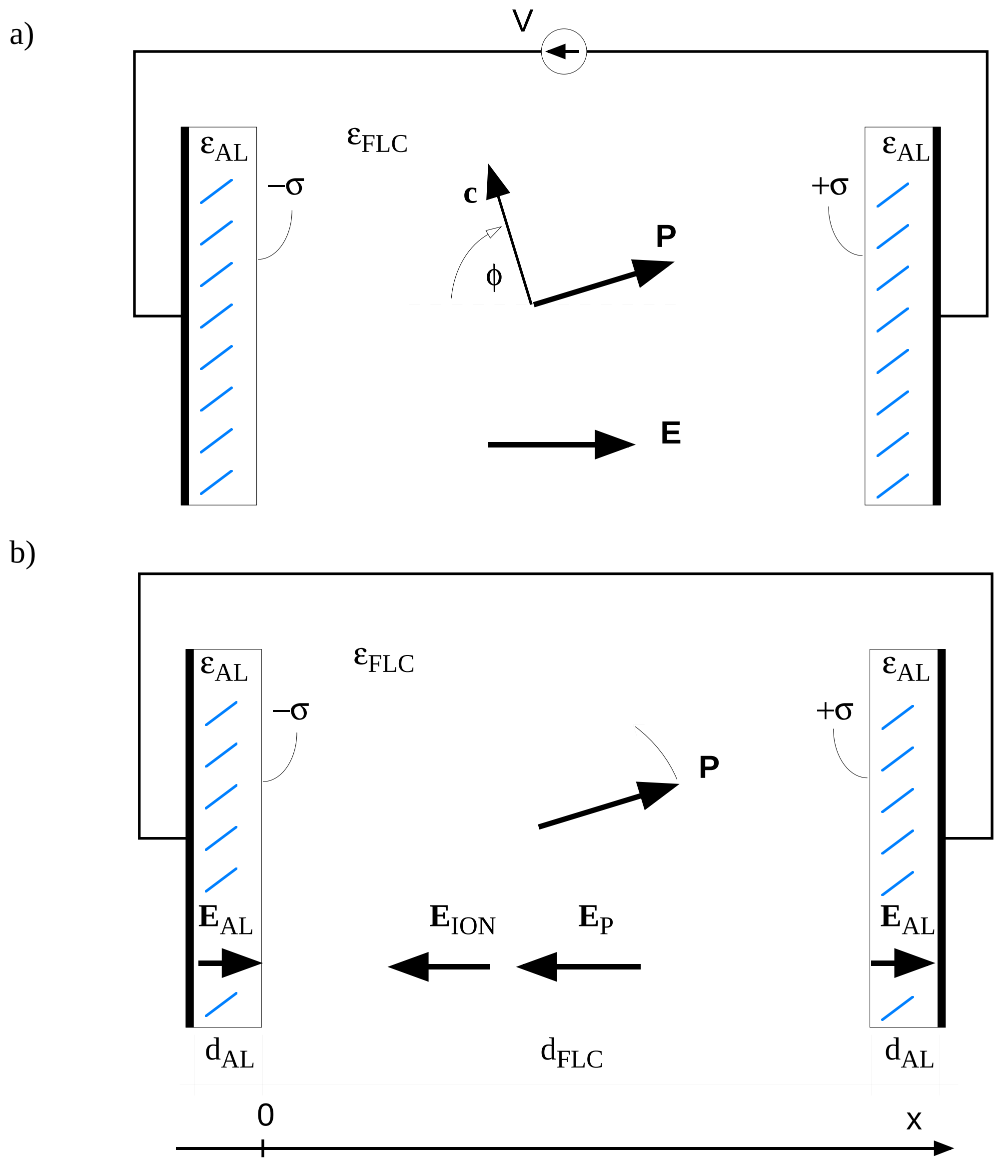


Figure 19. Electric field in an SSFLC cell a) during applied external voltage V and b) after short-circuiting. Reverse switching can occur due to the field induced by the spontaneous polarization and due to the ionic charge separation.

When all charges have separated, there will be no free charges left in the volume. The dielectric field $\vec{D}_{FLC}$ is then, according to Gauss law, homogeneous in the FLC. It is homogeneous also in the alignment layers, under assumption that there are no charges inside them, but only at the interfaces.

In a voltage-addressed liquid crystal cell, which is the kind of cells studied in this work, the voltage V between the two electrical contacts of the cell equals the sum of the voltage drops in the FLC and in both aligning layers:[92]

$$V(t) = \frac{D_{FLC}(t)d_{FLC}}{\varepsilon_{FLC}\varepsilon_0} - \int_0^{d_{FLC}} \frac{P_s \sin\phi(x,t)\cos\delta}{\varepsilon_{FLC}\varepsilon_0} dx + \frac{2d_{AL}(D_{FLC}(t)+\sigma)}{\varepsilon_{AL}\varepsilon_0} \qquad (25)$$

In a chevron structure ϕ must be a function of x. It is also generally, like the fields, the function of time.

In the analysis of De Ley *et al.* the expression (25) leads to a negative internal electric field E_{FLC} at the moment the external applied voltage is removed.

$$E_{FLC}\Big|_{V=0} = -\frac{1}{\varepsilon_{FLC}\varepsilon_0}\left[(1-\alpha)\sigma + P_s \sin\phi\cos\delta - \frac{\alpha P_s \cos\delta}{d_{FLC}}\int_0^{d_{FLC}} \sin\phi \, dx\right] \qquad (26)$$

where α

$$\alpha = \frac{C_{FLC}^{-1}}{C_{AL}^{-1} + C_{FLC}^{-1}} = \frac{\varepsilon_{AL} d_{FLC}}{\varepsilon_{AL} d_{FLC} + 2\varepsilon_{FLC} d_{AL}} \le 1 \qquad (27)$$

If d_{AL} is not very thin, α must differ appreciably from 1 and in that case the internal field may be high enough to cause switching.

Charge separation in an SSFLC cell can occur also if voltage pulses switching the cell in one direction are applied continuously. A picture can finally be burnt into the cell which becomes unswitchable.[30]

5 MULTIPLEXING OF FLC DISPLAYS

5.1 Matrix Arrangement of the Electrodes

A liquid crystal display consists of a great number of picture elements, so called *pixels*. Making individual connections to all these elements is technically impossible. The solution is offered by multiplexing techniques. In a typical display the electrodes are arranged in a rectangular matrix of horizontal and vertical stripes, called rows (or lines) and columns, respectively. The area where a row and a column electrode overlap forms a pixel. Each pixel is exposed to a superposition of voltage sequences delivered to both its electrodes. An image can then be created by sequentially applying a *selection waveform* to the rows while supplying *data waveforms* simultaneously to all columns, as schematically shown in Figure 20.

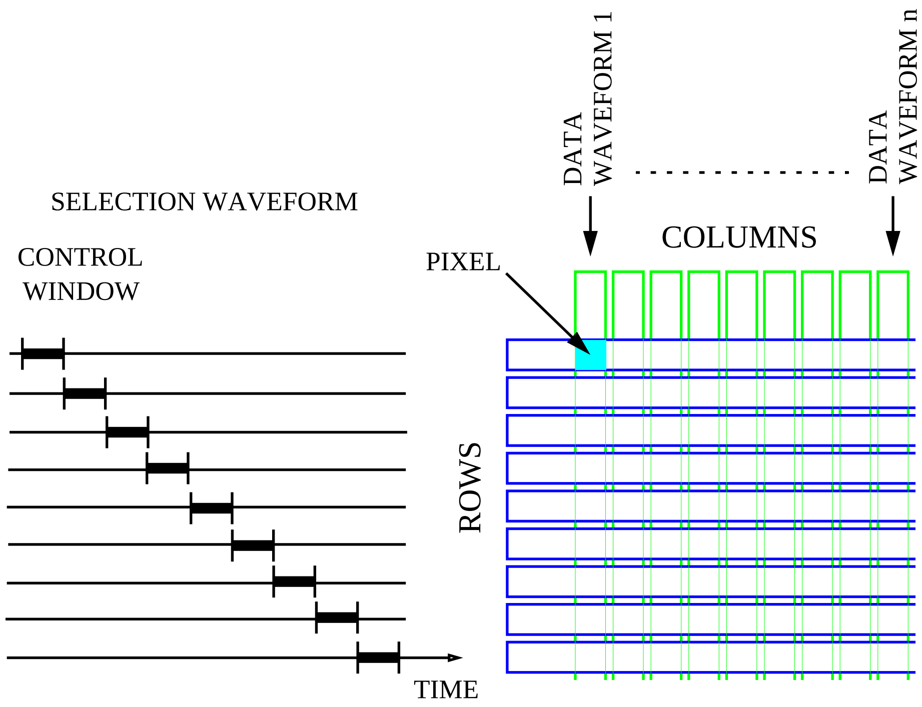


Figure 20. Matrix arrangement of electrodes in a typical SSFLC display. An image is created by sequentially applying a selection waveform to horizontal electrodes (scanning) while supplying data waveforms simultaneously to all vertical electrodes. The control window of addressing is defined as the time period when the data intended for a given pixel appears on its vertical (column) electrode.

Generally, the data waveforms consist of voltage sequences, each leading to switching either *up* or *down* (bright or dark). The *control window of addressing*, as indicated in Figure 20, is defined for each line as the time period when such a voltage sequence intended for the desired pixel appears on its column electrode. The width of the control window defines the *line addressing time* T_a, that is the time required to determine the optic state of all pixels in one row.

The selection waveforms applied to the rows are invariable and all alike. They are only phase-shifted with respect to each other by the amount corresponding to the size of the control window. The selection waveform is built in such a way that only the data within the control window can determine the final optical state of each pixel in the addressed row. This optical state should not significantly be affected by any combination of data outside the control window.

A set of data and selection waveforms for a display is called the *addressing scheme*. Its proper design is quite involved. The most important requirements are:

- to assure as narrow control window as possible to allow high refreshing rate (frame rate) for the display;
- to assure a good optical contrast and viewing angle of the written image;
- to assure a flicker-free image;
- to assure a wide operating range (waveform parameters reasonably insensitive to variations in temperature and cell thickness);
- to provide, if possible, control of grey shades;

Moreover, as it will be shown later, the overall dc-content in the applied waveforms should be zero.

5.2 Scanning Methods

An SSFLC display can be scanned in several ways to suit specific needs.[36, 57] Normal scanning by selecting consecutive rows is an obvious technique. The frame time is here simply the line addressing time multiplied by the total number of rows. However, the line addressing time of high resolution SSFLC screens demonstrated so far is rather long and flicker free video images cannot be produced in such a straightforward way.

Below the frame frequency of 30 Hz, the image flicker becomes noticeable because of the difference in optical state of the pixels being addressed and the remaining ones. The apparent frame rate can be increased using an interlacing technique, common, for example, in low-price CRT computer monitors. Instead of selecting consecutive lines, one jumps over a few lines and selects every n-th row. Hence, if a display has N lines, one selects only N/n lines within the first subframe. Next, another N/n lines are selected during the subsequent subframe. In this way, a flicker caused by too low temporal frequency is suppressed by the increase in the sweep velocity. For example, in the 1120-row SSFLC display prototype, exhibited by Canon at the 2nd FLC Conference in Göteborg (1989), the frame frequency was only 6 Hz.[57] The field frequency was, however, 48 Hz (n=8) and no flicker could be noticed.

The interlacing technique works well with still images but does not solve the problems concerning motion pictures. The bistability of the SSFLC structure invites a compromise – if the entire screen cannot be refreshed at video rate, one should identify the areas where an image changes rapidly and the areas where it is nearly static. A best example here is the cursor on a computer screen – when it moves, one has to concentrate on refreshing its picture, so it does not fade out. The remaining display area can temporarily be omitted during scanning or refreshed less frequently (to maintain image uniformity). In the above mentioned prototype screen, the cursor image was updated at 200 Hz. Later a movie could be shown in a VGA-size (480 rows) window refreshed at 14 Hz. These parameters have been further improved in recent screens from Canon.[88]

Consequently, the refreshing rate of the screen can be diminished by adding a number of virtual rows. This method could be useful in combination with fast addressing schemes (discussed later), where the line addressing time is very short and a static image can be preserved by a hf-stabilization.

5.3 Conventional Addressing Schemes

The simplest example of an FLC addressing scheme is the first published one (1985), the so called *Seiko* scheme,[14] which is still used as a reference in the literature. It evolved straight from driving methods used for nematic liquid crystals. In the Seiko scheme each data sequence consists of a pair of pulses of opposite polarity and equal amplitude $\pm V_D$. The selection waveform has a corresponding pair of pulses of amplitude $\pm V_S$ during the control window and zero voltage elsewhere. The widths of all these pulses are equal and are normally referred to as *time slots*.

If the pulse-pairs in data and selection waveforms have the same polarity within the control window (as sketched in Figure 21a), the pixel experiences a smaller voltage $|V_S-V_D|$ that is supposed not to affect the pixel's state. On the contrary, when these pulses are inverted with respect to each other (cf. Figure 21b), their amplitudes add up and produce a bipolar switching pulse $|V_S+V_D|$. With such an arrangement it is possible to switch the pixel into one state (dark or bright, depending on the order of pulses in the data sequence) or leave it unchanged. Two scans are needed for writing a complete picture - one subframe for writing bright pixels and another for the dark ones. It is thus a four-slot addressing scheme.

Figure 22 shows the Seiko scheme applied to a cell filled with SCE8 liquid crystal. (All cells utilized in this work are described in Chapter 10.3 *Preparation of SSFLC Cells* (page 96) and Chapter 10.4 *Parameters of the Experimental Cells* (page 97).) The ratio between the amplitudes of the selection and data pulses (V_S:V_D) is typically 4:1, which gives a ratio 5:3 between switching and non-switching amplitude. If V_S = 16 V, V_D = 4 V and the slot is τ = 330 μs (as in this example), the pixel has to switch at 20 V and not change state in response to 12 V pulses. Between the subsequent control windows the pixel is subjected to a series of pulses of amplitude equal to ±4 V. Their width is one or two slots (330 or 660 μs in this example). The adding-up occurs when data alternates between bright and dark. The chess-board-pattern is thus considered the "worst case" for many addressing schemes. It is clear that such large-area pulses strongly affect the instant optical transmission of the pixel, causing

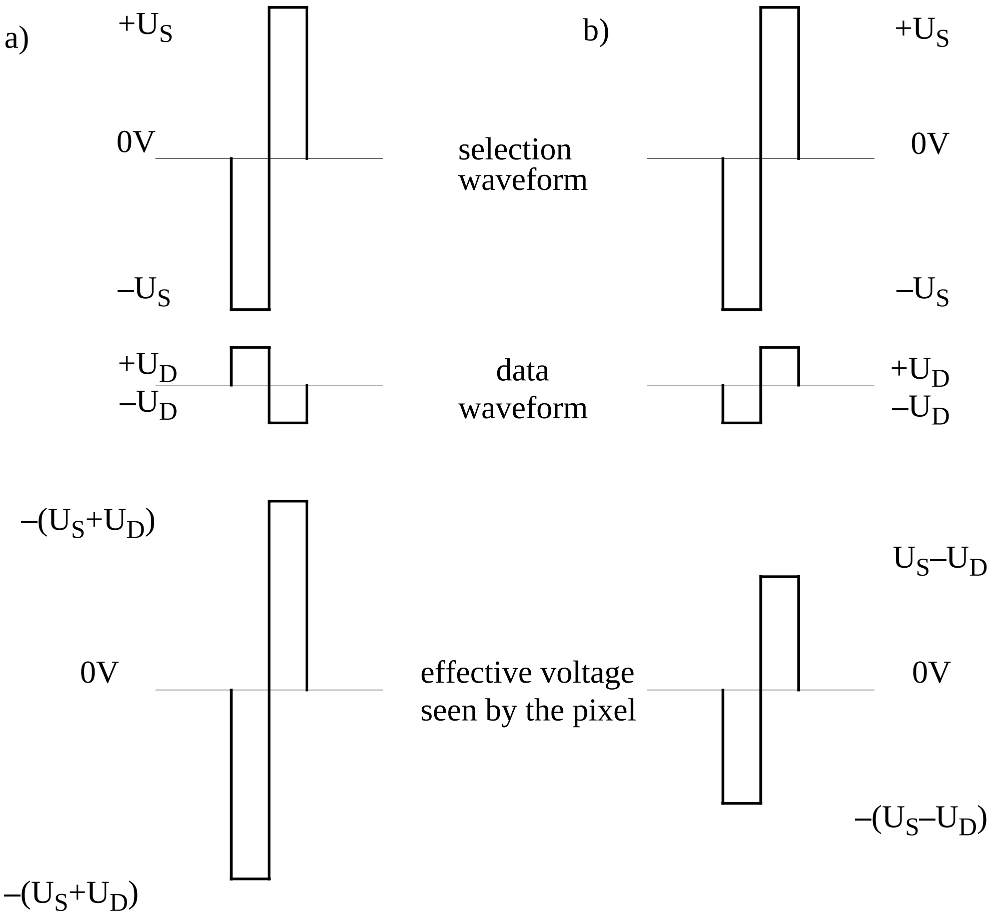


Figure 21. The superposition of the pulse pairs in selection and data waveforms, as used in the Seiko scheme. In this example the amplitude ratio of switching and non-switching pulses is 5:3.

substantial oscillations. Hence, the overall optical contrast based on average transmission levels is quite low.

A different approach was used in the *Chalmers 5-slot* addressing scheme (presented at the Berkeley Conference, 1986) shown in Figure 23 (Paper I). Here the aim was to achieve a high selection ratio defined as a proportion between the amplitudes of switching and all non-switching pulses. As compared to the Seiko scheme, the selection and data waveforms are much more complex. Four voltage levels: 0, U/3, 2U/3 and U are used. Switching pulses are thus ±U and non-switching ones only ±U/3, separated from each other by a zero-voltage time slot to prevent the add-up effect. Only one scan is required to write an entire image since the superposition of the selection waveform with a corresponding data waveform produces, within the control window, a pulse sequence completely switching a pixel to the dark or bright state.

The presented scheme allowed to demonstrate for the first time a dynamic pattern on a 16 by 16 elements SSFLC matrix (Paper I). By artificially addressing non-existing rows, multiplexing ratios beyond 1000:1 were simulated, proving that the number of rows in an SSFLC display is virtually unlimited, without loss of the excellent contrast achieved (see

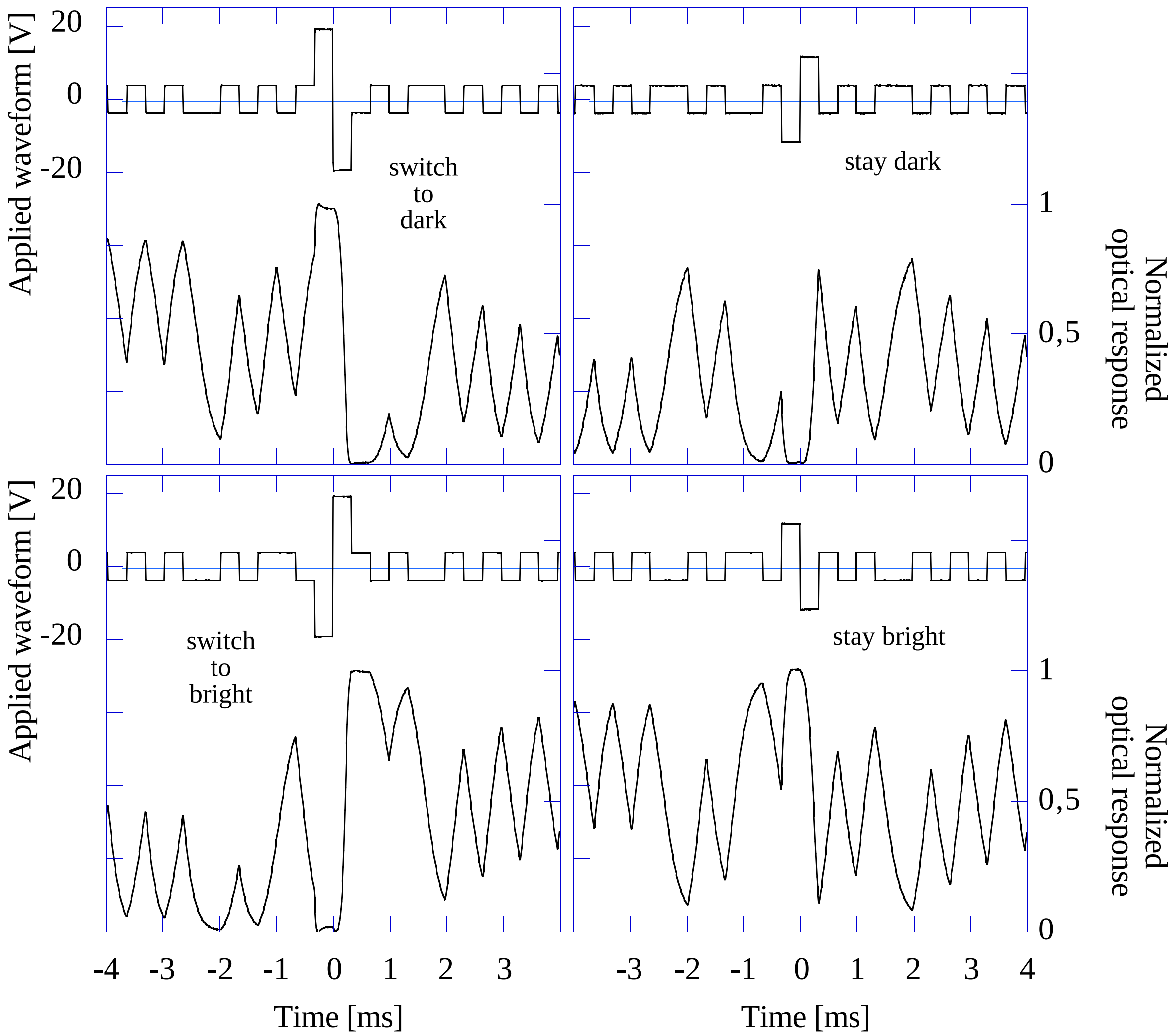


Figure 22. The Seiko multiplexing scheme (SCE8 cell at 24°C). Amplitude of selection waveform is 16 V and data waveform 4 V. One time slot is 330 µs, which gives the effective line addressing time t_a = 1320 µs. The long slot duration gives rise to large optical response oscillations on a millisecond time scale in spite of a very small amplitude of the crosstalk field. For the cell parameters, see Chapter *Experimental Cells and Setup* (page 93)

Figures 2-5 of Paper I).

The 5-slot scheme was further improved (Paper II) by reducing the number of required time slots to four, as shown in Figure 24. These slots were subdivided in halves resulting in crosstalk pulses of twice the amplitude but half the width as compared to the previous scheme. The contrast enhancement effect of the dielectric torque was increased in this way. The crosstalk pulses were separated by one or one half-slot period to prevent adding up. Utilization of the pause periods in these early addressing schemes reflects the opinion that the crosstalk pulses were disturbing and should simply be kept as small as possible. This approach has been abandoned in the modern addressing schemes discussed further on. The Chalmers 4-slot scheme is a step in the correct direction, trying to utilize dielectric effects. Nevertheless, introduction of pause periods leads to significant disadvantages. An obvious one is the waste of

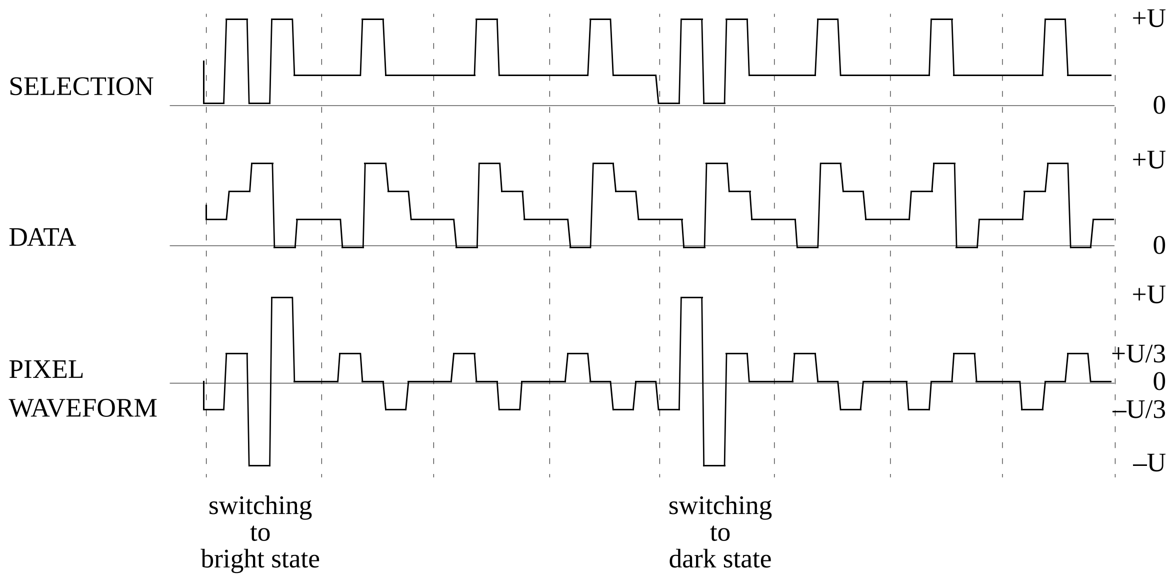


Figure 23. Chalmers 5-slot SSFLC multiplexing scheme (Paper I) shown as 4-way multiplexing. The selection and data waveforms have the same amplitude U and pulses are created using voltage steps of U/3.

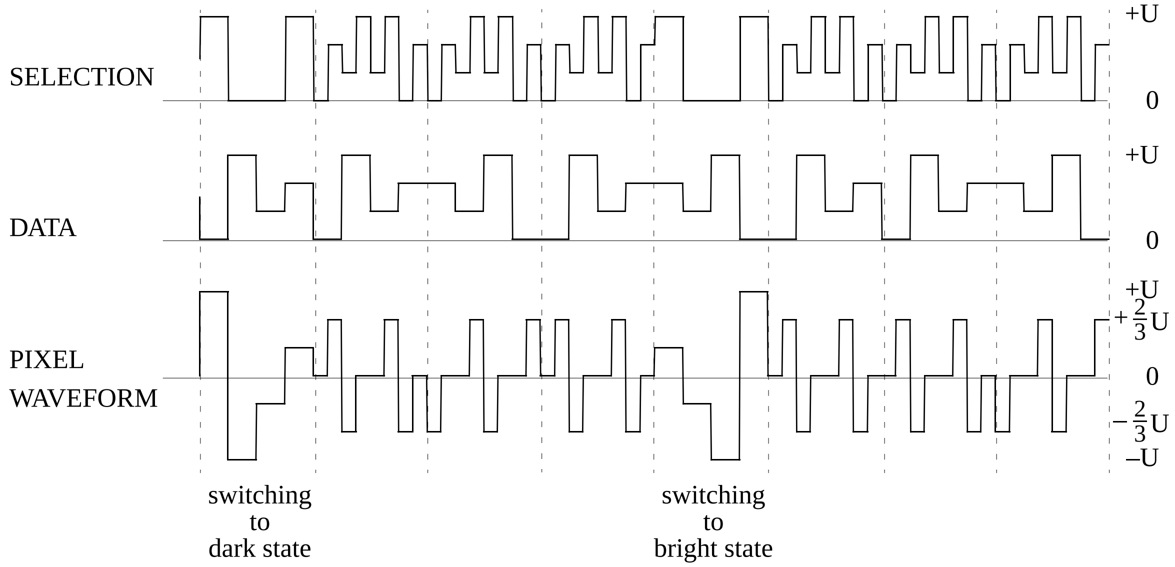


Figure 24. Chalmers 4-slot scheme with attempt to enhance the contrast dielectrically (Paper II). The slots are subdivided in two parts producing the crosstalk pulses of amplitude ±2/3 U but half the width, as compared with the previous scheme (Figure 23).

time. Moreover, as discussed in Chapter 4.3 *Bipolar vs. Monopolar Switching* (page 22), the SSFLC structure is more sensitive to the pulses preceded by a zero voltage period rather than by a counter pulse. The use of pause periods results in undesirably large oscillations in the optical response during the non-selection time reducing the achievable contrast.

5.4 Blanking

Presentation of video images requires a sufficiently high frame rate. It is widely assumed that the standard VGA resolution needs the line addressing time of 64 μs. This requirement cannot be met using the schemes presented above. Only a limited improvement can be achieved by developing faster liquid crystal materials and, to some extent, by rising the driving voltage. A new approach is therefore essential.

In the Seiko scheme the amplitude of the two pulses in the control window changes simultaneously so that the switching occurs either on both of them or none, resulting, as discussed before, in the need of two scans. If one now lets the first pulse remain large and only changes the amplitude of the second pulse, switching into either state within just one scan should be possible. In such a case the first, large pulse switches the pixel into one predetermined state. This is usually referred to as *blanking* or *erasing*. The pixel can then either remain in the erased state or be switched into the opposite one by the action of the second, *writing pulse*. The amplitude of the writing pulse varies according to the data sequence supplied to the pixel's column.

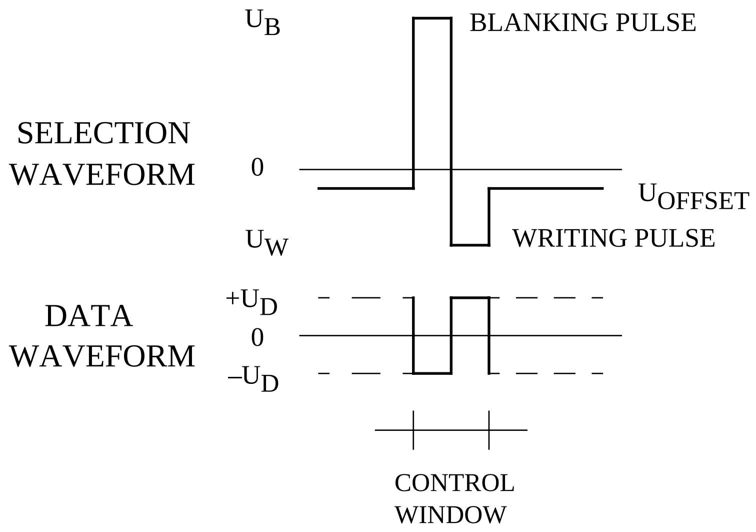


Figure 25. The idea of the GEC 2-slot addressing scheme. The large blanking pulse is dc-balanced by a constant offset. The data sequence drawn here results in latching on the writing pulse. The pixel remains in the dark state in case of opposite polarity of data pulses.

However, the dc-balance of such a multiplexing scheme would be unsettled. In the solution proposed by the GEC[18] and schematically shown in Figure 25, the dc-balance is restored by a small, constant offset in the selection waveform. The data waveform still consists of bipolar pulses and thus remains balanced. The amplitude of the erasing pulse obviously depends on the polarity of the applied data sequence and equals $U_B \pm U_D$ (using the notation from Figure 25). These values have to be adjusted so that even a blanking pulse of the amplitude $U_B - U_D$ accomplishes latching. The same applies to the writing pulse, where an amplitude of $U_W - U_D$ should not disturb the latched state, while an $U_W + U_D$ pulse has to fully change the optical state of the pixel. The required dc-offset is in this case given by:

$$U_{OFFSET} = \frac{U_B - U_W}{2(N-1)} \tag{28}$$

where N is the number of scanned lines (the above equation is stated incorrectly in the original paper[18]). If U_B = 20 V, U_W = -10 V and U_D = 4 V, the offset is only –25 mV in the case of a 200-row display. It is a very small value, which should not change the switching characteristics of a display panel. The main disadvantage lies in the complication of the driving electronics.

5.5 Time Overlap of Selection Waveforms

The use of a constant offset can be avoided by extending the addressing sequence over non-selected rows (blanking before writing) and eventually alternating selection polarity for consecutive frames. This kind of thinking was pioneered by the LETI group (Grenoble)[19,33] and has influenced much of the succeeding work. In the *N31* ("Normal Three-One") scheme the erasing pulse is three slots wide, "borrowing" two time slots from the preceding selection sequence. Since the row voltage stays constant during the overlap period, the area of this part of the erase pulse does not depend on the applied data (still consisting of a bipolar pulse pair). To clarify this point, the N31 scheme is sketched in Figure 26. The selection waveform is heavily unbalanced and its polarity has to be inverted for each consecutive frame.

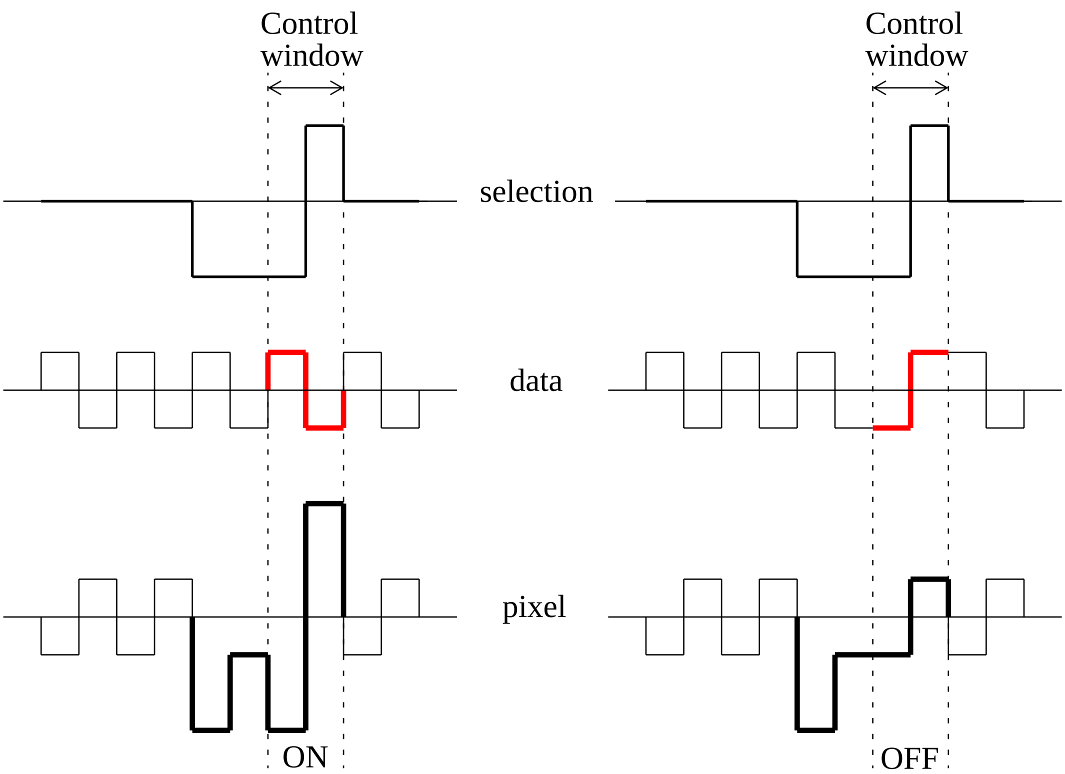


Figure 26. The superposition of the selection and data sequences in one frame of the N31 addressing scheme used by LETI. To assure dc-balance the polarity is inverted in the other frame. Data outside the control window are chosen arbitrarily.

It is, in fact, not necessary for the erase pulse to have a constant area. It only has to be large enough to cause latching under all conditions. In the *LETI-Bari N21* addressing scheme[32] the erase pulse was shortened to two slots reducing the transient dc–unbalance. This scheme was practically implemented to demonstrate video pictures on a small display.[31] In comparison with the Seiko scheme (Figures 21 and 22) the blanking technique allows better discrimination between writing and non-writing pulses, so that a smaller amplitude of the data waveform can be used. It also produces more reproducible and less distorted state before the writing pulse, which then can be made shorter. Since the N21 scheme is not dc-compensated on the row side, the polarity of the selection waveform has to be inverted every frame. This may cause low frequency flickering, which can be avoided by interlacing odd and even frames, so that for example row *i* is erased to the bright state, while row *i+1* is erased to the dark state and so on.[51]

The N21 scheme operates faster than previously described addressing schemes, which suppresses the crosstalk-induced oscillations in the optical response. Nevertheless, the bipolar data pulses may add up producing large deviations from the mean transmission. Several schemes, like for example the Chalmers 5- and 4-slot, contained a dead time in attempt to neutralize this effect. A better solution was presented by Dijon *et al.*[51] who converted the N21 scheme by shifting the selection sequence during even frames one slot to the left (Figure 27).

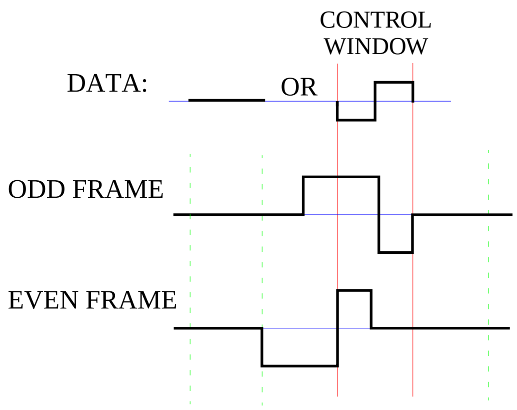


Figure 27. The Crosstalk Free (CTF) addressing scheme, where one of the data sequences is replaced by a zero voltage period. The selection sequences are shifted by one slot in respect to each other in odd and even frames. As their polarity is also inverted, the meaning of the data (on or off) is reversed.

In this case one of the two data sequences could be reduced to a zero voltage pause. To maintain the same discrimination between writing and non-writing pulses, as in the N21, the amplitude of the data waveform has to be doubled. The operation of the Crosstalk Free (CTF) addressing scheme is presented in Figure 28.

Further experiments revealed that a multiple erase sequence provides better separation from an initial state of the pixel and also eliminates the necessity of frame reversal. An example of such an addressing scheme is the “4631”[84] - the name refers to the number of time slots occupied by respective parts of the selection sequence – four, six, three and one, i.e. triple erase and a writing pulse (Figure 29).

Figure 30 presents the optical response of the SCE8-cell subjected to the “4631” addressing scheme. The data within the control window changes the size of the writing pulse and the switching toward either state is achieved. For the sake of comparison, oscilloscope traces corresponding to switching into dark and bright state are superposed. In the applied waveforms, only the data sequence within the control window is changed. Naturally, it has been checked during the experiment, that changing data anywhere outside the control window do

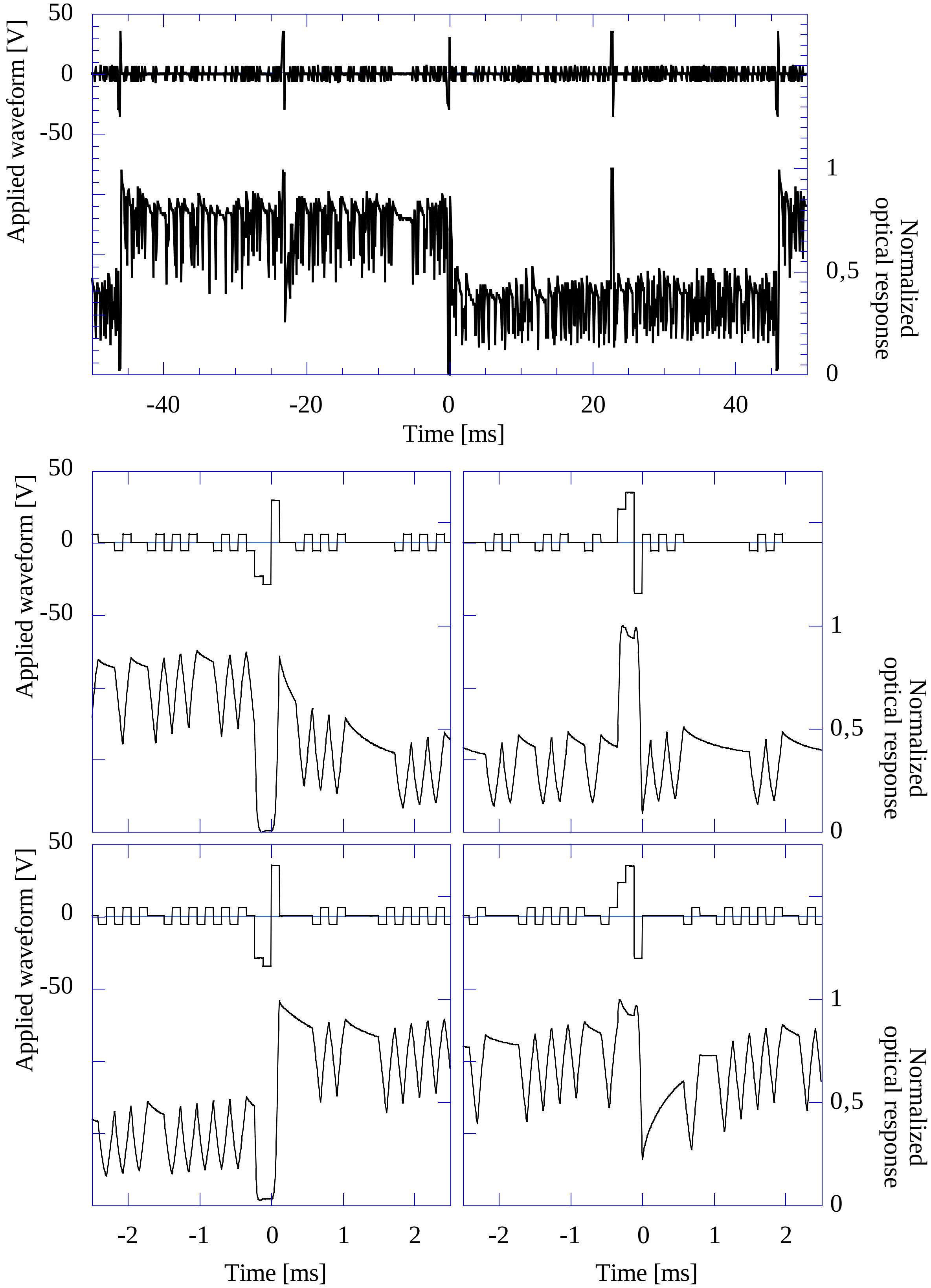


Figure 28. The CTF addressing scheme applied to the BDH858 cell. The amplitude of the selection waveform is 30 volts and data – 6 volts. The line addressing time is 230 microseconds.

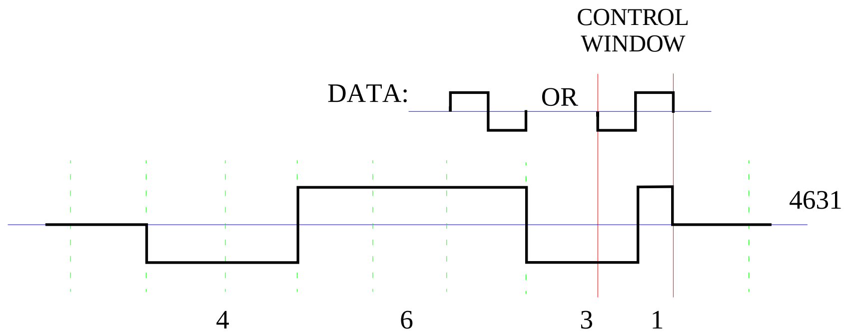


Figure 29. The selection waveform used in the “4631” addressing scheme. Multiple erase is performed by 4, 6 and 3 slots wide pulses, respectively. Applied data (analogous to presented in Figure 26) alters the area of the last, writing pulse.

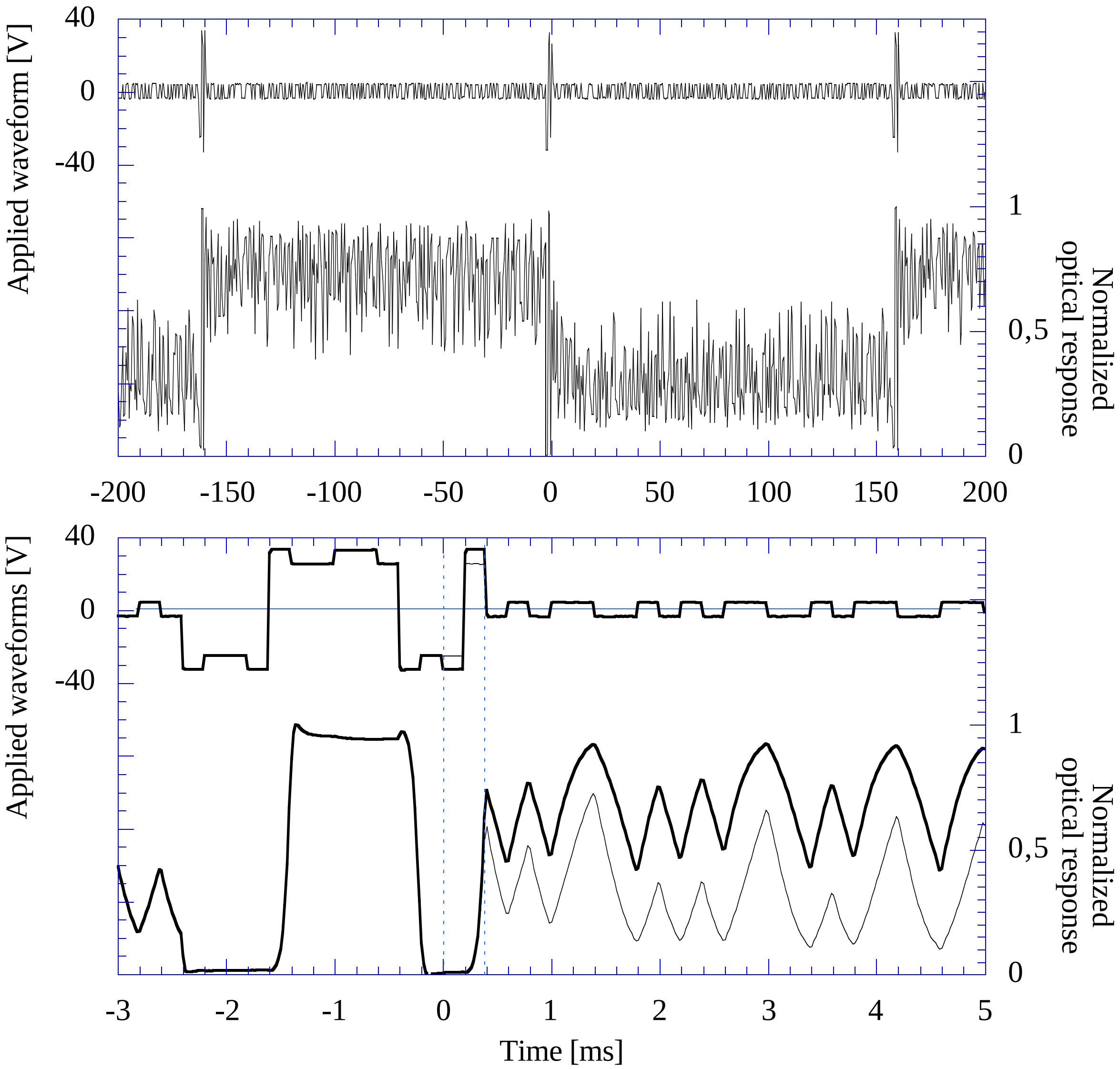


Figure 30. The “4631” addressing scheme applied to the SCE8 liquid crystal test cell. Amplitudes of the driving waveforms are 30 V and 4 V for the selection and data, respectively. The slot time is 200 µs (t_a = 400 µs). The upper diagram shows the optical response of one pixel in a 200-row display. The lower diagram gives a magnified view around the control window of addressing (between vertical dotted lines). Thicker lines show the applied pulse sequence and the corresponding optical response for switching into the bright state. Inverting the data within the control window results in switching into the dark state. This situation is drawn by thinner lines.

not affect switching. This remark applies to all experimental figures presented in this work.

5.6 Leading Pulse Latching

Looking again at the Seiko scheme, as the simplest example, it can be seen that the switching sequence consists of a pair of pulses of opposite polarity. The working point of this addressing scheme was originally set to achieve latching by the second (*trailing*) pulse. The first (*leading*) pulse was used solely as a dc-compensation. This resulted in a very slow operation – the line addressing time was, in each of the two subframes, approximately twice the switching time. Low frequency of the data waveform caused extensive oscillations in the optical response. The question arises if it is the only possible approach.

It has already been pointed out in Chapter 4.3 *Bipolar vs. Monopolar Switching* (page 22) that switching from a relaxed state is significantly shorter than switching from the saturated state in the sense that it requires a shorter writing pulse. The SCE8-cell required bipolar pulses of 330 µs to achieve clean latching, as it was shown in Figure 18, while a monopolar pulse switched within just 100 µs (at 30 V amplitude). One could then expect that also in the Seiko scheme *latching on the leading pulse*[29] should be achieved in a shorter time than on the trailing pulse. Let us make an experiment and increase the frequency of the applied addressing waveforms. Naturally, at first the image disappears as the scheme leaves its operating region. After further increase of the frequency the image reappears, but this time in the inverted, and also improved, contrast. Analyzing the optical response on the oscilloscope (Figure 31) one can clearly see that the leading pulse fully switches the pixel, while the trailing pulse is too short to be able to change the pixel's state. The slot time is 118 µs (after slight adjustment in waveform amplitudes), as compared with 330 µs in the original Seiko operating mode (Figure 22). Moreover, higher frequency of data sequences drastically reduces the oscillations by enhancing the hf-stabilization effect. Faster operation due to the leading pulse latching does not change the fact that the Seiko scheme is effectively four slot, so the effective line addressing time for the SCE8-cell is nearly half a millisecond.

5.7 The Minimum Voltage-Time Product

The addressing schemes discussed above were based on the assumption that the switching occurs when a pulse of an area (voltage-time product) larger than the threshold value is applied. The threshold characteristics were usually presented as in Figure 32a and measured up to a voltage limit imposed by the destruction of smectic layer structure. This limit is lower in some substances and surprisingly a sharp bend in the characteristics was found.[17, 41, Paper IV]

Figure 32b presents the minimum voltage-time product (τ-V_{MIN}) characteristics of the SCE8-cell used in several addressing experiments included in this work. As can be seen, significantly different threshold curves are measured using bipolar and monopolar switching pulses.

The voltage at which the minimum response time V_{MIN} occurs is related to the (relative) dielectric biaxiality and spontaneous polarization, as found by Towler, Jones and Raynes,[70] by

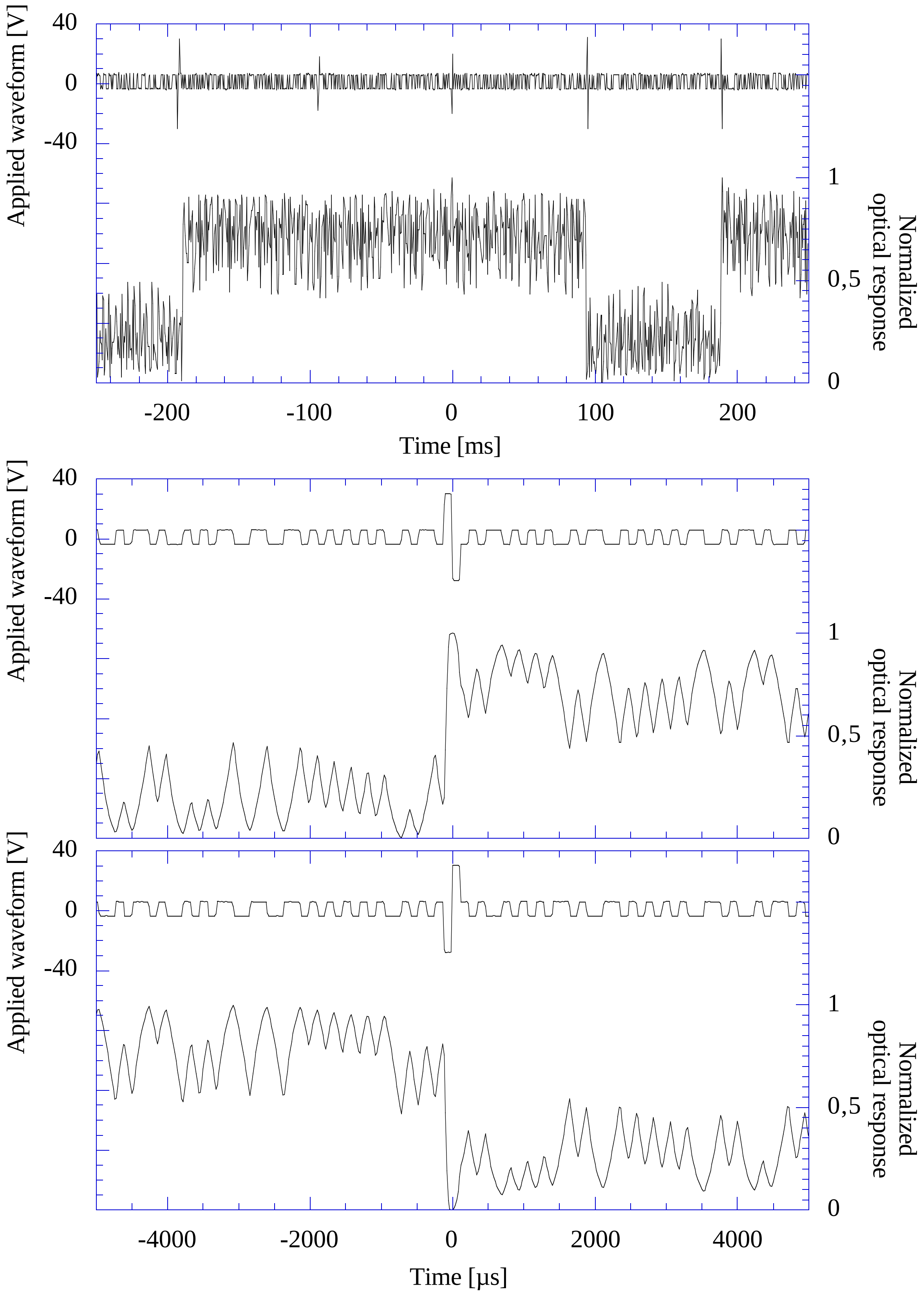


Figure 31. "Inverted Seiko" addressing scheme applied to CTH-HW19 cell filled with Merck SCE8 liquid crystal. Waveform amplitudes are 25 V and 5 V for the selection and data, respectively. The slot time is 118 µs and hence the effective line addressing time is 472 µs (two slots and two subframes). Upper diagram shows alternative up and down switching of one pixel in a 200-row display. Due to the necessity of two subframes the response is not symmetric. Lower diagrams show the leading pulse latching (compare with Figure 22).

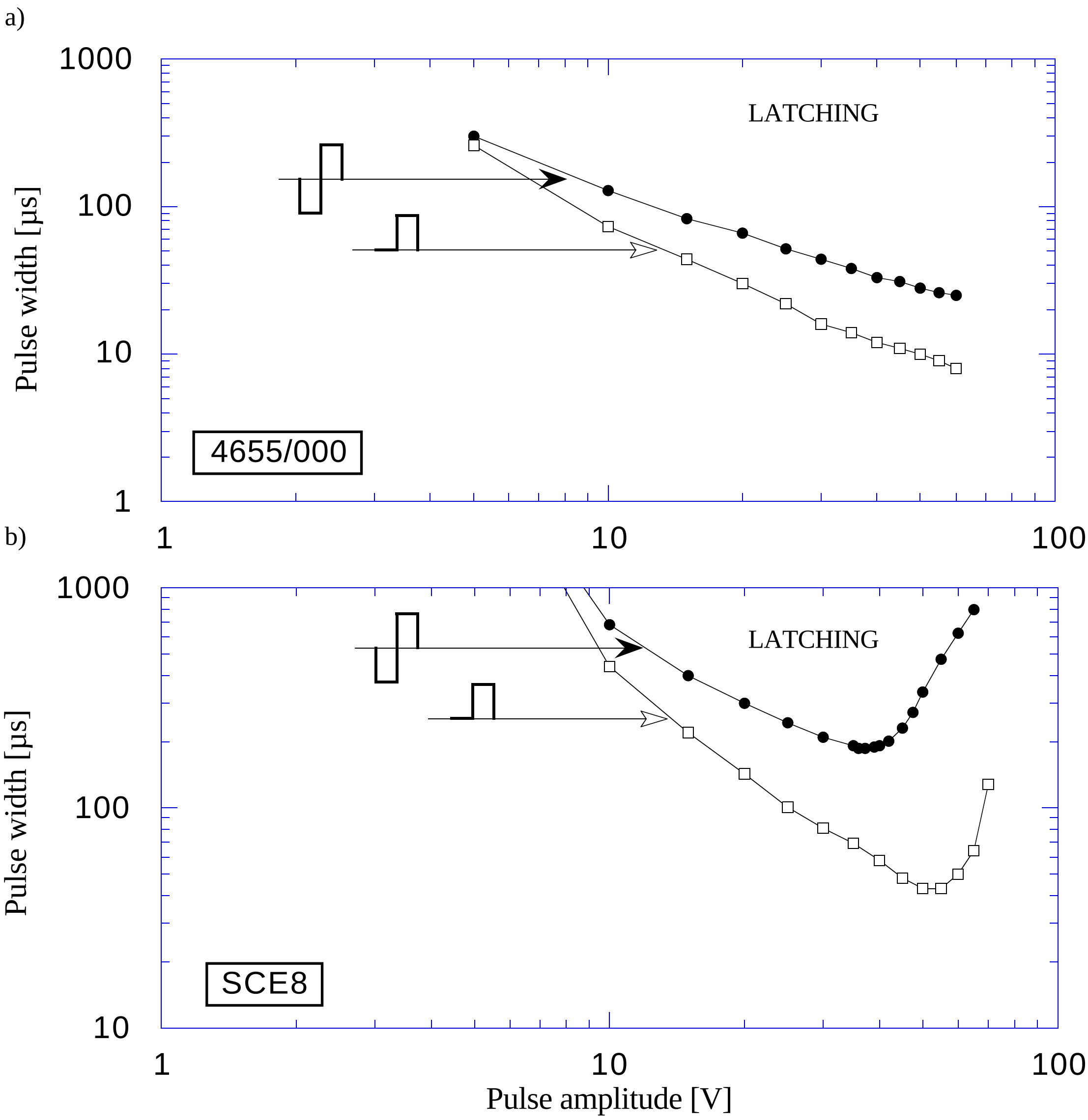


Figure 32. Minimum pulse width as a function of voltage required to switch an SSFLC cell between the two stable states by a bipolar and by a monopolar pulse sequence:
a) typical behavior measured in Merck 4655/000 liquid crystal (the 4655/000-cell at 24°C),
b) τ-V_{MIN} characteristics measured in Merck SCE8 liquid crystal (the SCE8-cell at 24°C).

$$V_{MIN} = \left|\frac{P_S d}{\varepsilon_0 \varepsilon_\Delta \cos\delta}\right| \tag{29}$$

and the minimum switching time is given by:

$$\tau_{MIN} = \frac{V_C t_C}{V_C\sqrt{\lambda}} = \frac{\eta_c \varepsilon_0 \varepsilon_\Delta}{P_S^2} \tag{30}$$

The lines denoting the threshold characteristics in Figure 32 correspond to a visibly clean

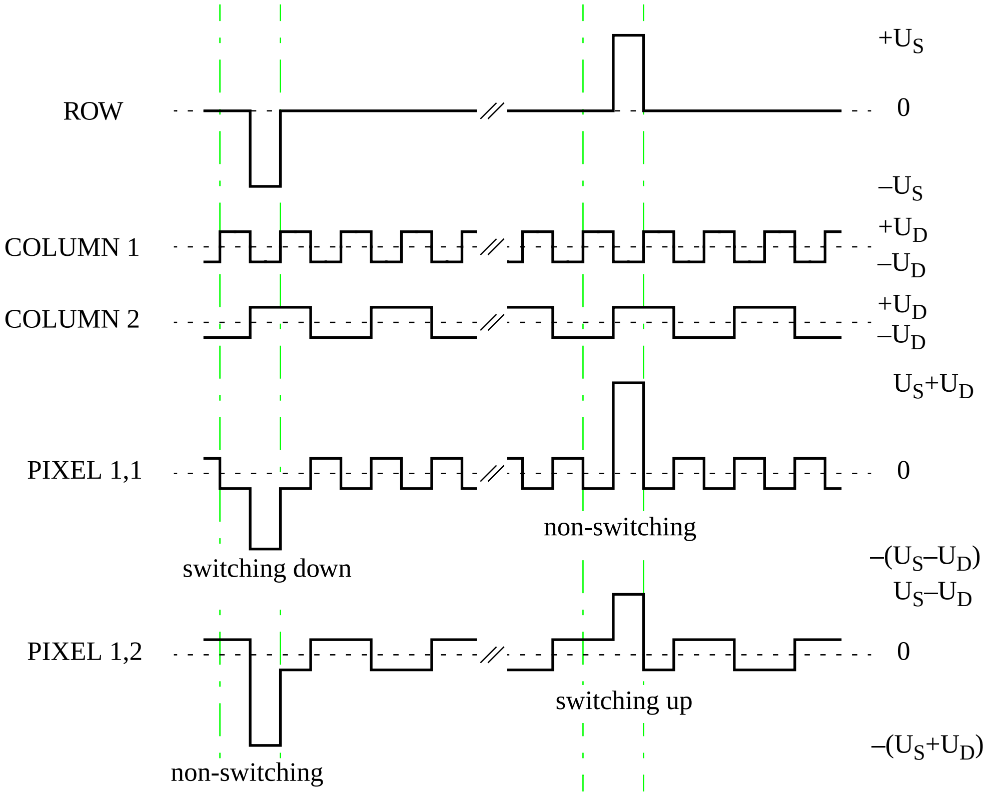


Figure 33. Four possible combinations of pulse sequences in the JOERS/Alvey addressing scheme, which is based on the τ-V_{MIN} type of threshold characteristics. Switching occurs for $\pm$[U_D ; U_S–U_D] sequence but not for $\pm$[–U_D ; U_S+U_D].

switching. Naturally, a partial switching (i.e. latching in some domains only) occurs while approaching this line. An interesting property is that the partial switching region is significantly reduced at voltages larger than V_{MIN}. Consequently, the discrimination between switching and non-switching pulses is better in the region above τ-V_{MIN} than in the normal part of the curve.

The τ-V_{MIN} behavior has been reported already in Paper IV and related to the dielectric properties. In Paper IX the switching dynamics has been studied to clarify which part of the response time – the delay, the rise time or both – causes the bend in the τ-V_{MIN} characteristics. The measurements show that the delay time is mainly a property of the cell and the liquid crystal. It is nearly voltage-independent and decreases only slightly with the increasing voltage. In contrast, the rise time is almost inversely proportional to the voltage in the region below V_{MIN} and diverges rapidly above it.

The existence of V_{MIN} leads to a situation where a larger pulse does not switch while a slightly smaller one does, and then an even smaller pulse does not switch again. It opens a way for new addressing ideas. The first to exploit this phenomenon was the JOERS/Alvey team.[60] Their scheme utilizes also a new kind of selection waveform - a *monopulse strobe addressing*. The row voltage is here zero during the first one of the two time-slots of the control window.

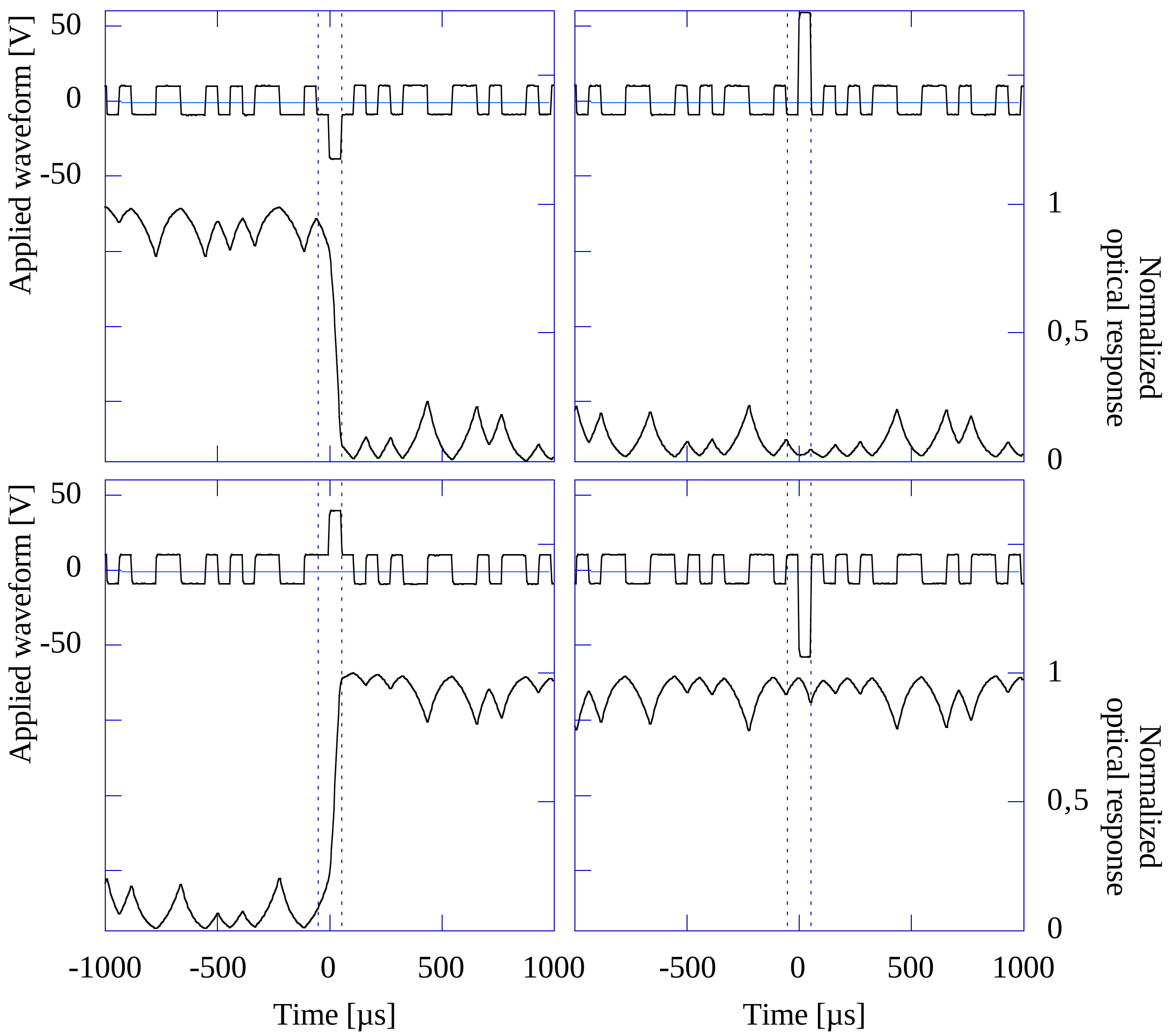


Figure 34. Optical response of a cell (CTH-HW19) filled with Merck SCE8 liquid crystal mixture to four combinations of selection and data sequences in the JOERS/Alvey addressing scheme utilizing the τ-V_{MIN} characteristics shown in Figure 32. Dotted lines mark the position of the control window with an oscilloscope trigger point (t=0) in the center. The amplitude of the selection waveform is 50 V and data 10 V, which gives the amplitude of the switching pulse equal to 40 V and the non-switching one 60 V. The switching pulse is preceded by a pulse of the same polarity, while the non-switching one by a counter pulse. The slot time is 55 µs and hence the effective line addressing time is 220 µs (2 subframes times 2 slots).

The superposition of the selection waveform with the corresponding data waveform produces either a switching or a non-switching sequence, as schematically shown in Figure 33. Two scans (with polarity inversion) are thus required to write one image, so it is still a four-slot scheme. The switching sequence consists of a medium size pulse having an amplitude of $|U_S-U_D|$ and preceded by an U_D pulse of the *same polarity.* On the other hand, the non-switching sequence consists of a large pulse of an amplitude equal to U_S+U_D, that is always preceded by an U_D pulse of the *counter polarity.* Figure 34 presents a set of close-ups showing worst-case sequences of the JOERS/Alvey scheme applied to the SCE8-cell. Looking at this figure and comparing the pulse sizes it seems clear that the JOERS/Alvey scheme utilizes the bend in

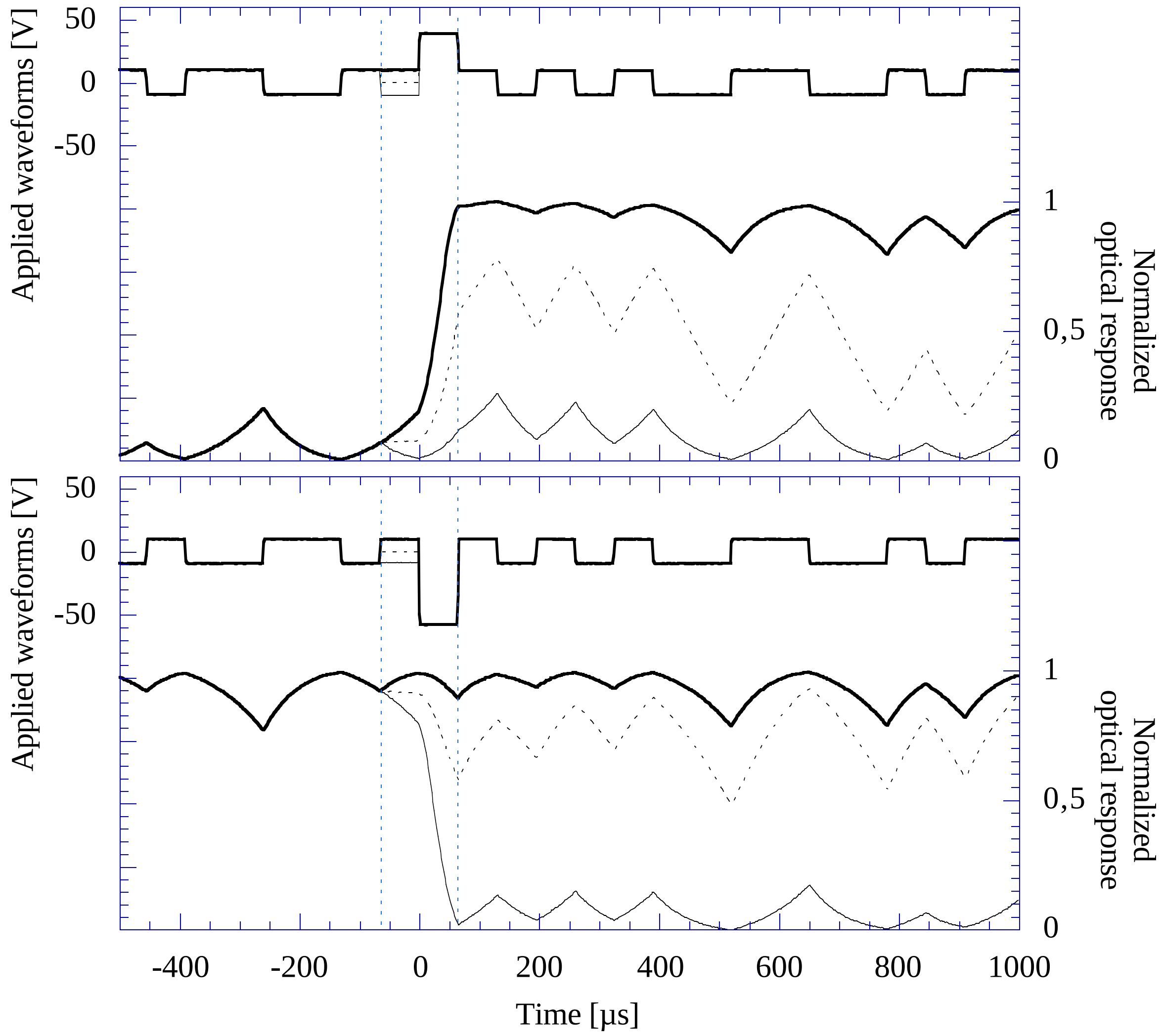


Figure 35. The importance of the shape of the leading pulse. Thicker lines correspond to normal operation of the JOERS/Alvey scheme as shown in Figure 34 (CTH-HW19 cell filled with SCE8, selection 50 V, data 10 V, slot 64 μs). Upper diagram presents the normally switching sequence and the lower diagram – the non-switching one. Broken lines show the effect of zeroing the leading pulse, while the effect of inverting its polarity is drawn by thin continuous lines.

τ-V characteristics. But is the polarity of a small leading pulse important? Let us make a simple experiment and invert just the leading pulse in a working JOERS/Alvey scheme. As can be seen in Figure 35 the effect is striking – the action of both switching sequences is also inverted! One might speculate that the polarity of the leading pulse changes the character of the switching pulse. If the leading pulse has the same polarity as the trailing one, the resulting sequence behaves like a monopolar switching pulse. In the counter case the behavior of the resulting sequence should resemble the one of the bipolar pulse, although the amplitude of the leading pulse is here much smaller. These two cases correspond to different τ-V characteristics. Figure 35 shows also the situation where the leading pulse is zero, which is supposed to give the monopolar behavior in both cases, but clean latching is not obtained. A slight increase in the pulse width (to 85 μs) to compensate for the area change is enough to return to the original operating mode, when a smaller pulse is the switching one (i.e. the pure τ-V_{MIN} behavior). This indicates that the above explanation is not entirely satisfactory and that more complicated phenomena are involved.

The effects of an electric field directly before, and also just after, the writing pulse will be further exploited in Chapter *Fast Addressing Modes* (page 51).

6 The Crosstalk Field

6.1 AC Contrast Enhancement

The data waveform inevitably produce crosstalk pulses on all pixels during non-select periods. In the conventional addressing schemes discussed in Chapter *Multiplexing of FLC Displays* (page 27) these pulses were considered “disturbing” and efforts were made to reduce them. On the other hand, it has also been shown in Chapter 4.1 *Polar Switching* (page 15) that the hf field may stabilize the director dynamically in a state of higher optical extinction. This effect is difficult to utilize in the conventional schemes due to the low frequency of the crosstalk field, where strong coupling with the ferroelectric torque causes extensive oscillations in the light transmission through the cell. Thus, if the crosstalk field is to be turned into advantage, its frequency has to be significantly raised. Addressing schemes presented in the next chapter fulfill this requirement.

Provided that the hf field has a high enough frequency, it can be used not only to stabilize the fully switched states, but also to complete the switching process after the end of writing pulse. This point is illustrated in Figure 36. The SSFLC cell is driven by a waveform described in detail in Chapter 10.5 *Test Waveforms* (page 98). The area of the writing pulse in the upper diagram is large enough to push the liquid crystal director past the “critical point” and the switching is completed toward the new (bright) state. The lower diagram shows the opposite case - a slightly too short writing pulse results in a return to the initial state. It is interesting to note that the difference in the switching pulse area is here only 8%.

Many experimental cells exhibit a completely different behavior. Their only reaction to the applied hf field are oscillations in the optical response around the field-off relaxation curve. A typical example is shown in Figure 37. We currently attribute this behavior to very strong surface anchoring. In fact, the cell presented here was intended for direct drive. It can be multiplexed by “normal” schemes, but it cannot work in addressing modes relying on high frequency effects. This example clearly shows that the cell technology for direct-drive applications differs significantly from the one intended for highly multiplexed displays. In a light chopper, for instance, the most important is perfect orientation and high contrast. Thus, strong alignment layers are preferable. In contrast, week alignment is adequate for multiplexed displays, if we want to use hf contrast enhancement effects.

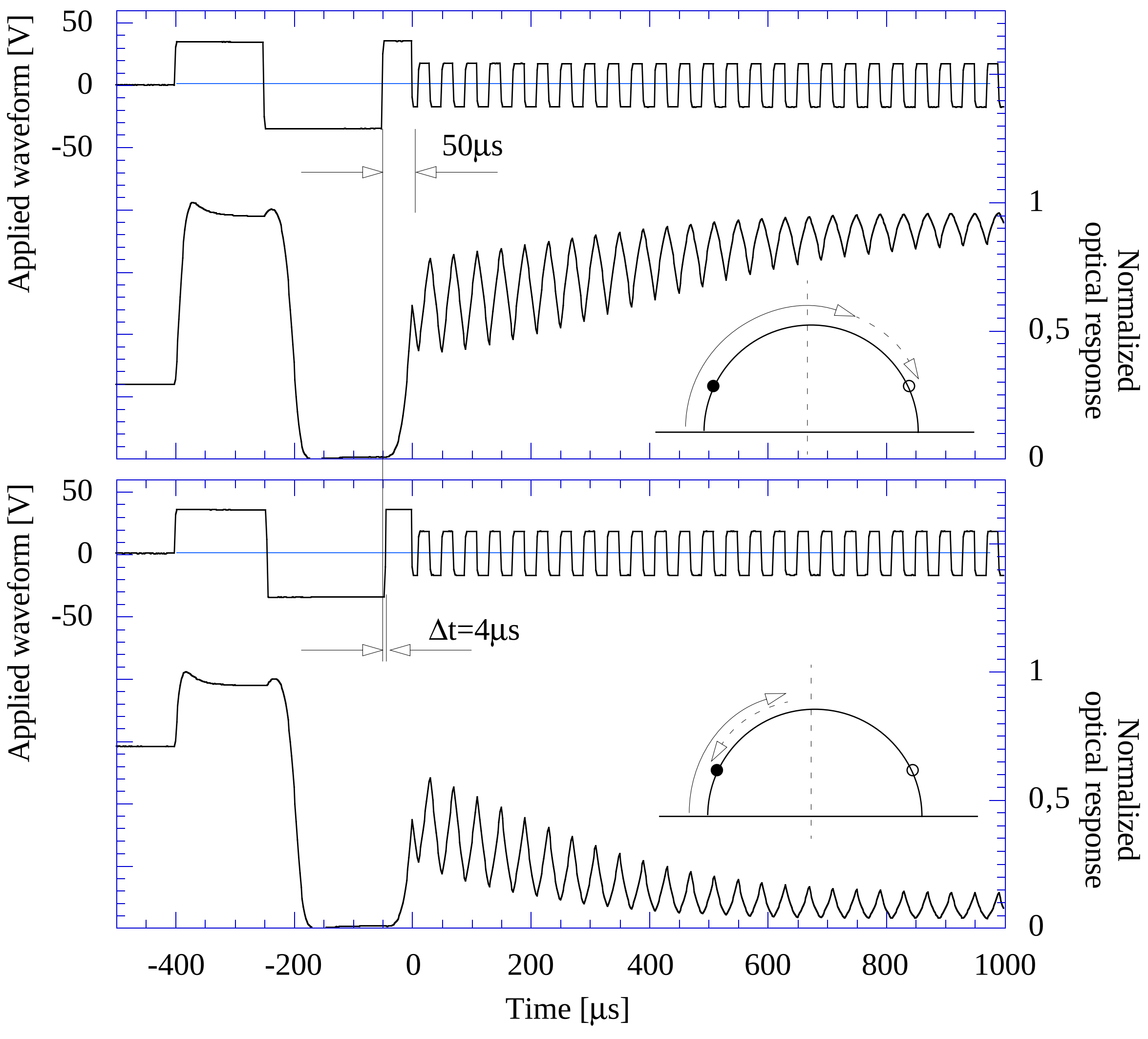


Figure 36. Utilization of the crosstalk field to complete the switching process. The switching pulse is 50 μs wide in the upper diagram and 46 μs in the lower one. The amplitude is 36 V in both cases, and the hf field is generated by a square wave of amplitude 18 V and half-period equal to 20 μs. The oscilloscope trigger point (time zero) is placed at the end of the switching pulse. Traces of the liquid crystal director corresponding to both cases are sketched in the diagrams. (4655/000 liquid crystal cell)

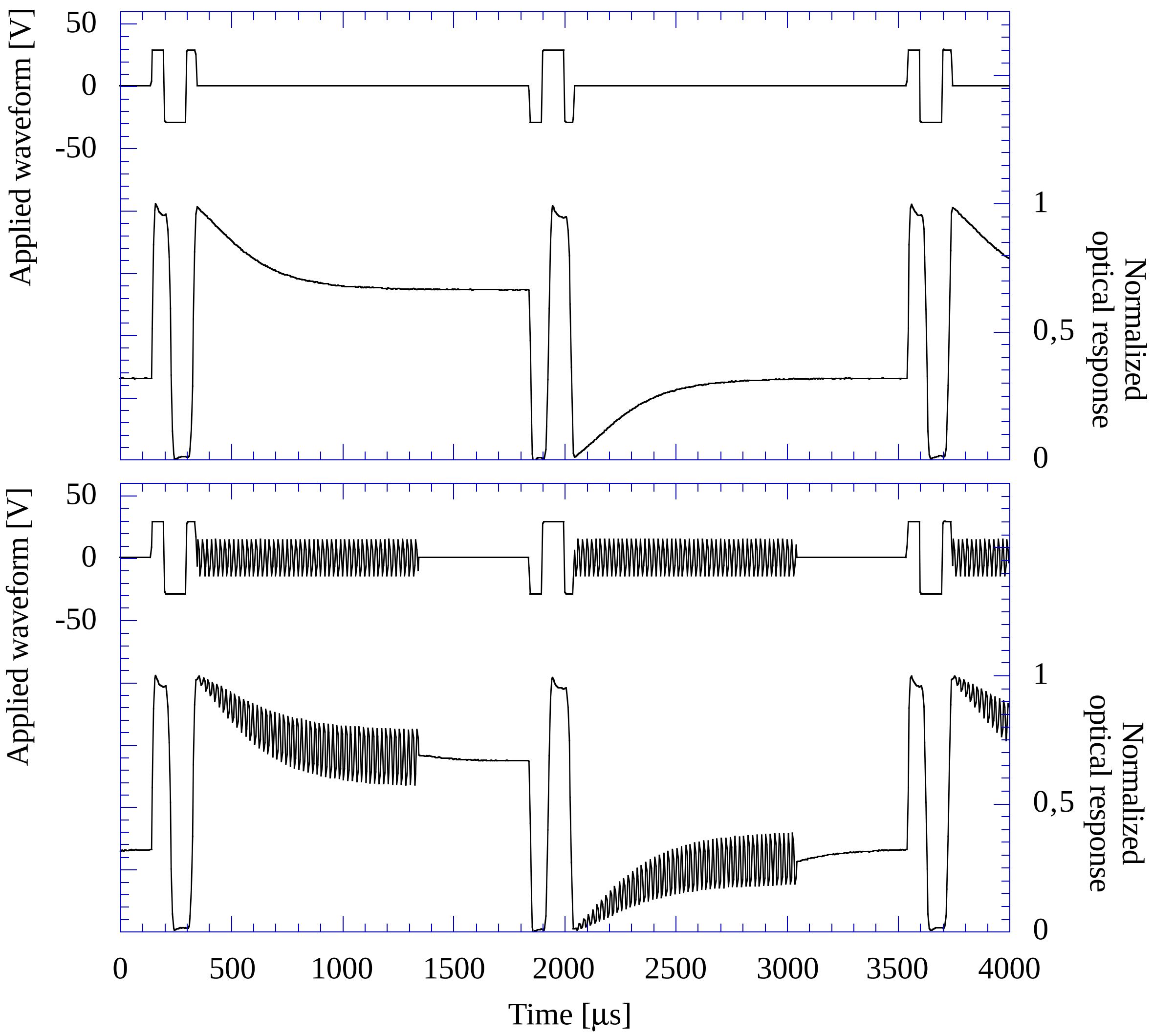


Figure 37. A typical example of the of hf stabilization effect in SSFLC cells with too strong boundary conditions. After the switching pulse, the director relaxes back to the memorized (surface-stabilized) state which only gives about 70% of full transmission. This state cannot be lifted up to a fully switched state. The additional hf voltage in the lower figure only induces director oscillations around the basic relaxation curve.

6.2 Design of Data Waveforms

During the scanning of a large display, each pixel experiences a crosstalk voltage for most of the time. It is, thus, important that the light transmission is not influenced by the data supplied to the column outside the actual pixel's time-window. A first, quite obvious requirement is that each data segment has to be dc-balanced – otherwise an offset stemming from long groups of the same data would cause switching, as shown in Figure 38.

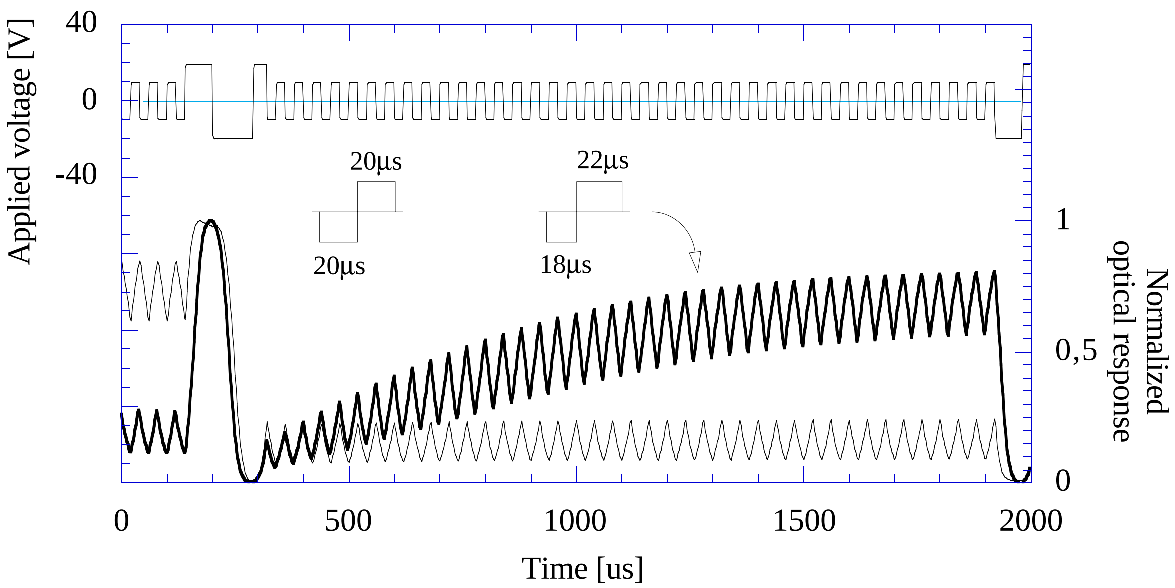


Figure 38. Illustration of the effect of a long series of unbalanced data segments. The data waveform is modelled here by a hf square wave (20 / 20 µs, ±15 V, thin lines). The thicker line shows the optical response after introducing a small asymmetry (18 / 22 µs) to the applied "data waveform". (4655/000 cell)

Even if dc-balanced, the crosstalk pulses in principle must affect the momentary light transmission through the pixel. As previously discussed, a typical data sequence consists of a pair of equal pulses of opposite polarity. When the data applied to consecutive pixels in a column alternates, as in the case of a chessboard pattern, the resulting crosstalk sequences are also inverted each time. This leads to the undesirable situation where neighboring pulses have the same polarity and add up to a two-slot wide pulse. This corresponds to halving the frequency of the field. As a result, enhanced image flicker or a temporal contrast change between different areas of the display can occur. The upper diagram in Figure 39 presents an example of oscillations induced by the conventional type of the data waveform in such a case.

By correct design of the data sequence the optical state of the pixel can be kept nearly constant. In the "crosstalk compensated" data waveform[32,71,82,83,Paper V] the compensation pulse is divided in halves and placed at the beginning and end of the sequence. Such a waveform never produces two-slot wide crosstalk pulses and the field frequency is effectively doubled. Fluctuations in the optical response are substantially reduced as can be seen in the lower diagram of Figure 39. Utilization of this kind of data sequence naturally requires redesigning of the selection waveforms. Examples of corresponding addressing schemes will be presented in the next chapter.

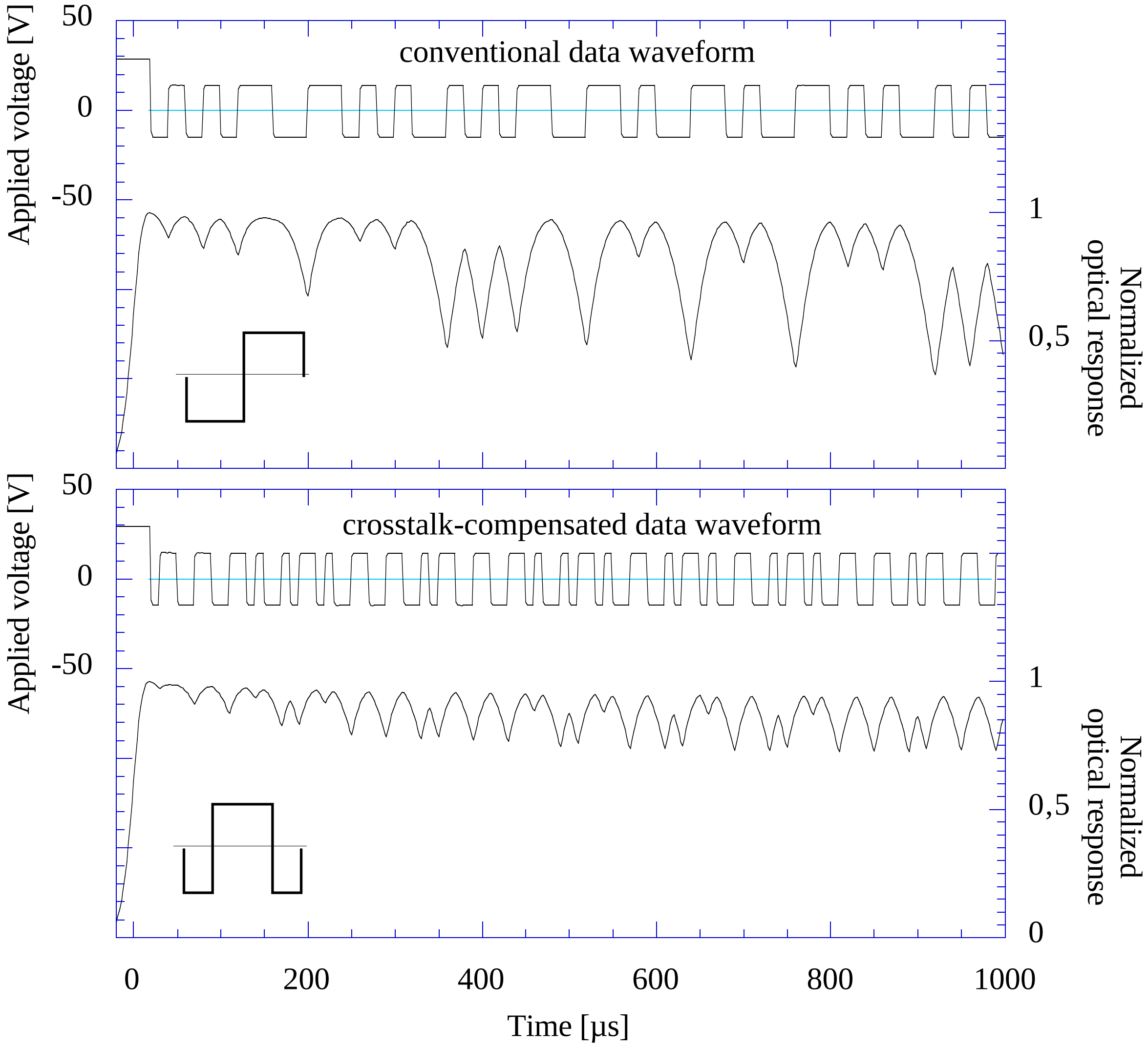


Figure 39. Oscillations in the electro-optic response of an SSFLC cell induced by a conventional (upper plot) and “crosstalk compensated” (lower plot) data waveform containing the same sequence of ON and OFF data. (4655/000 cell)

7 Fast Addressing Modes

7.1 Time Overlap of the Writing Pulse

It has been shown in previous chapters that the erase and dc-compensation sequences for a row of pixels in an SSFLC display can overlap in time with the process of addressing other rows (see Figures 26-30). Following this idea, why not "borrow" some time from the neighboring control windows to construct the writing pulse itself? This should be possible, since the difference between the writing and non-writing pulse width can be less than ten percent, as in the example presented in Figure 36. Hence, a major part of this pulse could be moved out of the control window. The corresponding addressing scheme then has to be designed such that the area of the "removed" part of the writing pulse is constant and independent of the column data.

In such a case the control window of addressing would be shorter than the writing pulse. There are two immediate advantages of this approach:

- the line addressing time can be made shorter than the intrinsic switching time of the FLC material,
- the increased frequency of the crosstalk field produces more efficient dynamic stabilization of the director, which should further suppress oscillations and increase contrast.

In a real addressing scheme it is much more difficult to achieve such clean differentiation of the writing pulse area as it was done in the test waveform. Reproducible initial conditions would certainly be of advantage, so a blanking sequence prior to the control window should be included. But how to design a correct writing sequence? In the simplest approach proposed by Hoechst[63] the bipolar pulse was extended on both sides of the control window by one time slot, as sketched in Figure 40 (denoted as the HOE scheme). Superposition of the selection sequence with the data waveform changes the area of both parts of the bipolar pulse. Since the pixel has already been erased, the leading part of the switching pulse can always accomplish saturated (fully switched) blanked state, independently of the variations in its area. On the other hand, the writing (trailing) pulse is sensitive to the area change. Figure 41 presents the HOE addressing scheme applied to a CTH fabricated cell filled with BDH858 liquid crystal. For the purpose of comparison, the oscilloscope traces corresponding to both on and off data

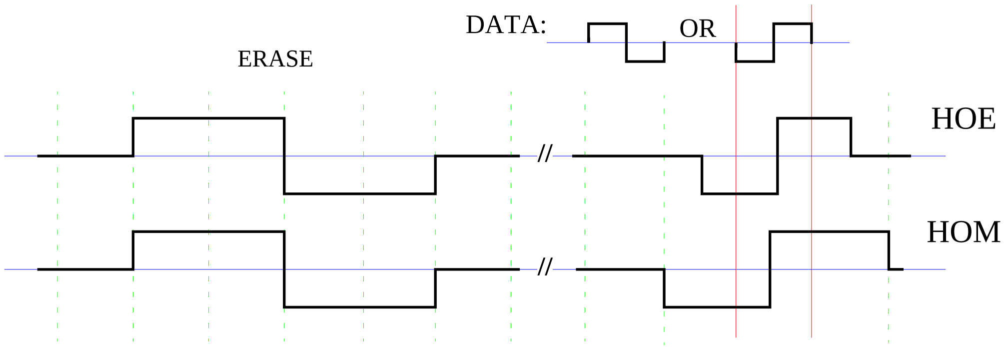


Figure 40. Selection waveforms of Hoechst (HOE) and modified Hoechst (HOM) addressing schemes. Prior to the writing sequence, the pixel is erased twice (in opposite directions) and then driven to the hf field stabilized state.

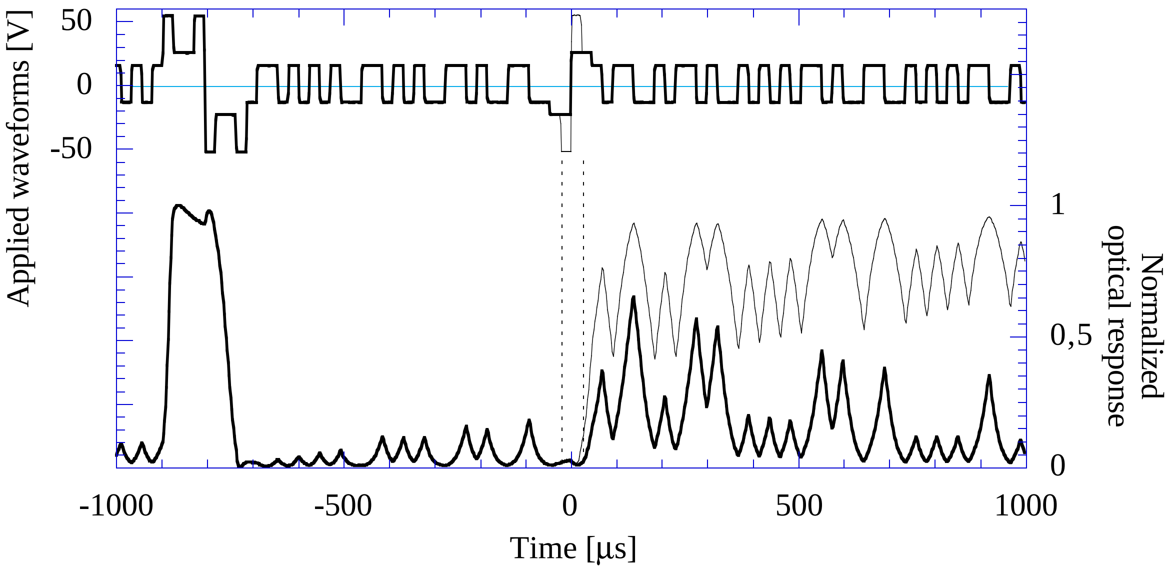


Figure 41. The Hoechst addressing scheme (HOE) applied at room temperature to the BDH858 liquid crystal cell. The selection and data are 40 V and 15 V, respectively. A 23 µs slot yields the line addressing time of 46 µs. The control window is marked by dotted lines and the oscilloscope trigger point (t=0) is placed in its centre. Thicker lines show the traces for switching into dark state; thin ones into the bright state. It can be seen that switching continues past the proper control window driven by the part of the writing pulse overlapping the next control window. The control window, and hence the line addressing time, is here shorter than the real switching time of the material.

within the control window are shown in the figure. The scheme works well and the line addressing time obtained here is 46 µs (i.e. twice the slot time of 23 µs, since the conventional data waveform is used here).

The effective width of the writing pulse is two slots in the HOE scheme. Is a further increase in the writing pulse width possible? In the "Modified Hoechst" addressing scheme proposed by Maltese *et al.*[95] the bipolar switching pulse extends over the entire preceding and succeeding control windows. The effective width of the writing pulse is, thus, three slots as shown in Figure 40 (denoted as the HOM scheme). The HOM addressing scheme applied to the same cell as the previous one yields the line addressing time of 30 µs (Figure 42).

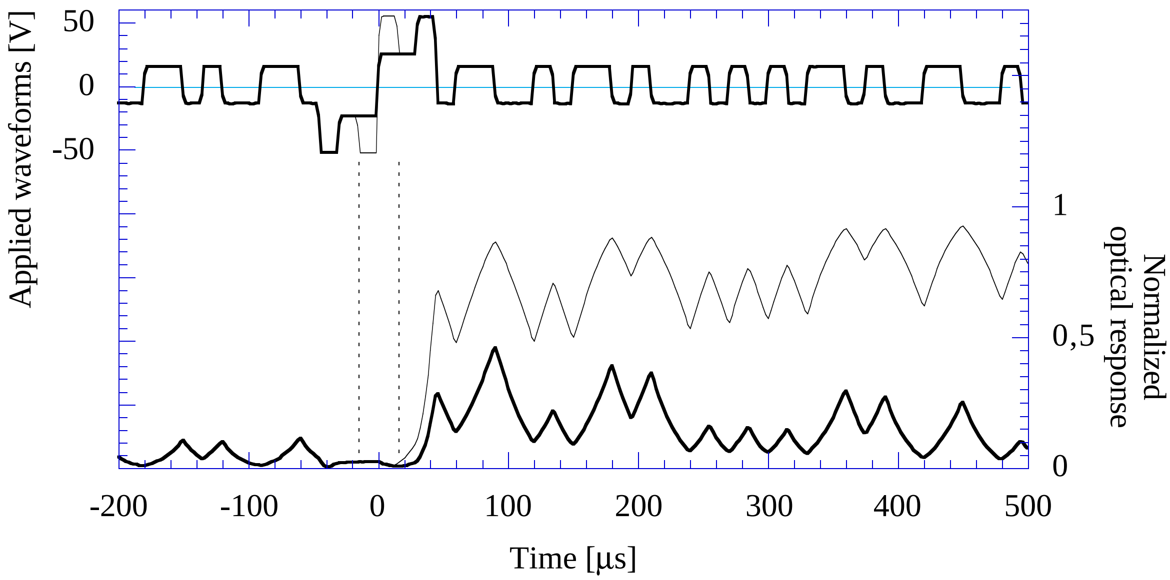


Figure 42. Modified Hoechst addressing scheme (HOM) operating in the same conditions as the original Hoechst scheme shown in the previous figure. The time slot is shorter and equals 15 µs, which gives the line addressing time of 30 µs. The erasing sequence is not shown (in order to allow higher magnification).

In the HOE scheme the writing pulse is 2 x 23 = 46 µs wide (in the presented example) whereas in the HOM scheme it has the real duration of 3 x 15 = 45 µs. Thus, the pixel is driven by switching pulses of effectively same size in both cases, but with the HOM scheme we have to spend 30% less time at each display line.

Further extension of the selection sequence does not seem to be possible, because the control window rapidly becomes too short to sufficiently differentiate the on and off areas of the writing pulse. In fact, already the HOM scheme does not work with all cells. For example, the SCE8 cell could be addressed with the original HOE scheme at 40 V selection, 8 V data and 90 µs slot, but no reliable operating conditions for the HOM scheme were found. Thus, if we want to obtain even shorter control windows we have to look for another effect which could be exploited.

7.2 Utilization of Dielectric Biaxiality

As discussed in Chapter 2.3 *Biaxiality of the Dielectric Tensor* (page 7) the difference in the dielectric torques due to the three principal permittivity values (ε_1, ε_2, ε_3) can counteract the switching in its initial phase and accelerate it in the final stage. Figure 43 presents the rate of change of the azimuthal angle ϕ of a C* molecule around the cone ($d\phi/dt$) as a function of ϕ for a set of amplitudes of a positive switching pulse. The plots were obtained from the model described in Chapter *Bistable Switching* (page 15) using equation 22. The simulation parameters correspond to a GEC-SCE8 cell and were derived in Paper IX. The curves in Figure

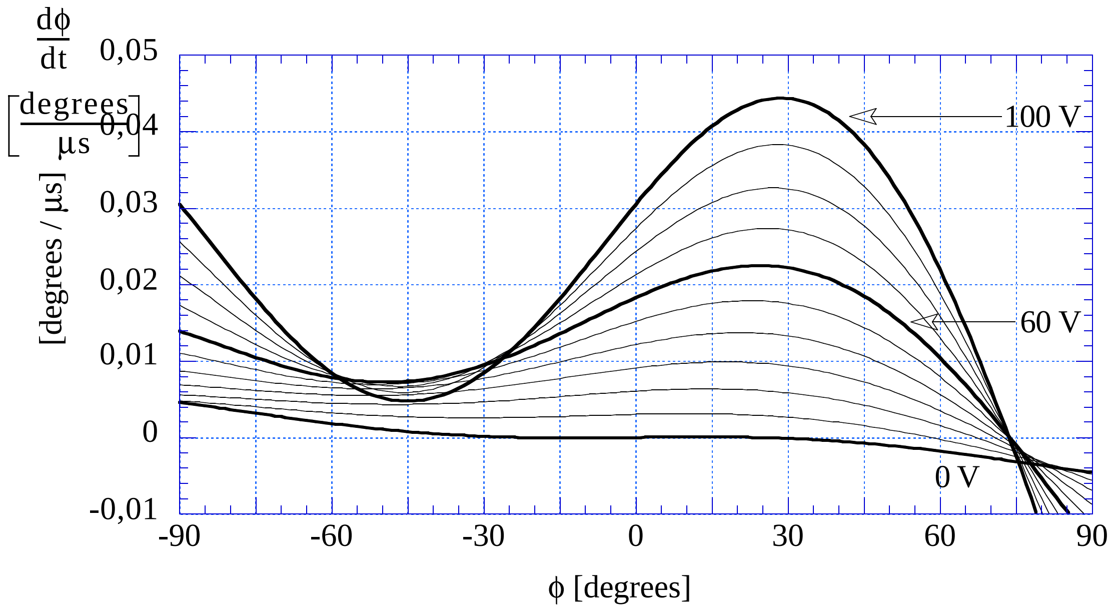


Figure 43. Rate of change of the azimuthal angle φ of a C* molecule around the cone (dφ/dt) as a function of φ for a set of switching pulse amplitudes ranging from 0 V (corresponding to the elastic torque only) to 100 V in steps of 10 V. The curves are obtained from the simulation model (equation 22) using the following parameters derived in Paper IX for a GEC (UK) fabricated SCE8 cell: φ in the relaxed (field off) state ϕ_0=23°, cone angle θ=20.5°, layer leaning angle δ=18°, dielectric biaxiality ∂ε=0.128, dielectric anisotropy Δε=-0.723, spontaneous polarization P_S=4.5nC/cm^{-2}, relaxation time t_R=400µs, viscosity η=678mPas and cell thickness 1.7µm. The reduced simulation parameters are in this case: limit value for φ at infinite voltage ϕ_V=69°, characteristic voltage V_C=26.3V, characteristic time t_C=125µs and voltage linearity range λ=2.56.

43 represent switching from negative values of the angle φ as a response to an applied positive voltage. They are clearly asymmetric and for pulse amplitudes above 60 V the switching is first slowed down (for starting φ in –69° position) and then strongly accelerated toward the opposite fully switched state. It turns out that the value of biaxiality ∂ε is the most important parameter controlling dφ/dt. Hence, if the writing pulse lies near the limit between the switching and non-switching one, increasing or decreasing the dielectric torque during selected parts of the switching process should produce the required difference in the optical response. The strength of the dielectric torque can be controlled by the hf component of the applied waveform. This consideration makes up a base for new, fast addressing modes.

The control window of addressing should be placed where the effect of the dielectric torques is strongest, i.e. near the beginning or end of the switching. In the first case we get an addressing scheme which may properly be called *hold-back mode* and in the second case a scheme which may be called *hold-on mode*. These modes were originally discovered at higher amplitudes of selection waveforms, where the asymmetries in switching slopes caused by dielectric effects are most prominent. They were therefore often referred to as “high voltage” modes,[33,60,68,82,83,97] although they can be utilized also at quite moderate voltage levels.

7.3 The Hold-back Mode

The principle of operation of the hold-back mode (or hampered writing mode according to the nomenclature proposed by Maltese *et al.*)[97] can be illustrated by a simple experiment presented in Figure 44. The addressing waveform is here modelled by a monopolar switching pulse surrounded by a square wave. As can be seen in the upper diagram, this pulse is not able to switch the cell all the way up to the bright state and the optical response falls down to the initial level. By suppressing the square wave, and hence the decelerating dielectric torque, immediately before the switching pulse a clean latching can be accomplished. The switching pulse itself is not changed and the process is controlled solely by the hf component preceding it. Thus, the control window of addressing does not need to include the writing pulse itself, which is a quite surprising conclusion in the light of multiplexing methods discussed so far.

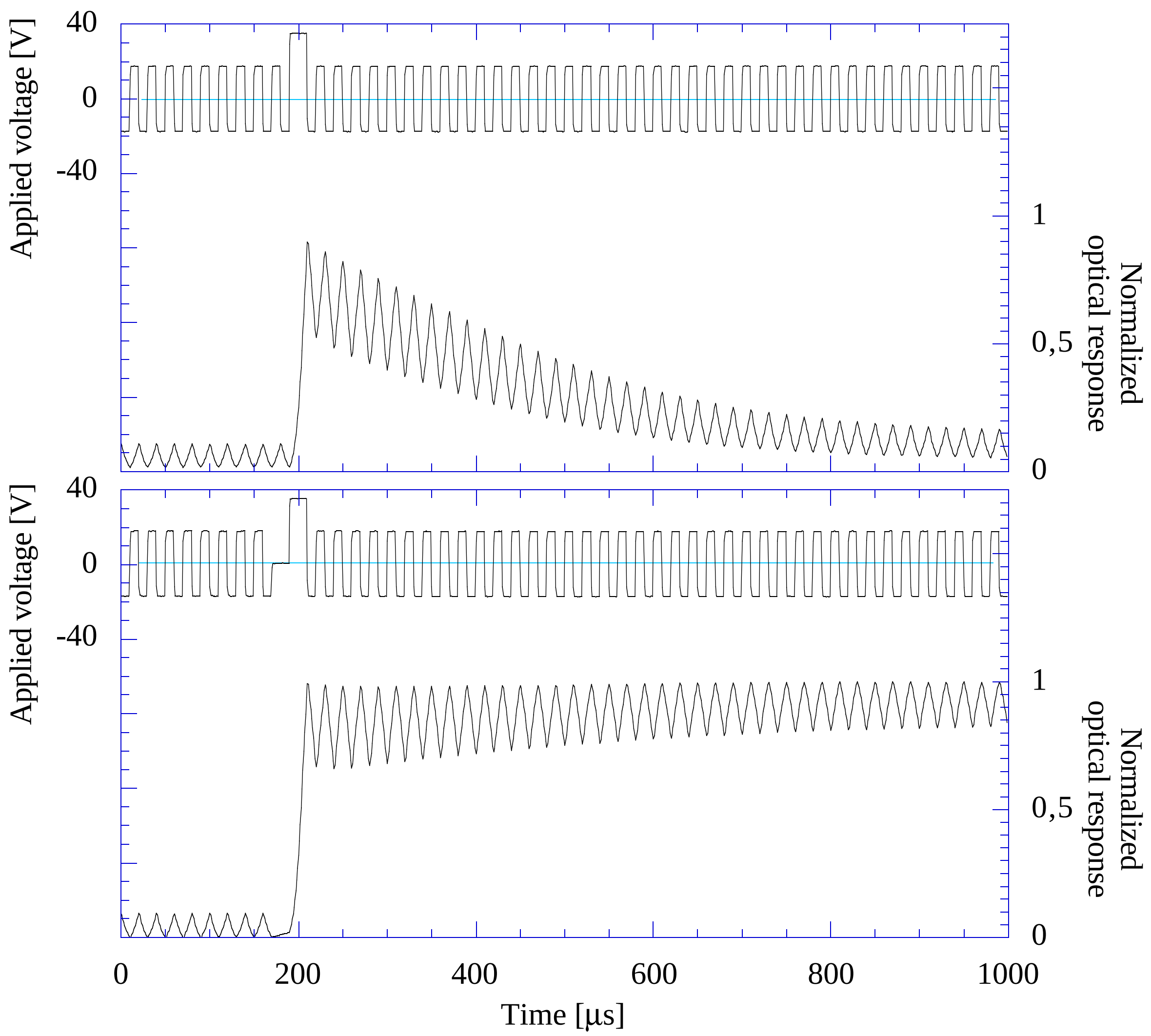


Figure 44. The principle of the hold-back mode – switching is accomplished by suppressing the high frequency component immediately preceding the constant writing pulse. (4655/000 cell, switching pulse 36V/20µs, crosstalk modelled by a square wave 18V/10µs)

This effect can be clearly seen already in the JOERS/Alvey scheme as illustrated in Figure 35. Introducing the time-overlap of the writing pulse into this scheme lead to a family

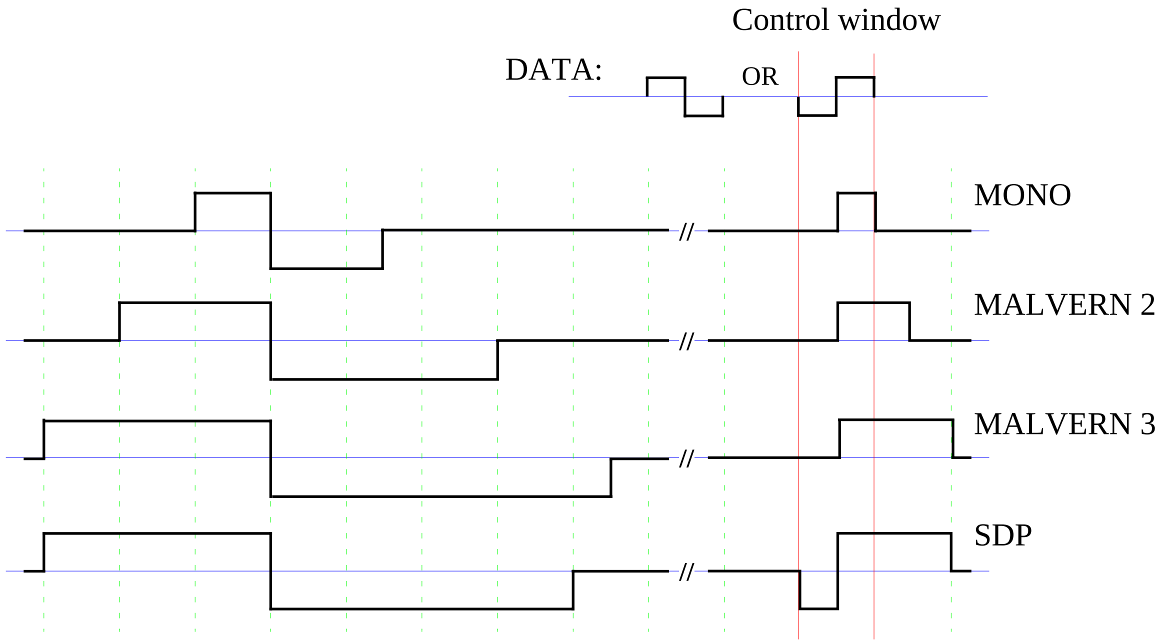


Figure 45. Hold-back mode addressing schemes utilizing conventional data sequences.

of Malvern addressing schemes.[78] In the Malvern 2 scheme the writing pulse is extended over one time slot in the succeeding control window (effective width is then two slots and hence the notation). Consequently, one more slot is appended in the Malvern 3 scheme. Originally[78] these schemes were presented as direct extension of the JOERS/Alvey method and still utilized two subframes with a polarity reversal of the writing pulse. Since the leading pulse is reduced in width from being equal to the switching pulse to a fraction of it, the discrimination between switching and non-switching pulses is reduced. As has been pointed out before, efficient erasing prior to writing would be of advantage. Maltese *et al.* modified the Malvern schemes by introducing a double-erase sequence[33,32] with an additional pause.[84] This technique allows also for direct dc-compensation of the writing pulse. Polarity inversion and two-field addressing can be avoided in this way. McDonnell *et al.*[75] adopted this approach and presented a Monopolar (MONO) addressing scheme, which is a direct combination of the JOERS/Alvey one-slot writing pulse with a blanking sequence. Recently, Maltese *et al.*[95] proposed a “Stay-Down-Pulse” (SDP) addressing scheme, where the hold-back effect within the control window is enhanced. All these schemes are based on conventional data sequences and are

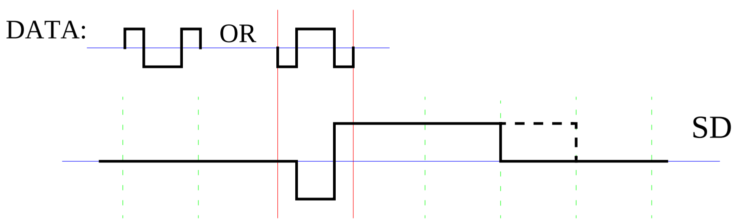


Figure 46. The hold-back addressing scheme (SDS) utilizing crosstalk compensated data sequences. The number of slots overlap with the writing pulse can be adjusted to suit the parameters of the SSFLC cell. The presented selection sequence is dc-compensated against the double erase sequence preceding it (not shown here).

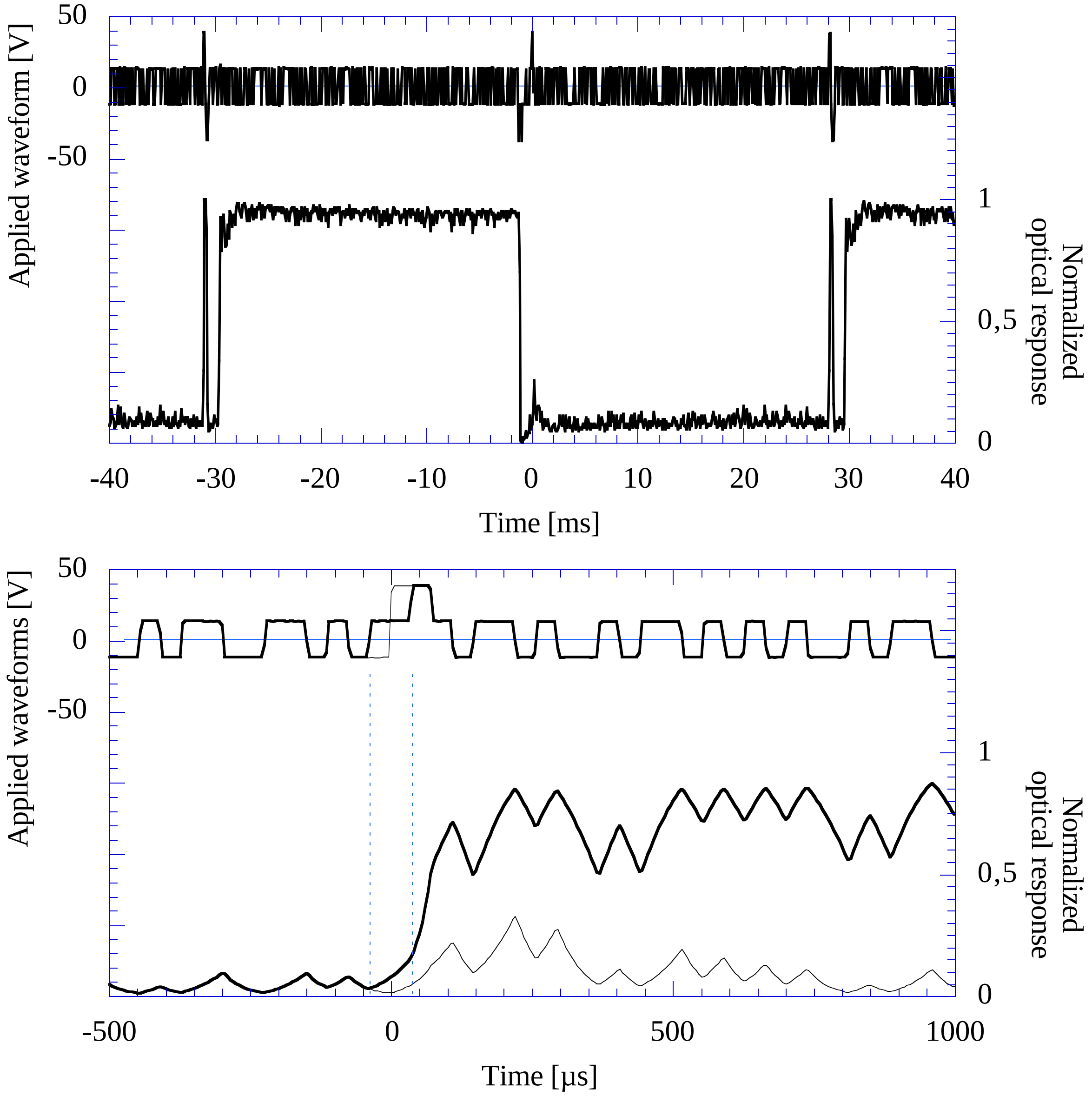


Figure 47. Example of the hold-back mode; the modified Malvern3 addressing scheme applied to the SCE8 cell. Waveform amplitudes are 26 V and 13 V for selection and data, respectively. The slot time is 37 µs (i.e. t_a = 74 µs). The upper diagram presents the optical response of one pixel in a 200-row display switched alternatively between bright and dark states. The lower diagram shows a detailed view in the vicinity of the control window (marked by vertical lines).

schematically presented in Figure 45. The crosstalk compensated data sequences are used in the “Stay-Down-Superfast” (SDS) scheme sketched in Figure 46.

In the schemes where the writing pulse overlaps the entire succeeding control window, its area is not affected by the data that can appear there in either phase. This compensates for the reduced discrimination effect of the data within the proper control window. Consequently, schemes like Malvern 2 and HOE are more sensitive to the data following the control window. This problem is avoided in the schemes based on crosstalk-compensated data sequences.

Figure 47 presents the modified Malvern 3 scheme applied to a test cell filled with Merck

SCE8 liquid crystal. With 26 and 13 volts at rows and columns, respectively, the obtained slot width is 37 µs, which corresponds to 74 µs line addressing time.

At the same conditions (26 V, resp. 13 V) the modified Malvern 2 scheme needs 45 µs slot width (i.e. t_a = 90 µs). The original Malvern schemes require higher amplitude of the selection waveform for correct operation, since without the erasing sequence the initial conditions before the switching pulse are not well-defined. At 50 V for selection and 10 V data (i.e. the same as in the JOERS/Alvey scheme), the Malvern 2 yields a 36 µs slot width, while Malvern 3 gives 29 µs. The effective line addressing time is (due to the two subframes) equal to 144 µs and 116 µs, respectively.

7.4 The Split Writing Mode

Paper X discloses a new family of very fast, hold-back mode addressing schemes where the writing pulse is divided in two parts with an interruption in between. In such a *Split Writing* (SW) scheme the control window overlaps the first writing pulse (or a part of it), the interruption period and the beginning of the second writing pulse. It uses the crosstalk-compensated data waveforms. The selection sequence is presented in Figure 48. Both parts of the writing pulses can be expanded over a number of neighboring control windows to achieve optimum speed and discrimination. Prior to the writing sequence, the pixel is erased twice and driven to its hf-stabilized state, as it has been shown before.

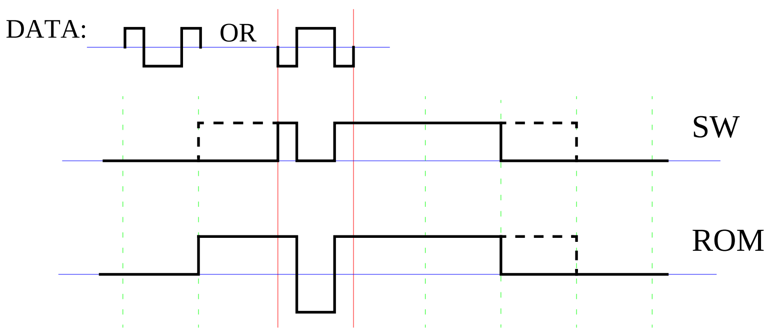


Figure 48. Selection waveforms used in the Split Writing (SW) and Rome (ROM) sets of addressing schemes. The writing pulse is divided in two parts. During the control window in the SW scheme the switching is interrupted and in the ROM scheme – counteracted. The width of the pulses preceding and succeeding the control window has to be adjusted to the parameters of the SSFLC display to achieve optimum performance.

The first writing pulse initiates the switching. During the interruption the switching, depending on the supplied data, is either allowed to continue in a smooth way or counteracted. As can be seen in Figure 49, the dielectric torques generated during the control window differ significantly in both cases. The switching continues during the second writing pulse, but if it was counteracted on the way, it cannot reach a level from which it could be completed by the dielectric action of crosstalk pulses and is instead forced back by the same action to the original state. In the example presented in Figure 49, the SW scheme is applied to a CTH fabricated cell filled with Merck SCE8 liquid crystal. With moderate amplitudes of selection and data waveforms (26 V and 12 V, respectively) the line addressing time in a simulated 800-row display is 44 µs. This should be compared with the approximately 100 µs switching time of this cell in response to a monopolar pulse (and 300 µs in the case of a bipolar pulse), as shown in Figure 18 on page 23.

Increasing the amplitudes of the driving waveforms to 50 V and 10 V, respectively, does not change the operating speed but improves the discrimination between bright and dark switching traces, as shown in Figure 50. Extending the trailing part of the writing pulses to overlap three control windows allows only for a slight reduction of the slot time to 10 µs. Extension of the leading part of the writing pulse was not found advantageous in the case of the SCE8-cell.

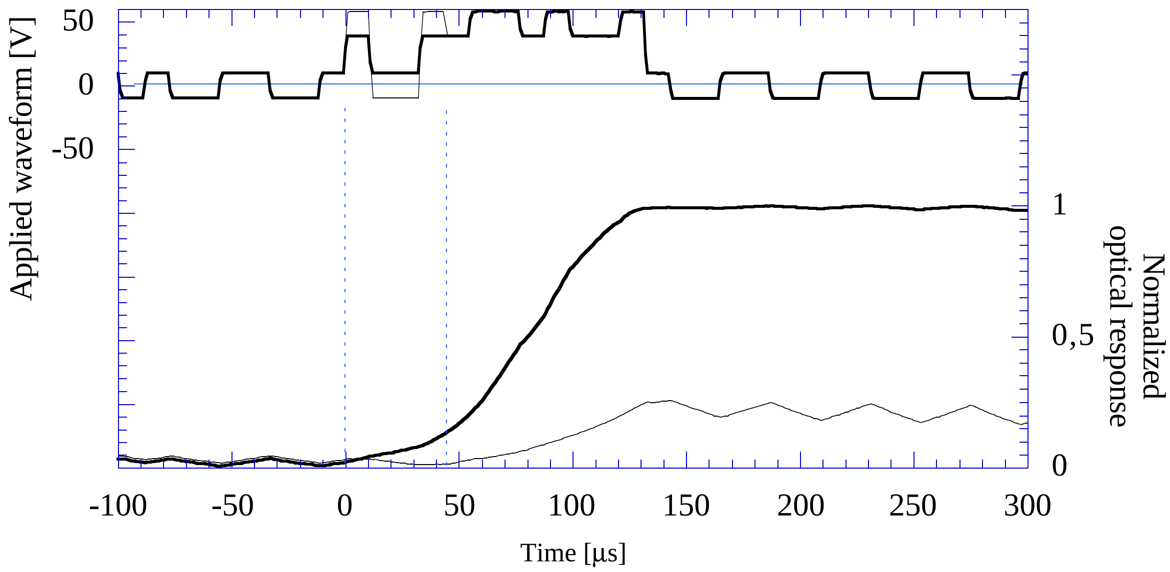


Figure 50. Discrimination between switching and non-switching data is increased when the Split Writing scheme operates at higher amplitude of the selection waveform (compare with bottom diagram in Figure 49). Driving voltages are here 50 V and 10 V for selection and data, respectively. The slot time is 11 µs.

Stronger dielectric interaction is utilized in the “Rome” set of addressing schemes (ROM)[93] also shown in Figure 48. The switching is initiated equally for both possible data waveforms and then interrupted by a sequence containing a pulse of opposite polarity. The switching trace falls toward the initial level by an amount depending on the size of the “call-back” pulse, which is defined by the data within the control window. Afterwards the switching is resumed, but due to significant difference in the new “initial” state it can either be completed or fall back to the erased state. As opposed to the SW scheme, this mode utilizes an additional effect of the reversed ferroelectric torque to make the switching interruption more effective, which can be seen in Figure 51. In order to provide room for this effect, the leading part of the writing pulses has to be extended. On the SCE8-cell the ROM scheme was found to operate at the same conditions as the Split Writing scheme.

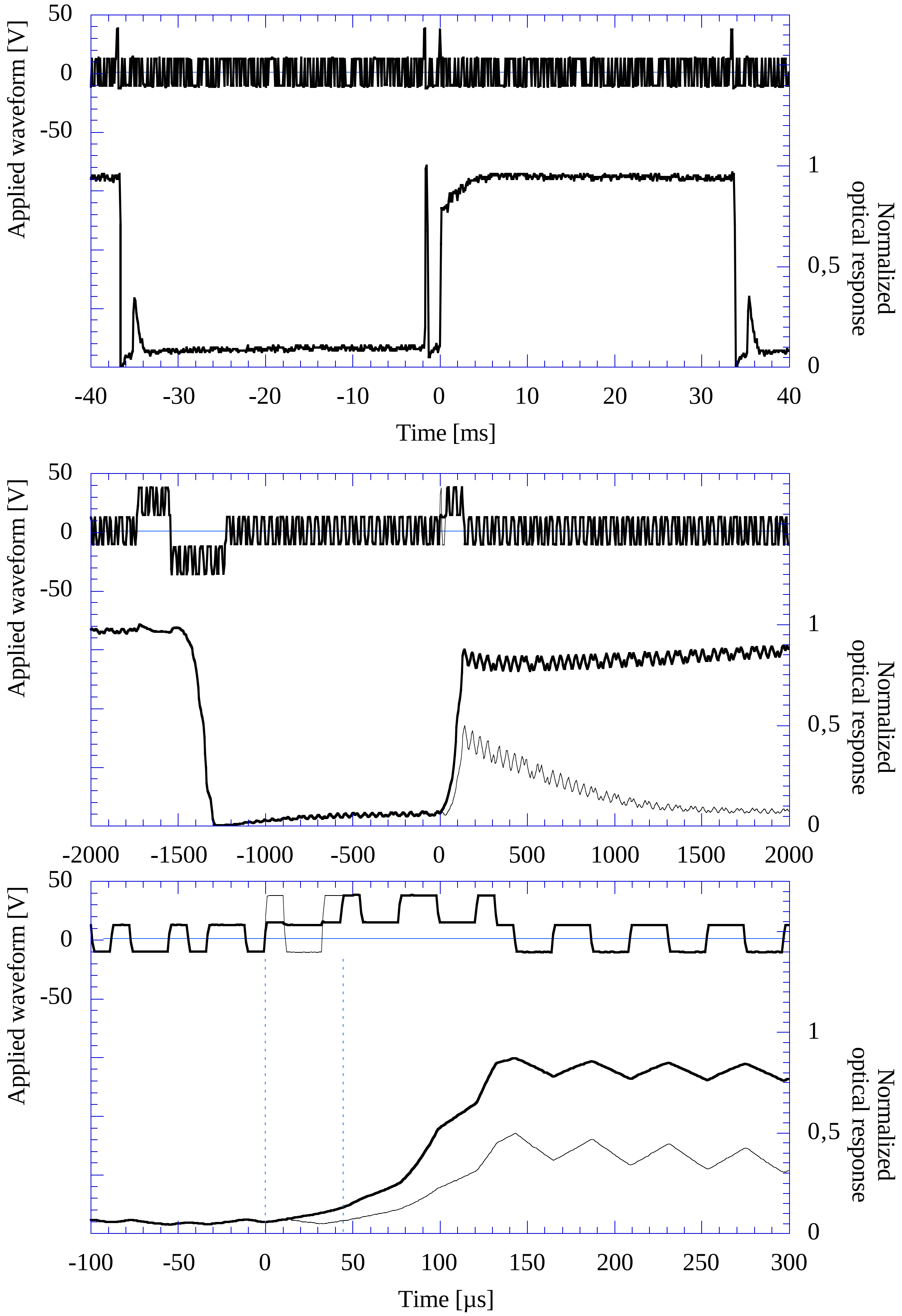


Figure 49. The Split Writing (SW) addressing scheme applied to the SCE8-filled cell. The top diagram presents the electro-optic response of one pixel in an 800-row display. Below – the control window of addressing in increasing magnification. Amplitudes of selection and data waveforms are 26 V and 12 V, respectively. The time slot is 11 µs, which corresponds to 44 µs line addressing.

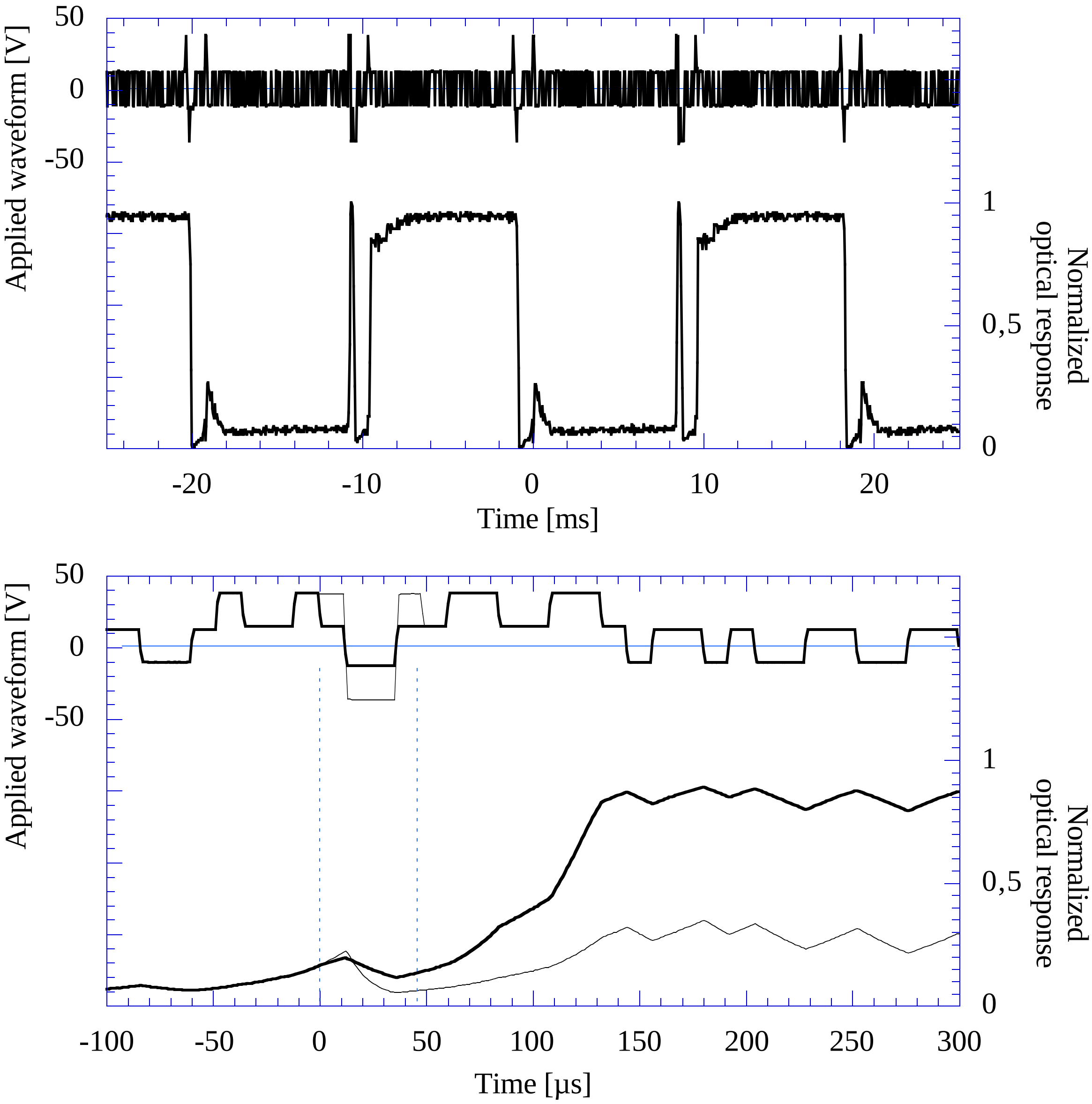


Figure 51. The ROM addressing scheme operating in the same conditions as SW in Figure 49 (SCE8-cell, 26 V selection, 12 V data, 11 µs slot). The writing pulse overlaps four time slots before and eight slots after the control window. Switching is counteracted by a negative pulse, the amplitude of which is defined by the data within the control window.

7.5 The Hold-on Mode

The hold-on mode (or stopped writing mode according to the nomenclature proposed by Maltese *et al.*)[97] relies on the effect of high frequency field in the proximity of the final stage of the switching. To illustrate this let us make a simple experiment and apply the test waveform to the SCE8-cell. This waveform, as described in Chapter 10.5 *Test Waveforms* (page 98), consists of a dc-compensated three-pulse switching sequence followed by an hf field. The three pulses play here the role of erase, write and stop pulse, respectively. The amplitude is set to 30 volts and the durations are adjusted so that the stop pulse is able to invert the optical state imposed by the writing pulse. This situation is plotted with thicker lines in Figure 52. We now superpose a short hf-burst over the end of the writing pulse and the beginning of the stop pulse, as drawn by thin lines in the same figure. The induced dielectric torque presses the liquid crystal director toward the written state and the stop pulse cannot switch it back. Hence, the resulting optical state of the pixel can be controlled by the strength of the hf field within the time window positioned as in the presented experiment.

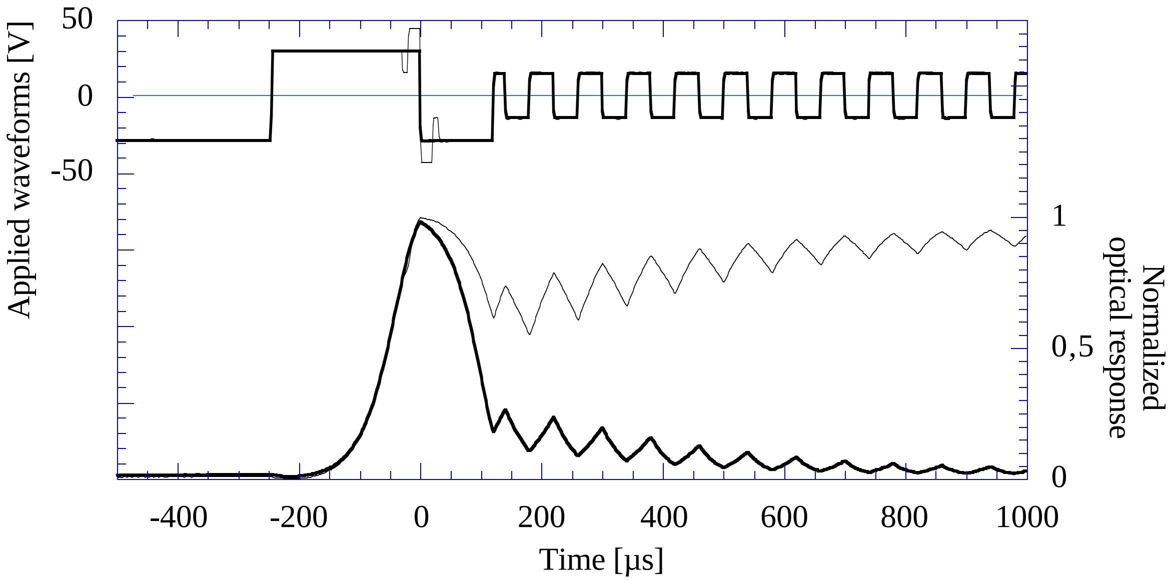


Figure 52. Experiment showing the principle of the hold-on mode – the final optical state of the pixel is controlled by the strength of a hf field applied in the time window covering the end of the writing pulse and the beginning of the stop pulse. (SCE8-cell at 25°C)

The “4631” scheme shown in Chapter 5.5 *Time Overlap of Selection Waveforms* (page 34) can be adapted to operate in the hold-on mode simply by increasing its amplitude and frequency, as proposed by Maltese *et al*.[84] In this case the last erase pulse takes over the role of the writing pulse, while the old writing pulse becomes a stop pulse. The contrast is increased due to suppressed oscillations. It is also inverted, since the meaning of the data sequences changes. Figure 53 presents the F4631 (Fast Four-Six-Three-One) scheme applied to an SSFLC cell filled with Merck 4655/000 mixture. The line addressing time is 25 μs at quite moderate amplitudes of the applied waveforms (36 V and 18 V for selection and data, respectively). The upper diagram presents the light transmission through a pixel in a frame scale, while the two diagrams below show the control window of addressing in high magnification. To simplify comparison the data differs only within the control window. As can be seen in both plots, the switching to the opposite state occurs when a writing pulse of slightly bigger area is followed by a high amplitude, short counter pulse (stop pulse). The traces of the optical response within the control window resembles the bipolar pulse switching utilizing the effect of leading pulse latching, but starting from some intermediate level produced by a part of the writing pulse preceding the control window.

The F4631 scheme uses conventional data sequences. Crosstalk compensated data waveforms are instead used in the “Pause-Superfast” (PS) family of addressing schemes[82,83]

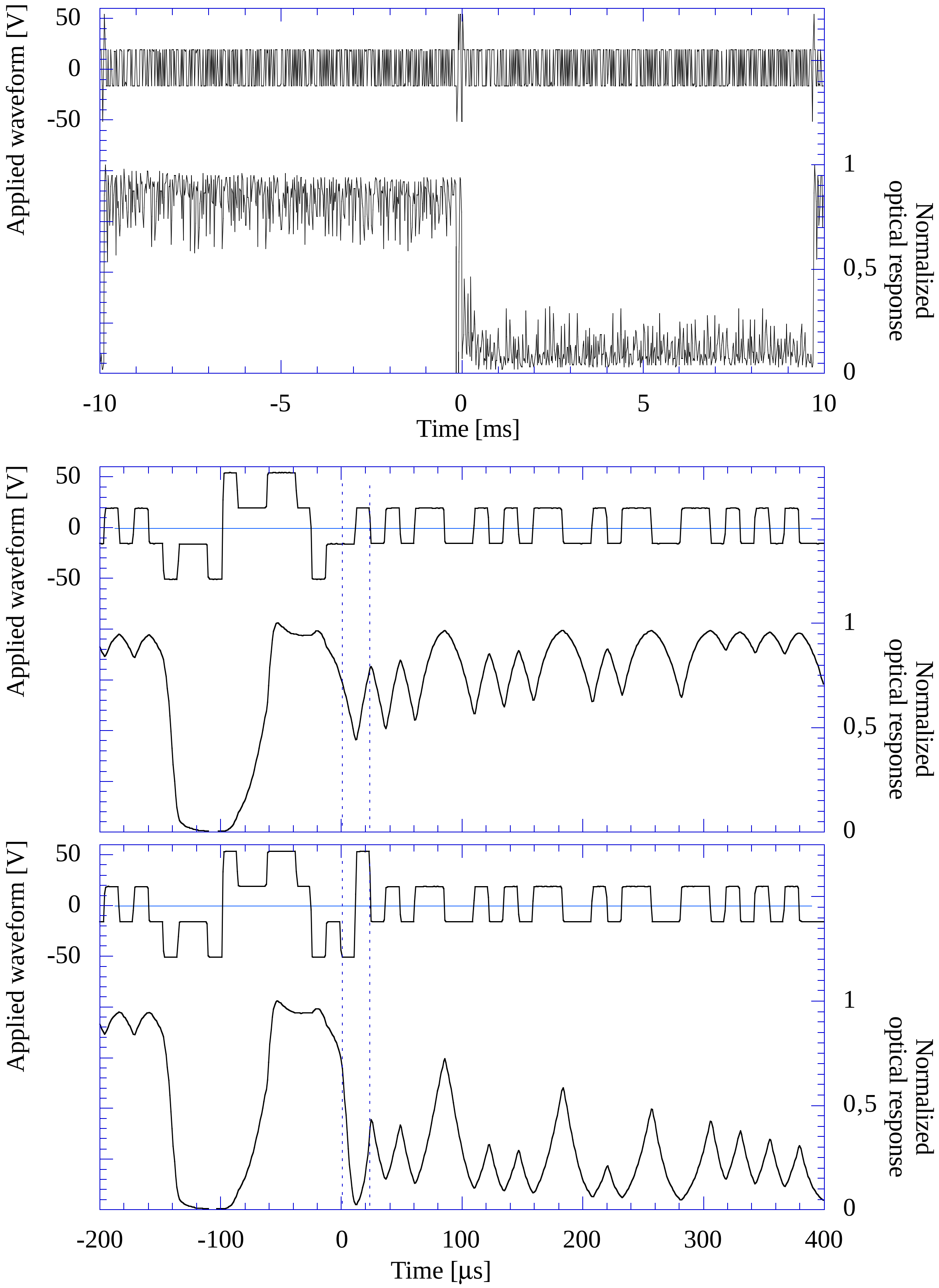


Figure 53. F4631 addressing scheme applied to the 4655/000 cell at room temperature. The line addressing time is 25 µs and the selection and data amplitudes are 36 V and 18 V, respectively. The upper diagram presents the optical response of one pixel in a 400-row display, while its magnified parts corresponding to switching into bright and dark states are shown below. To simplify comparison, the data differ only within the control window (between the dotted lines).

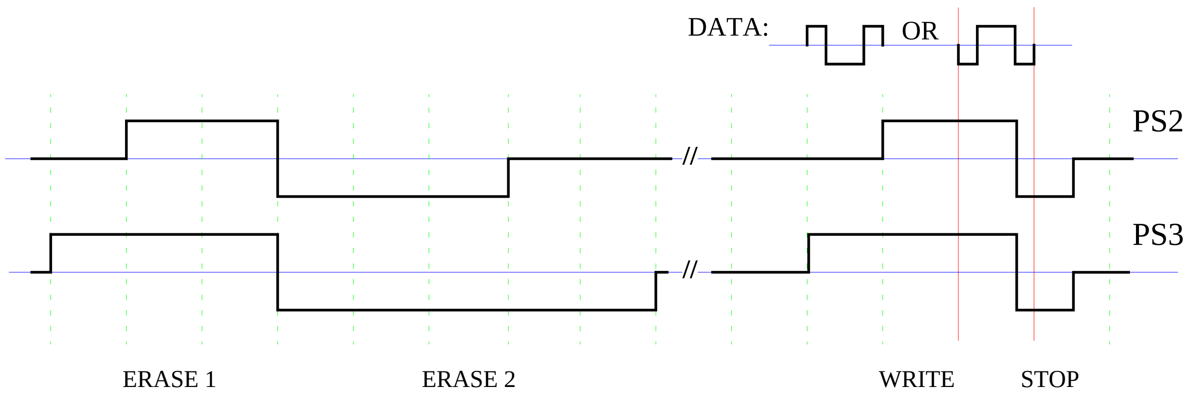


Figure 54. Selection waveforms of PS2 and PS3 addressing schemes operating in the hold-on mode and using crosstalk compensated data sequences. Prior to writing, the pixel is erased twice in opposite directions and allowed to relax to the hf field stabilized state. The control window spans over the end of the writing pulse and the beginning of the stop pulse.

sketched in Figure 40. The two erase pulses are here separated from the writing sequence by a pause, during which the liquid crystal director is driven to the field-stabilized state (as discussed before). The duration of this pause has to be adjusted to the cell properties, so that the initial state just before the writing pulse is the same and independent on the previous state of the pixel. PS2 and PS3 schemes differ in the size of the writing pulse – it spans over two or three control windows. This directly indicates that the PS3 is faster than PS2, since the absolute duration of the writing pulse is nearly constant for a given amplitude of the applied voltage. Figure 55 show the operation of the PS3 scheme.

7.6 General Classification of Addressing Modes

Figure 56 summarizes the essential features of the “normal”, hold-back and hold-on modes. According to the proposed classification,[97, Paper X] the “normal” addressing mode is characterized by writing from a saturated (fully switched) state; the pixel is first fully driven into one state and then switched toward the opposite state by a writing pulse. The area of the writing pulse is controlled by data sequence supplied within the control window. In both hold-back and hold-on modes a major part of the writing pulse is outside the control window.

The control window in the hold-back mode is placed in front of the writing pulse and acts on the switching process in the initial stage. If the generated hf component is strong, the switching is initially hindered, and if it is weak – the state of the pixel is not altered significantly and the switching process starts with the arrival of the writing pulse.

The hold-on mode exploits the dielectric effects in the final stage of switching. Here, the strong dielectric torque overrules the ferroelectric one and forces the liquid crystal director toward the nearest hf-stabilized state.

Using the same convention, the Split Writing technique can be presented as in Figure 57a. Here, the switching is initiated a short time before the hf field is applied.

Obviously, it is possible to combine the two fast addressing modes. Figure 57b shows a

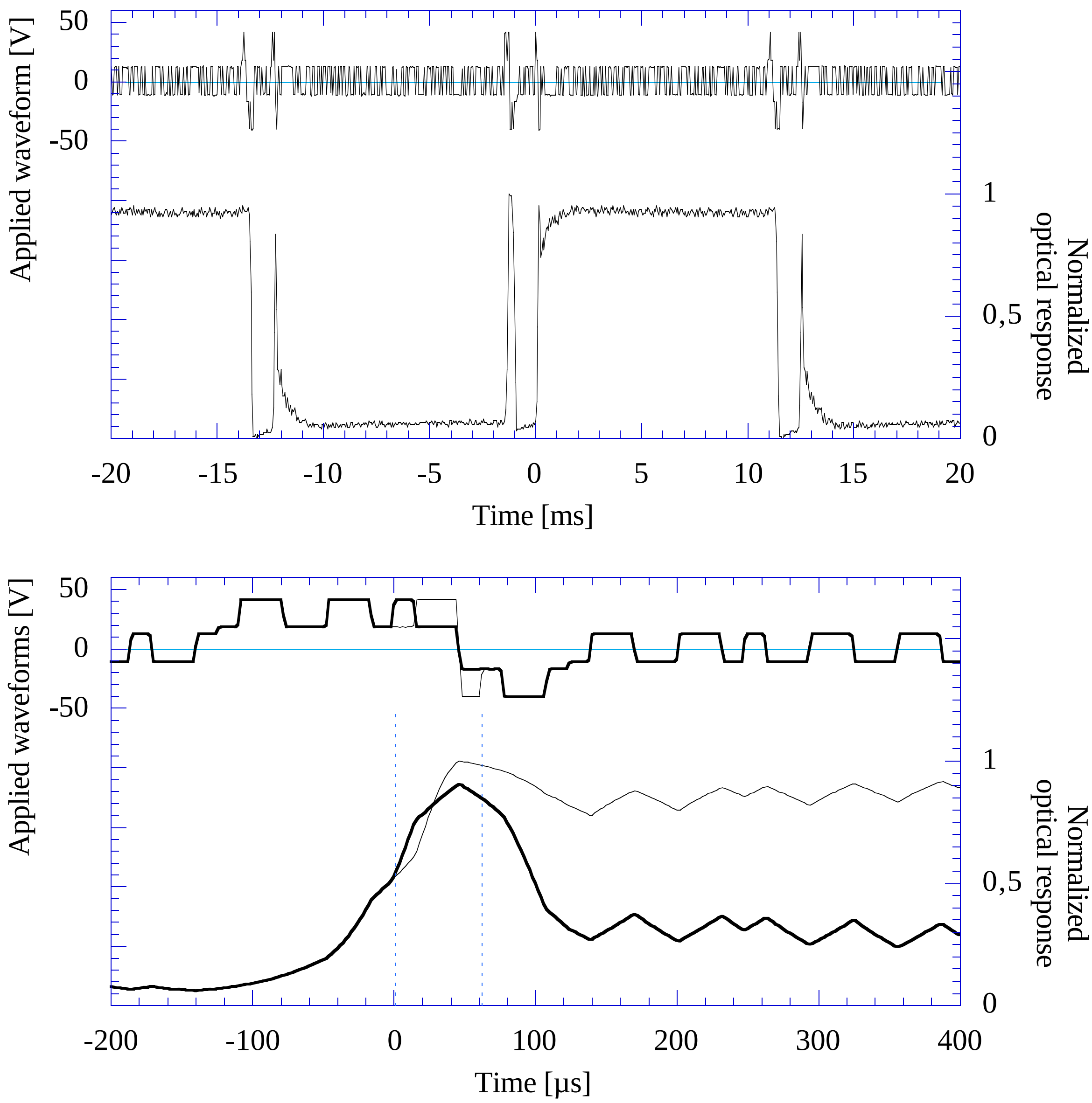


Figure 55. The PS3 addressing scheme (hold-on mode) applied at room temperature to the SCE8 ferroelectric liquid crystal cell. The achieved line addressing time is 62 µs. The amplitudes of the selection and data waveforms are 26 V and 12 V, respectively. The vertical dotted lines show the position of the control window.

mixed mode, where the control window is split in two parts. The first one causes the hold-back effect in the initial stage of switching and the other causes the acceleration effect in its final phase. Both control sub-windows are much shorter in this case and very fast addressing has been recently reported[93] using this method.

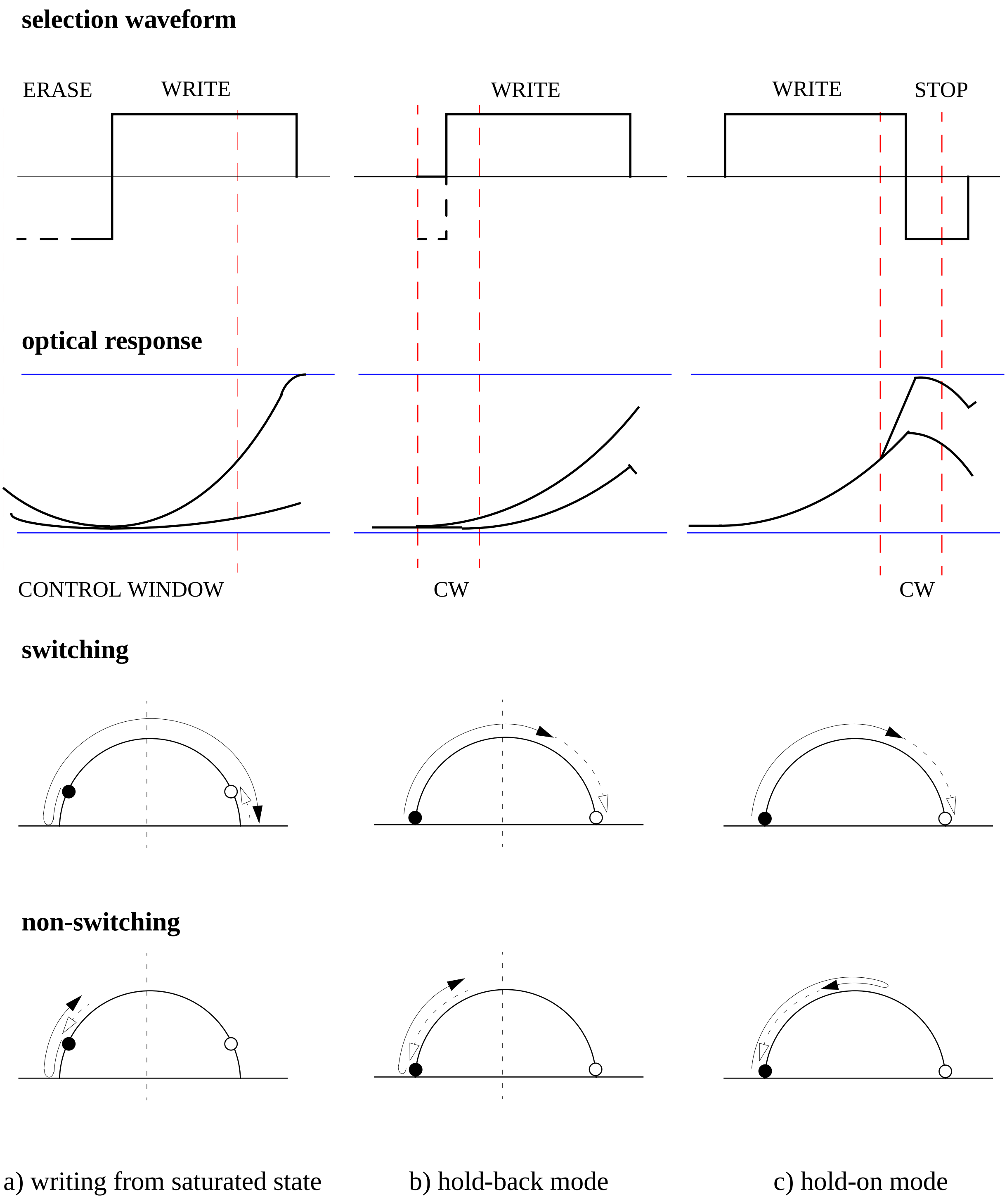


Figure 56. Proposed classification and essential features of addressing modes. The two traces in the optical response correspond to the effect of the data applied during the control window (CW) and are drawn for the simplest case of bipolar (conventional) data sequences. Data pulses are not shown. The movement of the molecule around the cone is sketched in the lower part of the figure. Switching is illustrated by the arrows going from black to white circles, non-switching from black to black. The switching is completed by the action of the crosstalk pulses as shown by broken lines.

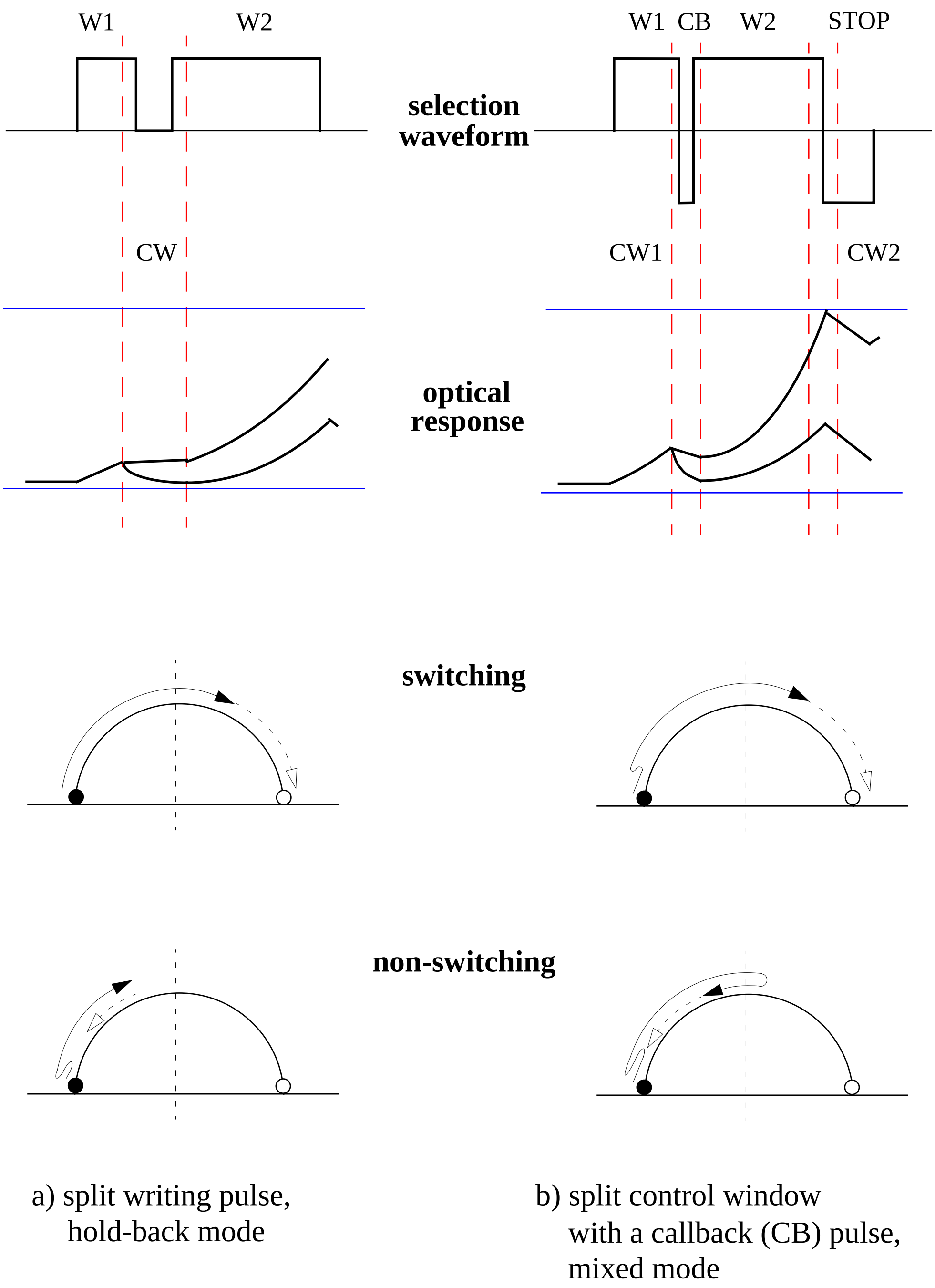


Figure 57. Schematic representation of the hold-back, split writing pulse addressing mode (a) and a mixed mode, in which the control window is split in parts and affects the switching both in the initial and in the final stage (b).

8 GENERATION OF GREY SHADES

8.1 Number of Light Transmission Levels

The bistability in the SSFLC naturally favors generating black and white images. On the other hand, a good reproduction of halftone images demands grey shades. Obviously, the required number of grey levels depends on the specific application and on the resolution of the display panel. Simple graphics can be done with as few as 8 shades, and 64 are quite sufficient for a color TV.[59] The human eye can, however, distinguish more than a hundred tones. Therefore, in a good quality picture reproduction, 128 grey levels is considered a minimum, and 256 is a common value in computer applications. These numbers relate to the standard resolution of today's displays, which is quite low. The SSFLC technique gives prospects of very high resolution screens, where photographic quality pictures can be displayed using only a few shades.

It is also clear that the stated amounts of grey levels (8, 16, 32, 64, 128, 256 etc.) are derived from the number of data bits required to describe the optic state of each pixel and the complexity of the video-driver circuit. They have nothing to do with the physics of liquid crystals displays and are accepted solely to suit the driving electronics.

Equally spaced light transmission levels are quite straightforward to generate and are therefore used in most of the grey-shade displays demonstrated so far. On the other hand the perception of the human eye is logarithmic. Hence, logarithmically spaced grey shades would be more appropriate.

Generally, the methods of creating grey scale can be categorized as *digital* and *analog* techniques.[16,40]

8.2 Digital Techniques

The digital techniques are straightforward for bistable cells because each pixel is in either a black or white state. The impression of a grey shade is generated in the observer's eye by integration in time and space - of so called *temporal* and *spatial dither.*

In the temporal dither technique, the grey appearance of a pixel is achieved by subsequent switching it on and off with a certain duty ratio. This method relies on a very fast

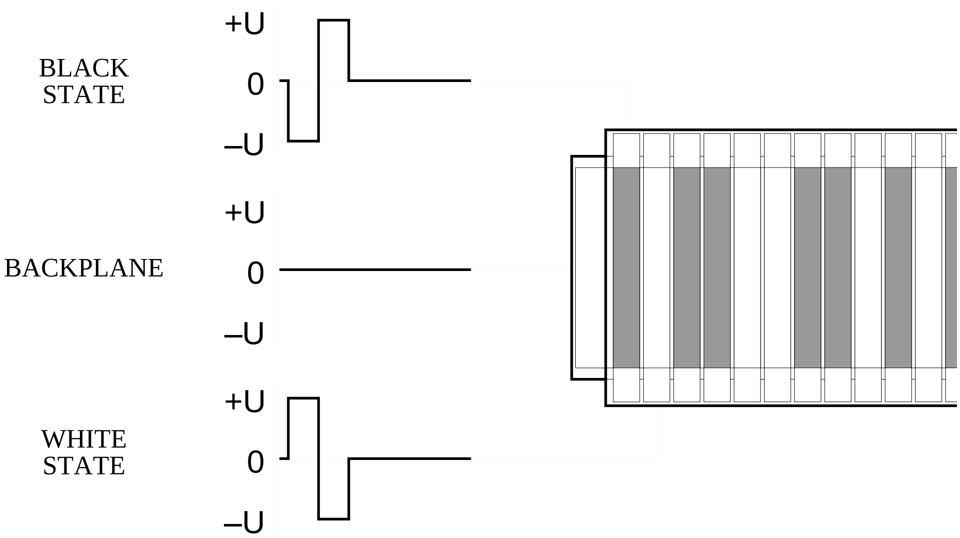


Figure 58. A dynamic pattern of eight grey shades has been demonstrated on an SSFLC linear array using purely temporal dither technique (Paper III). All electrode stripes were directly driven by waveforms consisting of bipolar pulses separated by a pause.

switching, but does not require any special cell preparation nor extended number of electrical connections.

A grey scale generated by temporal dither was shown on an SSFLC display for the first time during the 1st Ferroelectric Liquid Crystal Conference (Arcachon, 1987) and is described in Paper III. A linear array of 96 bars, driven by a double-pulse waveform was used (Figure 58). The switching pulse width was about 50 μs at 9 Volts and the delay time between subsequent addressing was set to 1 ms. The pattern showing 8 grey shades was moving back and forth through the display area at a speed of about 50 lines per second.

Producing a grey scale on large screens based purely on temporal dither is hardly possible as it would require an unrealistic switching speed. An alternative is the spatial dither technique. Here the electrodes are split to achieve subpixel patterning of a size below the human eye's spatial resolution in the same way as used for a conventional CRT’s production of color by using red, green and blue subpixels. Splitting rows would double the frame time, because the SSFLC matrix is scanned a line at the time. Therefore, it is better to divide the columns. This increases the number of connections and driver circuits, which is easier to cope with.

Figure 59a shows a simple dither obtained by unsymmetrical cut of the columns in the ratio one to three. By time division into two subframes (temporal dither), it is possible to obtain nine equally spaced grey levels, as shown in Figure 59b. This technique was used by LETI in their demonstration of the first black and white TV display.[31] Generally, this approach is based on successive subdividing the pixel areas in proportion 1:(f+1), where f is the number of sub-frames. With N subpixels one can obtain $(f+1)^N$ equidistant grey levels.

Splitting the column electrodes in two parts and using two frames gives $(2+1)^2=9$ levels.

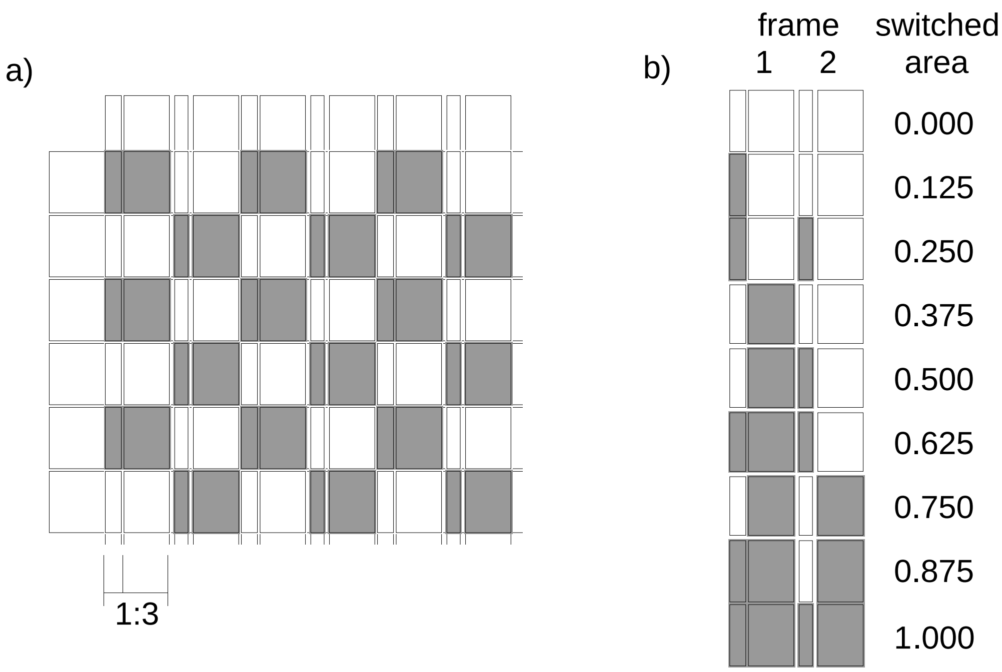


Figure 59. Example of electrode pattern for digital grey scale.
a) Spatial dither achieved by unsymmetrical division of the column electrodes. The area ratio is 1:3.
b) Nine possible grey levels obtained by the combination of spatial dither (two column stripes) and temporal dither (two scans).
This technique was first used in the LETI video display.[40]

By dividing also the row electrodes we get four subpixels and, consequently, $(2+1)^4=81$ grey shades. This simple example shows that both digital techniques should be used together to reduce their mutual disadvantages and gain an optimal performance.

8.3 Analog Techniques

Grey shades can be also created by varying the transparency of the pixel area in a continuous or quasi-continuous way, for example by the use of special addressing waveforms. The technique is based on the ability of an SSFLC cell to memorize intermediate pixel states, which usually are mixtures of just two kinds of uniform domains.[68]

Paper V describes an experiment on the generation of analog grey shades. The selection waveform[32] consists of the *compensate* (2τ), *erase* (3τ) and *write* (1τ) pulses (Figure 60). A hf field is used for stabilization between addressing. The grey shades are controlled using a phase modulation to manipulate the area of the writing pulse. The position of the negative pulse in the data sequence is shifted within the control window of addressing. While retaining the dc balance, its superposition with the selection sequence produces different writing pulse areas.

Since the dedicated instrument described in Chapter *The Waveform Generator* (page 77) was not yet constructed, the driving waveform was tested using a Krone-Hite Arbitrary Waveform Generator (AWG). The AWG was a single channel device and the measurements could only be performed on one pixel at a time. Because of the very troublesome, manual program-

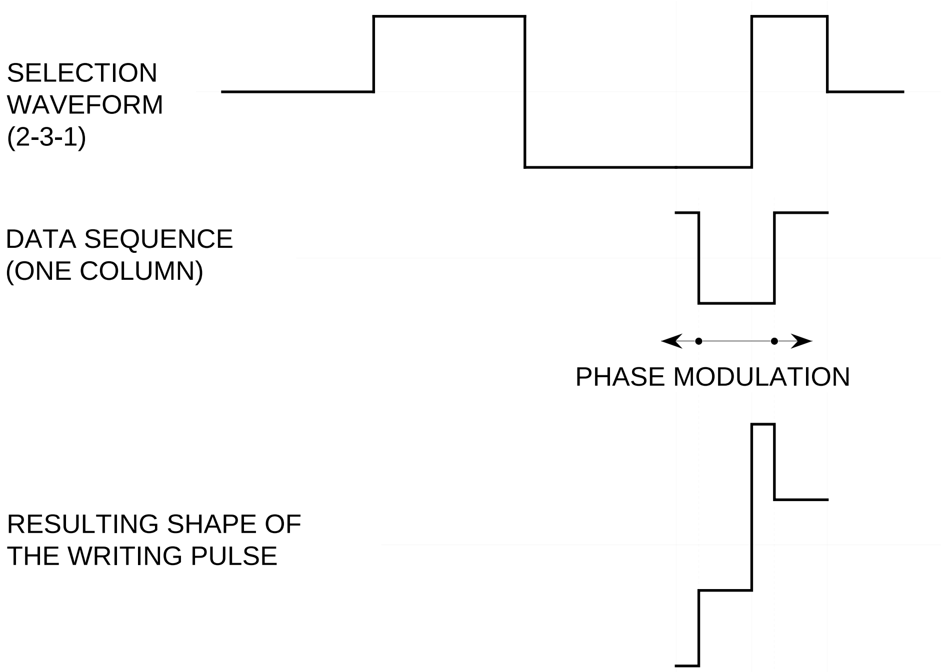


Figure 60. Addressing waveform for analog generation of the grey scale. The area of the writing pulse is controlled by the phase modulation of data sequence (i.e. the position of the negative data-pulse is varied within the limits of line addressing time).

ming procedure of this instrument, the data waveform between selection sequences had to be replaced by a simple square wave obtained from a function generator. It was not possible to synchronize the two parts of the waveform and the frequency of the square wave had to be set unrealistically high. Moreover, the interaction between data pulses and the part of the selection sequence outside the control window (i.e. the compensate pulse and the first 2τ of the erase pulse) had to be neglected.

Figure 61 shows the driving waveform used in the experiment. It was possible to generate sixteen equidistant shades, but each step corresponded to only 1% change of the writing pulse area (see Figure 5 in Paper V). The operating range was thus too narrow for

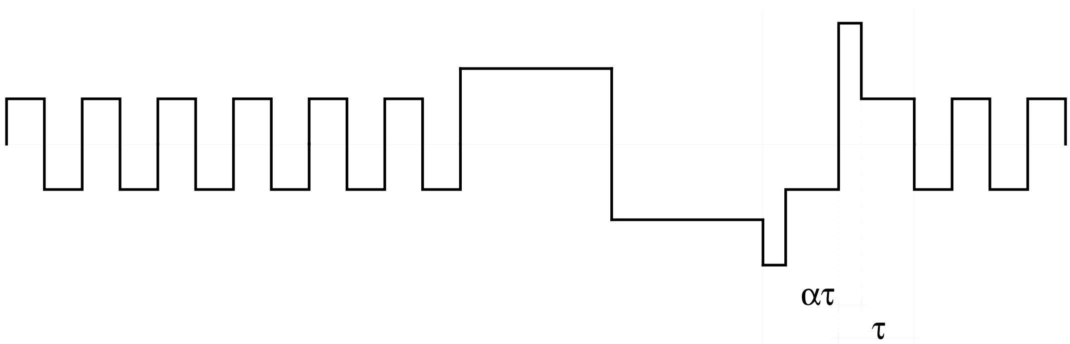


Figure 61. Synthesized driving waveform used in analog grey scale experiments presented in Paper V. Data pulses outside the selection are replaced by a simple square wave.

practical use. This was attributed to the inadequate characteristics of the cell. The experiment showed that the nucleation and growth of the domains is not reproducible to the required extend and additional control of this process is necessary. Such control can be achieved by:

- local threshold variation,
- local electric field variation,
- control of the amount of charge injected to each pixel.

8.4 Local Threshold Variation

Using certain preparation methods[28,50] it is possible to break down the SSFLC structure into a multidomain texture of a fairly homogeneous domain size. Such a texture exhibits excellent bistability due to the strong adhering of the defect lines at the boundaries. The threshold varies stochastically over the surface on the 1 μm to 10 μm scale and allows switching smaller or larger number of domains within each pixel.

This approach allowed the demonstration of grey shades on a 2.5" diagonal, 140 rows by 170 columns, video SSFLC screen by Hartmann *et al*.[54] The required texture of the liquid crystal was obtained by treating the cell (after filling it in isotropic phase and slowly cooling down to room temperature) with a 25 Hz square wave at a stepwise increasing amplitude. The treatment causes irreversible reorientation of the smectic layer structure. First, the needle-like zigzag defects are shrunk, then the texture changes through a roof-type to a rather homogeneous striped texture (*texture method*[50]). The required uniformity of the cell thickness (1.4 μm) was assured by high concentration of quartz spacer beads (ca. 1800 per mm^2). The addressing waveform was analogous to the one presented in Figure 60, but instead of the phase shift, amplitude modulation of data sequences was used.

An interesting method of threshold variation was proposed by Sony researchers. They dissolved small amount of nanometer-scale particles (carbon black and titanium dioxide) in the ferroelectric liquid crystal.[89] The paper reports broadening of the threshold curve that could be controlled by the distribution of the particle size.

8.5 Local Electric Field Variation

Since the analog grey scale generation is so sensitive to non-uniformities one may turn the problem the other way around and use this property to an advantage. By introducing the non-uniformities in a controlled way, discrete steps in the threshold curve may be created.

The *multi-gap* technology,[21] introduced by Canon, is based on randomly varying the cell thickness, obtained by the roughness (in the order of 0.15 μm) of the glass surfaces. Unfortunately, this aggravates the alignment problems and so far has not been successfully pursued. Another approach proposed by Canon is based on the inclined row electrodes,[69,87] as shown in Figure 62. The cell thickness varies in a well-controlled way within each pixel and hence the electric field felt by the liquid crystal molecules.

Various methods of voltage division may also be used to control the electric field in different parts of the pixel. Canon's concept was to make selection electrodes from a highly

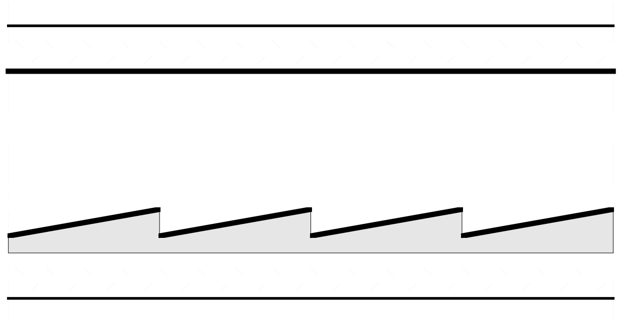


Figure 62. Electric field variation by inclination of scanning electrodes (cross section).

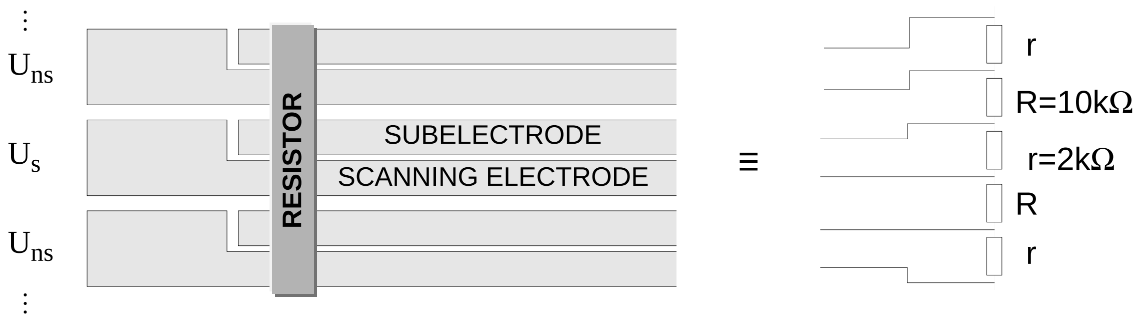


Figure 63. Voltage division created by printing a resistor across all scanning electrodes. Additional sub-electrodes do not have external connections. During selection the voltage on this electrode is equal to $(R\ U_s + r\ U_{ns}) / (R + r)$.

resistive ITO and to place metal stripes lengthwise on both sides of each electrode (Figure 64).

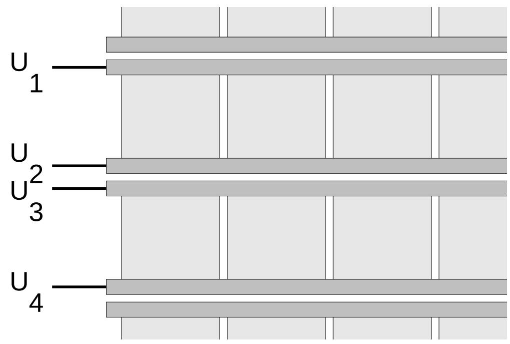
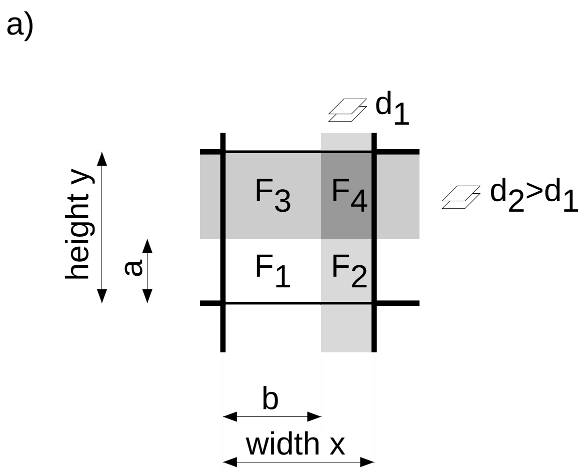


Figure 64. Potential gradient across the selection electrode achieved by the use of highly resistive ITO and metal stripes on both sides of each electrode.

In such a way a voltage drop across the ITO can be achieved. A direct disadvantage of this method is the power loss on the electrodes which may lead to an undesirable heating of the cell.

Matsushita proposed a simpler solution. Each scanning electrode is divided lengthwise in two parts. One part is connected in the usual way to an external electronic driver. The other subelectrode is instead connected with neighboring scanning electrodes through resistors that are created by depositing a resistance paste across all electrodes by screen printing and then baking it. The subelectrode is thus in the mid-point of a voltage divider. The division ratio is defined by the geometry of the electrode pattern, as sketched in Figure 63. By varying the amplitude of the writing pulse three levels of light transmission (bright, grey and dark) can be obtained. A capacitive voltage divider can also be used in this method.

A different way of introducing well-defined threshold steps into the cell is described in Paper V. As shown in Figure 65a, a thin dielectric layer (SiO_2) is deposited lengthwise on the electrodes covering a part of their surface. This increases the threshold in the coated area, because the field within liquid crystal is lowered (assuming that the dielectric layer has a smaller dielectric constant than the liquid crystal). In the experimental 2 μm thick cell, a layer of 210 nm SiO_2 increased the critical pulse amplitude by 23%. We evaporated dielectric layer stripes both on the row and column electrodes. Moreover, the dielectric layer deposited on the row electrodes was thicker than the one on the columns. Such a geometry has four areas ($F_1 \ldots F_4$) of distinct size and threshold, and yields five light transmission levels, when varying the $V\tau$ product of the switching pulse.



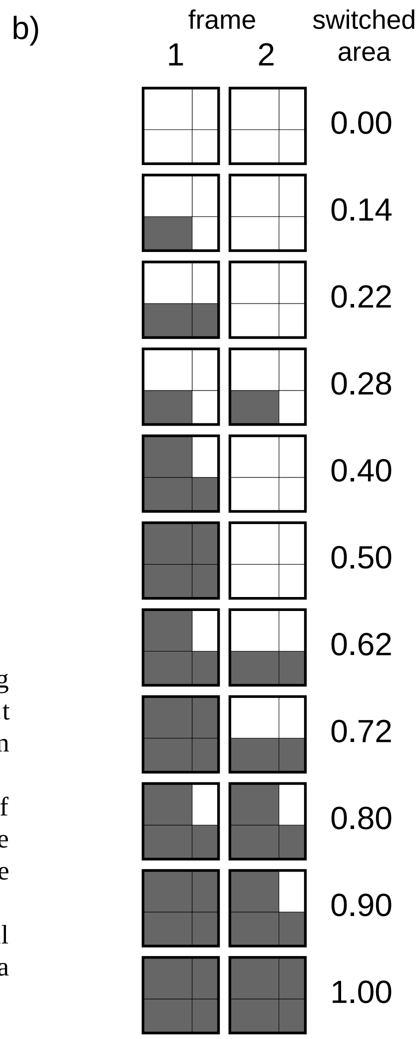


Figure 65. Generation of a grey scale by analog addressing of the pixel with four sub-areas of distinct thresholds (according to the experiment presented in Paper V).
a) The pixel structure with additional dielectric layer of thickness d1 evaporated on a part of the column electrode and a d2 layer on the row electrode. The division factors are here a = 0.432 and b = 0.652.
b) Eleven grey shades obtained using two scans (temporal dither). The switched area is relative, assuming "1" as a fully switched pixel during both frames.

This approach creates a spatial dither (discussed in the previous paragraph) in an analog way and, naturally, can be combined with the temporal dither technique. In the presented experiment, we obtained 11 equidistant light transmission levels using two scans (Figure 65b). The electrode area division factors were equal to a = 0.432 and b = 0.652. The logarithmic gradation scale can also be achieved. Beside the evaporation of the dielectric stripes, the preparation of a suitable display involves additional steps, since planarization layers are required to avoid inhomogenities of the surface treatment, defects in alignment and discoloration.

8.6 Charge Control

A promising way to improve analog grey scale addressing is to control the electric charge injected into each individual pixel capacitor. The charge depends on the area in which the polarization reversal, and hence a transmission change, has taken place.[39] This method seems, at present, to be too complicated for large, highly coupled matrices. One possible way to overcome these problems is to use a thin film transistor (TFT) matrix structure to drive an SSFLC screen. The active addressing allows reaching the video speed even if the FLC material is not fast enough in passive scanning. Such a screen has been demonstrated[27] and proved to have a better optic performance than active screens based on Twisted Nematic LC. The achieved contrast was high, viewing angle independent and, due to a faster switching, the flicker was absent. In spite of that, the use of such a difficult and extremely expensive technology is questionable.

8.7 Outlook

The choice of the method for grey scale generation is dictated by many contradictory factors. One needs the means of producing a sufficiently large number of shades in a fast, reliable way and at low cost. So far, these requirements cannot be met. Digital techniques are the most straightforward, but require fast switching and an extended number of connections and drivers. Analog methods would be a better choice if only grey levels could be created in a repetitive way over the whole display area. So far, there is no a reliable technology for suppressing the deviations in threshold characteristics. These are caused by uneven cell thickness, defects in alignment, temperature gradients, voltage drops on the resistance of electrodes, electrical charges etc. As a result, the grey levels might get out of control in some parts of the screen.

The addressing schemes discussed in Chapter *Fast Addressing Modes* (page 51) support the time dither technique, due to their short line addressing time. The analog methods presented above are all based on conventional driving waveforms and are, thus, significantly slower. Further studies leading to the adaptation of high speed addressing methods for this purpose would be beneficial.

9 THE WAVEFORM GENERATOR

9.1 Background

Available arbitrary waveform generators are not well suited to liquid crystal addressing experiments since they were all designed with quite different applications in mind i.e. the generation of advanced analog functions, usually in one channel and at low voltage. Such functions are composed from a huge number of amplitude points that are equally spaced in time. The frequency and overall amplitude of these signals may be changed easily. However, if such an arbitrary waveform generator is to be used for creating an FLC driving waveform, consisting of the train of pulses of different duration and amplitudes, each pulse has to be defined using a certain number of points corresponding to its width. Changing an amplitude of one such a pulse involves altering all those points. The problem is aggravated, when the desired change concerns a pulse width. Then a large number of data has to be moved in the generator's memory and the total length of the waveform has to be redefined. This, in practice, requires computer control and dedicated software. It is also obvious that the process of sending new data to the instrument has to take some time, during which the connected liquid crystal cell experiences intermediate voltage steps. Such unbalanced voltage sequences may disturb the electro-optic response measurements or even damage the cell.

Because of all this and after considerable thought, I have decided to construct a waveform generator dedicated primarily to liquid crystal research. The aim was a multichannel, high-voltage device, which would allow unrestricted and safe experimenting with the waveforms during operation. And, since pulses and their combinations in addressing schemes must obey certain rules, and therefore are functionally related to each other (like switching pulses, compensation, data, etc.), the instrument and its software were designed to operate in a manner taking into account such relations.

The result was an eight-channel Waveform Generator (Figure 66) capable of pulse amplitudes up to ±100 V at a slew rate of 330 V/µs. Each pulse has its own duration stored in only one memory location. The generator is controlled by a Macintosh computer using a specially written extensive software that converts the creation and use of addressing schemes to a relatively simple task. The software includes also an on-line simulation of the optic response of the SSFLC cell. The unique feature of the device is that the process of altering the waveforms is separated from their generation (in the way described below), and undesired, intermediate pulse sequences are never delivered to the connected liquid crystal cell.

PAPER VII describes in detail an early prototype and this chapter presents the final version of the Waveform Generator.

Figure 66. Photograph of the eight-channel waveform generator.

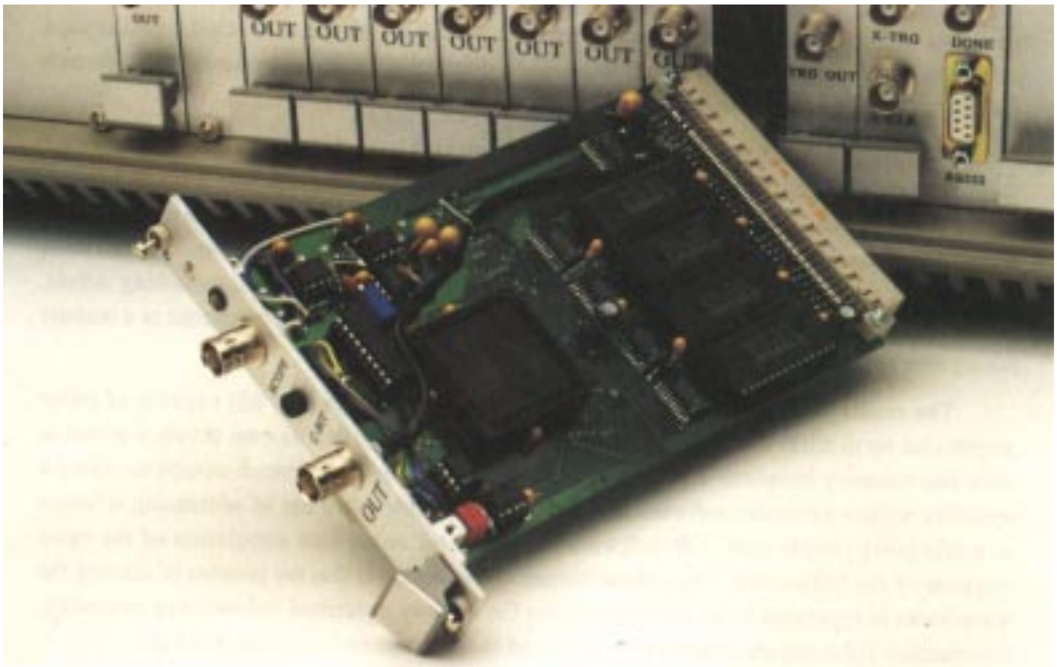


Figure 67. Photograph of the low voltage part of one analog channel. The two memory banks (four integrated circuits) surrounded by surface-mount buffers can be seen in the rear part of the board. The large square circuit in the center is the programmable logic device (MACH 130). The digital-to-analog conversion circuitry is placed in the upper left part of the board.

9.2 The Double Memory Concept

Figure 68 shows the main functional blocks of the waveform generator. It consists of a microprocessor based *Controller*, one *Time-Base* module and up to eight *Analog Output Channels*. The Controller acquires data and commands from the computer and governs all functions of the instrument. The Time-Base module generates a clock signal corresponding to the duration of the generated pulse. Amplitude data for the pulse defines, during this time, the voltage level delivered by the Analog Output Channel.

There are two *memory banks* in each module. Initially both of them store the same data. At any time one memory bank is used in the process of the output signal generation, while the second memory bank can be freely accessed by the controller. Such a configuration is the prerequisite for undisturbed waveform modification during operation. This can be clarified by the following example. Suppose that we want to change the width of a pulse N in a waveform being currently used to drive a liquid crystal cell. We do it on the computer screen using a mouse. The information about the position and the new width of the changed pulse is automatically sent to the generator. The controller circuit interprets the received information and changes the data in the corresponding location of the memory bank 2 (in this example) of the Time-Base module. It also stores it in its own memory for future use. So far, the generated

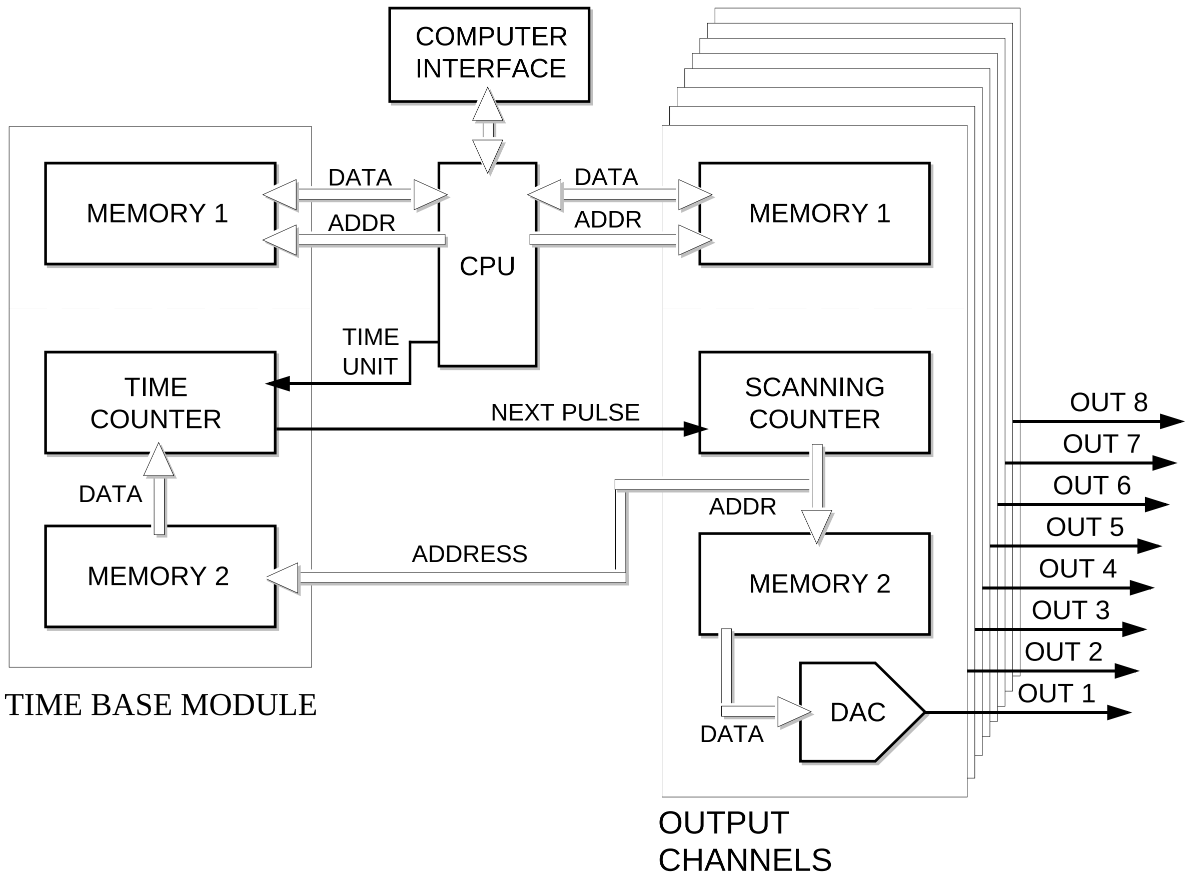


Figure 68. Functional concept of the waveform generator. The CPU block represents the entire Controller module (cf. Figure 74). Memory banks 1 and 2 are isolated from each other in each module. In this example Memory 2 is used for waveform generation, while Memory 1 is being updated by the computer. Memory banks are interchanged (swapped) at certain times.

waveform is not affected, since solely the memory bank 1 is used for its creation. The system waits now for the generated waveform to be completed and then interchanges (swaps) the memory banks. The swapping operation does not introduce any delay. The waveform generation proceeds using data from memory bank 2 and the controller gains access to the memory bank 1. Using stored information about the performed change, the controller updates also this memory. In such a way the initial state, where both memory banks hold the same data, is restored.

The existence of two memory banks functionally divides the instrument in two fairly independent parts:

- the microprocessor-based system associated with one data memory and communicating with the host computer,
- the hardware-controlled waveform synthesis circuitry using data stored in a separate memory.

Figure 69 shows the memory arrangement which is present in all module boards (the time-base and analog channels). The memory bank (cf. Figure 68) consists of two Random Access Memory (RAM) circuits capable of storing 8k (i.e. 8192) 8-bit data each. They hold a lower and an upper half of the required 16-bit data word, respectively. The memories are tied to the data bus through tristate, bidirectional buffers. Normally, the buffers are in the high-impedance state (disabled), effectively disconnecting the memories from the data bus. When a specific memory circuit is selected by the controller, the corresponding buffer is opened. The direction of the data flow is then defined by the read/write signal. The buffers associated with the memory set used for the waveform synthesis are always disabled and these memories are, thus, isolated from the controller activity.

Both memory banks have separate address buses. Their function is associated with the memory bank swapping. One of them is simply the microprocessor address bus while the other one is driven by a scanning counter. The scanning counter points at the memory location where the data for the next pulse to be generated is stored.

The *Data Selector and Control Logic* block (Figure 69) converts the two 8-bit data from chosen memories to the 16-bit format and governs the activity of the buffers, the direction of data transfer and the memory bank swapping.

To clarify this point, Figure 70 presents the functional block diagram of the Analog Output Channel in the situation where the first memory bank is accessed by the microprocessor and the second memory bank is being used for the waveform synthesis. Both buffers associated with the second memory bank are in the high-impedance state, which means that there is no connection between the memory circuits and the common data bus. The data, chosen by the supplied address, are directed straight to the digital-to-analog converter (DAC). It uses only twelve bits out of sixteen, so the remaining four bits can be used for other purposes. In the present design bit number 16 is provided on a front panel of each module and can be utilized for synchronization with other equipment. Figure 69 shows also how the controller reads data from the first memory bank. The buffer associated with the selected memory circuit is opened in the direction from the memory to the common data bus, while the other one remains in the

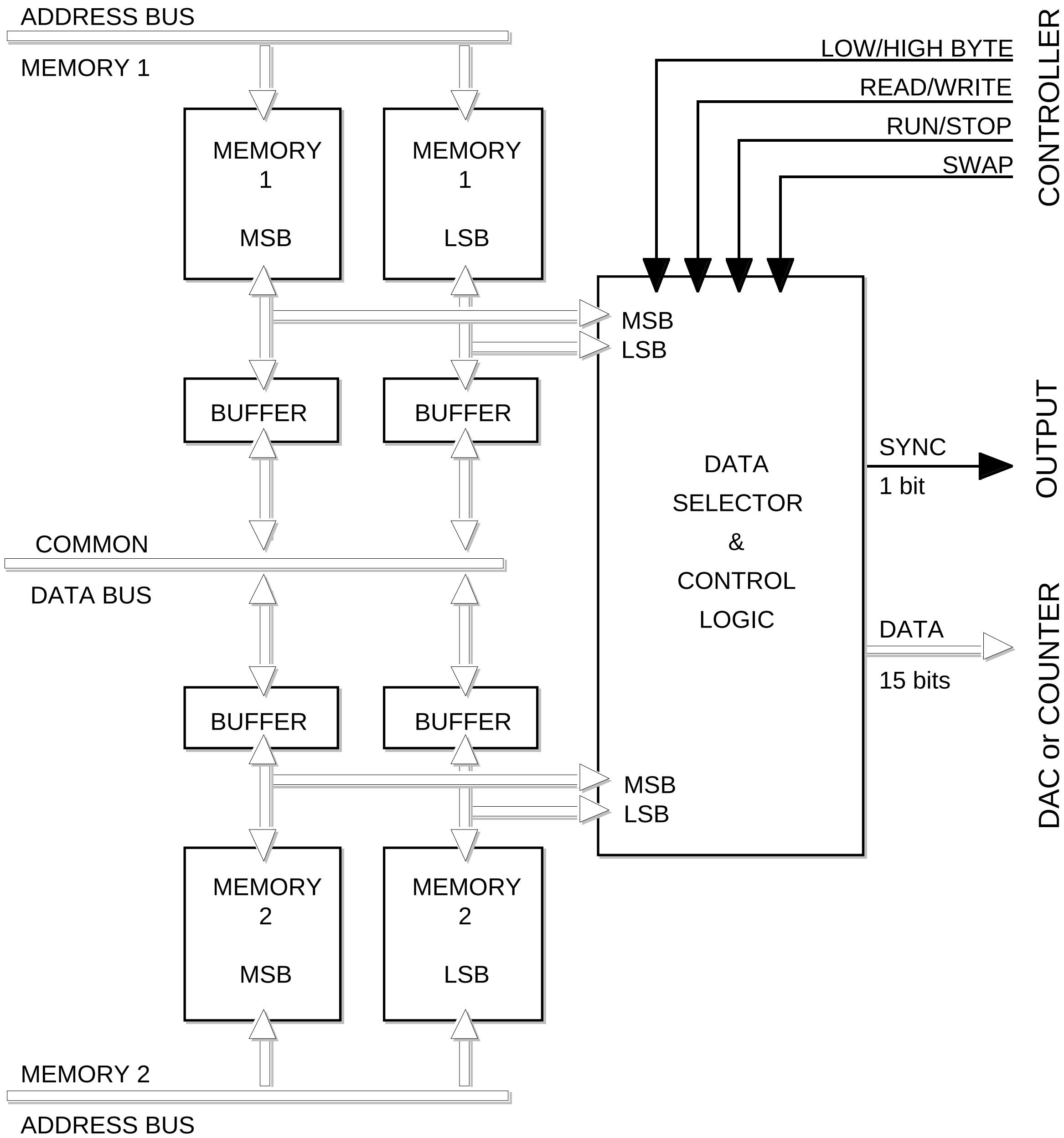


Figure 69. The memory arrangement on each analog channel and time-base boards. Upper and lower byte (msb and lsb, respectively) of the 16-bit data are stored in separate memory circuits. Four bidirectional buffers govern the data flow.

high impedance state. The signal routes of the two operations have no common parts and they can, thus, be performed independently.

9.3 Creation of an Analog Output Signal

The binary data describing the pulse amplitude are supplied to the digital-to-analog converter circuit (DAC). The DAC produces a current which is then transformed by an operational amplifier to a voltage level in the range ±10 V that is finally expanded to ±100 V by a high voltage amplifier.

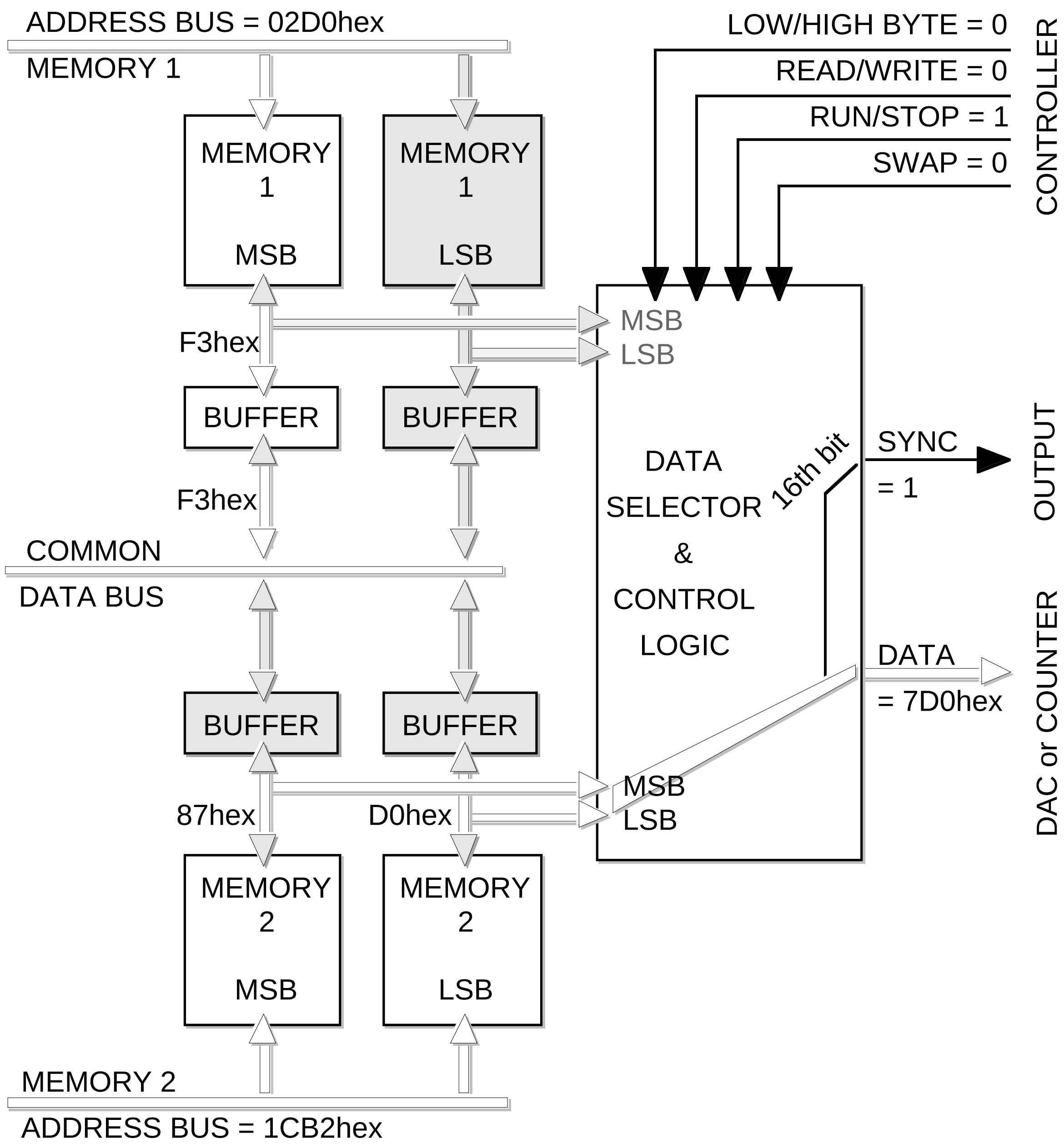


Figure 70. Functional diagram of the output channel in an example situation where the controller reads a most significant byte (msb) for the pulse number 720 (2D0 hexadecimal) from the memory bank 1, while a pulse number 7346 (1CB2 hexadecimal) is being generated. As can be seen, this pulse contains also a trigger point (logical 1 at the SYNC output). The disabled data paths and directions are shaded.

The key parameters are the conversion speed and the bandwidth of the amplifiers. After a number of experiments, the digital-to-analog converter type AD668 (from Analog Devices) was chosen. Its output reaches 99% of the desired value within 25 ns (the settling time). An operational amplifier AD844 makes up the second stage and the PA85 high voltage amplifier (Apex µtech) brings the voltage up faster than 330 V/µs. The scheme is presented in Figure 71 and an oscilloscope trace of a generated pulse sequence is shown if Figure 72. The high voltage amplifier has a very low output impedance, less than 0.1 Ω, and the pulse amplitude is inde-

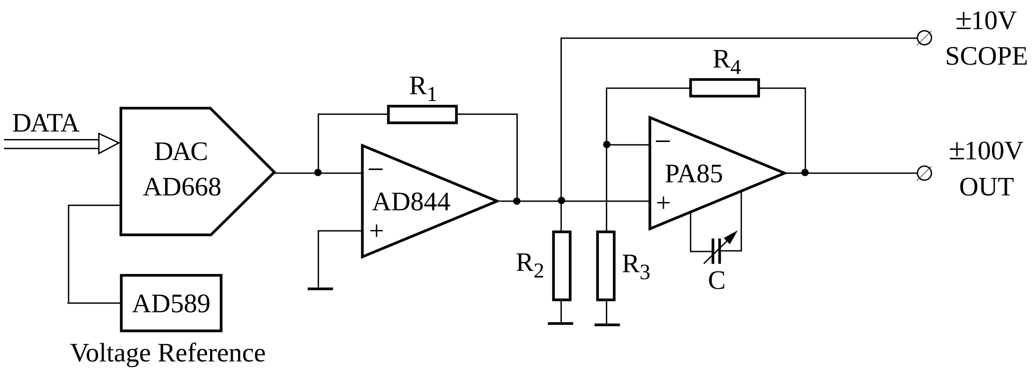


Figure 71. The scheme of the analog part of the waveform generator performing the conversion of the pulse amplitude from digital to analog form (a voltage level).

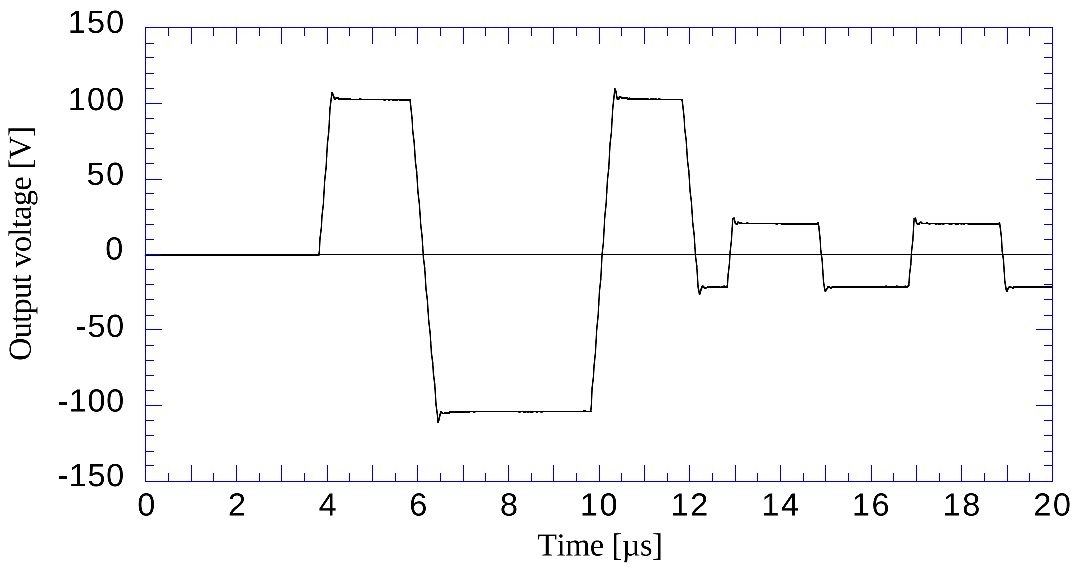


Figure 72. An example of the Waveform Generator high voltage output: the oscilloscope trace (Tektronix TDS320) of a generated pulse sequence of the SSFLC cell test waveform.

pendent of the connected load (within the current limit), which is not the case in a conventional Arbitrary Waveform Generator.

In order to avoid voltage spikes while switching the instrument on, the high voltage power supply for the PA85 amplifiers is delayed until the digital part and the low voltage analog part reach their normal operating conditions and the input signal for the high voltage amplifiers stabilizes at zero volts. For the same reason, when switching the instrument off, the high voltage is completely removed before the supply voltage of the digital part starts to fall.

Output connections from both operational amplifiers are provided on the front panels of the analog modules. The intermediate, low voltage output (±10 V) can be used for monitoring the signal on the oscilloscope. Liquid crystal addressing experiments typically require simultaneous observation of the optical response of a chosen pixel and the voltage applied to it. This voltage is formed by a superposition of respective row and column waveforms. Since the oscilloscopes usually have only two channels and one of them is already occupied by the cell's optical response signal, an additional summation module has been incorporated into the generator. It has an inverting and a non-inverting low voltage input and produces a superposition waveform of an amplitude scaled down to ±10 V. The summation module is constructed using three operational amplifiers arranged as shown in Figure 73.

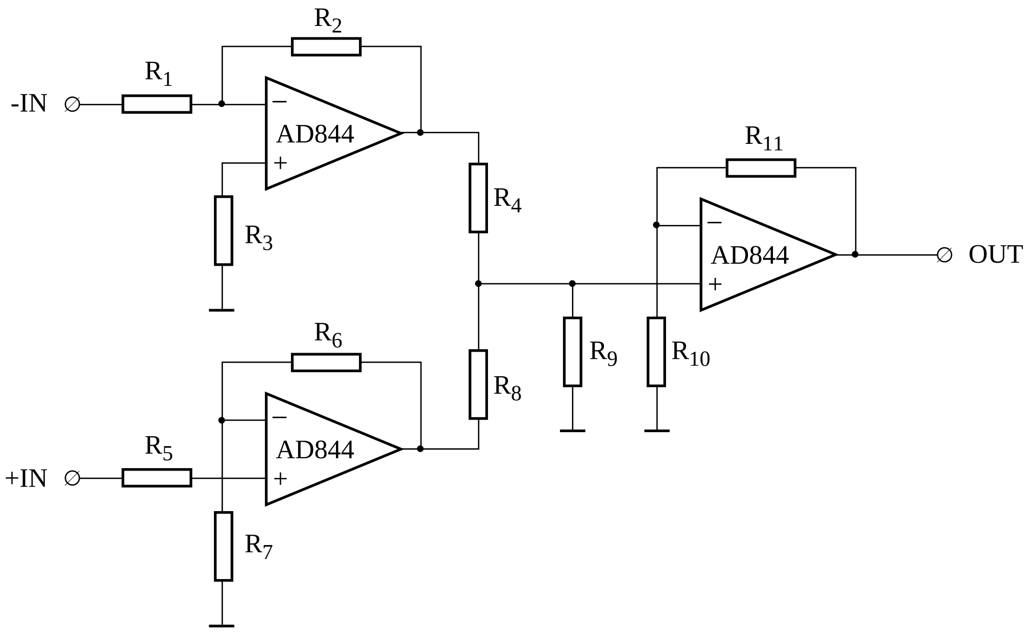


Figure 73. The summation module creates a signal corresponding to the difference between two supplied low voltage (±10 V) signals reproducing, from the superposition of row and column signals, the actual waveform acting on the pixel. The resulting superposition signal is scaled down by one half to the ±10 V range.

9.4 The Time-Base

The Time-Base module defines the width of each pulse being generated. The module contains the same memory arrangement as the analog output channels (cf. Figure 69), but instead of a DAC there is a binary counter. Out of available sixteen data bits, fifteen hold the duration of the pulse defined as a number clock periods. The last, sixteenth bit controls the trigger signal used to synchronize an oscilloscope with a chosen part of the generated waveform.

At the beginning of each waveform step a 15-bit data is loaded to a counter. The time-base counter is decremented by every falling edge of the supplied clock signal. When reaching zero, which signifies the end of the pulse, this counter sends a signal to increment the memory address counter. The data corresponding to pulse amplitudes in the subsequent waveform step are then supplied to the DAC in each analog output channel. At the same instant the time-base counter is reloaded with a new value and the process repeats.

The period of the clock signal is normally 250 ns or 1 µs. If very long pulse durations are required it can be set to multiples of 1 ms (in the range from 1 ms to 65.5 s). The clock signal can also be supplied externally, using for example a simple square wave generator.

9.5 The Controller

All functions of the Waveform Generator are supervised by the Controller Module (Figure 74). Its central unit is the Motorola 68HC11F1 microprocessor operating at 4 MHz.

The microprocessor's involvement in the waveform generation is, for the reason of speed, limited to posting two "flag" signals only. One is the *Run* flag that, when raised (to the logical "true" level), directly initiates the generation of the waveforms. By inverting this signal the microprocessor requests that the generation should stop. The second "flag" signal provided by the microprocessor indicates that its memory bank has been updated and that the memory swap should take place. Both these flags are checked by the hardware logic during the last waveform pulse and the corresponding action is taken.

The hardware logic consists of functional blocks shown in the central part of the Figure 74 - the Control Logic, the Scanning Counter, the Top Address Register, the Comparator and the Address Bus Selector. The Scanning Counter provides the memory location of the data corresponding to the pulse currently being generated. The value in the counter is continuously compared with the address of the last waveform pulse. By this means the end of the waveform can be recognized. The Address Bus Selector performs the memory swapping. It directs the output of the Scanning Counter to one memory bank while attaching the other memory bank to the address bus of the microprocessor. The information about the memory arrangement is also contained in the Swap signal, which is used to control the memory data buffers (cf. Figure 69).

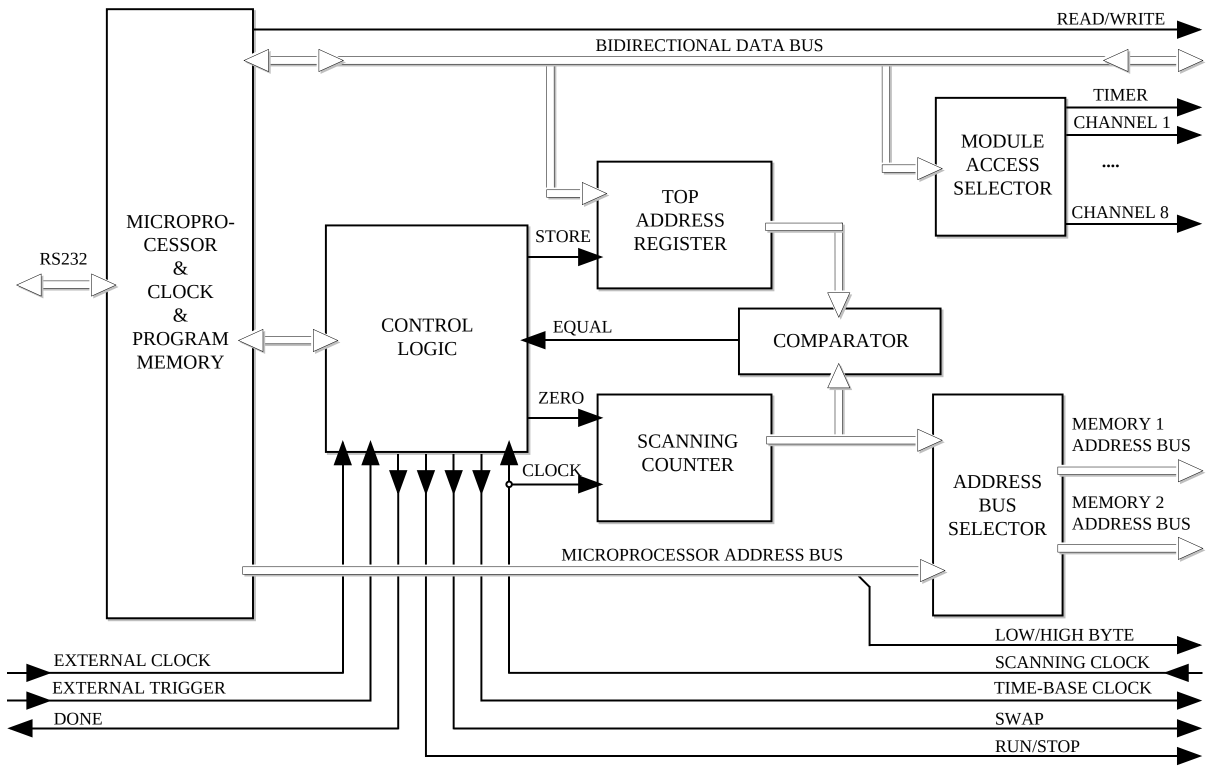


Figure 74. The functional scheme of the Controller module.

The main duty of the microprocessor is to communicate with the host computer, receive data and perform commands. The communication is done serially (according to the RS232 standard) at a speed of 19200 baud (bits per second). The function of the microprocessor is defined by a program written in the assembler language and contained in the Read-Only Memory (ROM) circuit. The communication with the host computer is initiated by reporting the number and position of installed analog channels. The user assigns waveforms to these channels and the computer starts sending data. At this point the generator is stopped and the microprocessor has access to both memory banks. It can thus place each received data byte at the desired memory location in one bank, swap the memory banks, and write the byte again to the other memory.

The memories on all modules occupy the same physical address space. In order to find the desired memory location, the microprocessor must first choose which module it wants to access. This is done by setting or clearing corresponding bits in the Module Access Selector block (cf. Figure 74). Then the memory bank (1 or 2) is defined by the swap signal. Each bank consists of two memory circuits holding lower or upper byte, respectively. The choice of the circuit is done by the Low/High Byte signal (the lowest address line of the microprocessor, A0, plays this role of selection). The exact location within the chosen memory circuit is determined by the applied address. Finally, the direction of the data flow is controlled by the Read/Write signal.

As mentioned before, when the generator is running the microprocessor can access only one memory bank. The received data have to be stored until the other memory bank becomes available. This is done using a “note-pad” memory (32 kb RAM) placed on the controller module.

9.6 The Programmable Logic Design

Except for the buffers, the Waveform Generator does not contain any traditional, small TTL-type circuits. All digital logic was constructed using large programmable logic devices (EPLDs) - MACH 130 and MACH 210 (produced by Advanced Micro Devices). Some functional blocks were designed in the form of a scheme using the library models of standard digital circuits, while others were defined as Boolean equations. Using PALASM 4 software, the design was converted first to a set of minimized logical equations and then to a form required by the device programmer (a so called JEDEC-standard file). In order to detect eventual errors in the early stage of the design, the operation of each block was first individually simulated. Then, the whole design was reduced to 3-bit address and 4-bit data lines to allow software simulation of the entire function of the Waveform Generator at once.

The controller module requires three circuits: one MACH 130 contains the scanning counter and address bus selector, another MACH 130 holds the top address registers, comparator and module access selector, while all remaining control logic occupies the MACH 210. The analog-output channels use one MACH 130 each, containing the data selector and control logic for the buffers. In the timing module, this circuit incorporates also a 15-bit down-counter. In this way the timer and analog output channels could use the same printed circuit layout.

The use of programmable logic circuits simplified the layout of printed circuit boards since the pin numbers could be quite freely assigned to the signals. Starting up a new design usually requires some adjustments to be made. These were limited to changing or adding a few equations or symbols in the scheme drawn on the computer. The involved MACH circuit was then simply reprogrammed without the need of remaking the printed circuit layout.

9.7 The Waveform Generator Software

The development of a software which would be as straightforward to work with as possible, but containing all the desirable features, was also a quite time consuming task. I have chosen to design it for the Macintosh system due to its well-known, user-friendly graphical interface and the modern, powerful operational system of that computer.

A snapshot of the computer screen is presented in Figure 75. The program window is divided into several areas. On the top there is a menu bar. In the center there are two sections (so called “panes”) where waveforms can be drawn. Their superposition is presented in the upper pane. The controls for the timing, amplitude, displayed waveform and the communication with the generator occupy the right hand side of the window.

In the liquid crystal addressing experiments we are usually interested in the relation between row and column signals. Thus, two waveforms (marked A and B, respectively) may simultaneously be designed. For the same reason, the superposition of these two waveforms (A-B or B-A), corresponding to the effective driving voltage seen by the liquid crystal cell, is presented (in a quarter scale) on the upper part of the screen. The optional, thin vertical lines mark the line addressing periods. The waveforms, to be displayed on the screen, are chosen via ‘pop-up’ menus (drawn, by convention, as rectangles with a drop-shadow). The text on the menu button consists of the associated output-channel number and the waveform name. The number of waveforms is limited only by the available memory in the computer.

The pulses may be created or altered either by the usual ‘point, click and drag’ method (cursor) or by entering the desired value from the keyboard. A grid may be defined to facilitate the editing operation.

The timing information is drawn in the lower part of the screen. Short vertical lines mark the time-slots. The widths of the pulses may be altered in the same way as their amplitudes. Additionally, the boundary between two time-slots may be moved. An arbitrarily placed oscilloscope trigger signal, marked as a small triangle, is also visible here. Since the waveforms are normally much longer than the available window size, a scroll bar is provided at the bottom of the window. The *Goto* menu assists in finding the desired waveform step.

Pulses, sequences and entire waveforms may be copied, cut, pasted, cleared, deleted and duplicated in the usual Macintosh-way. They may also be inverted, mirrored or rolled. The last editing operation can always be undone.

The commands affect the selected pulse or waveform. In the example presented, waveform A is active, which is marked by a frame around the ‘A’ letter. The pulse selection is visualized by an animated ‘marching ants’ pattern (seen on the drawing as a dashed rectangle).

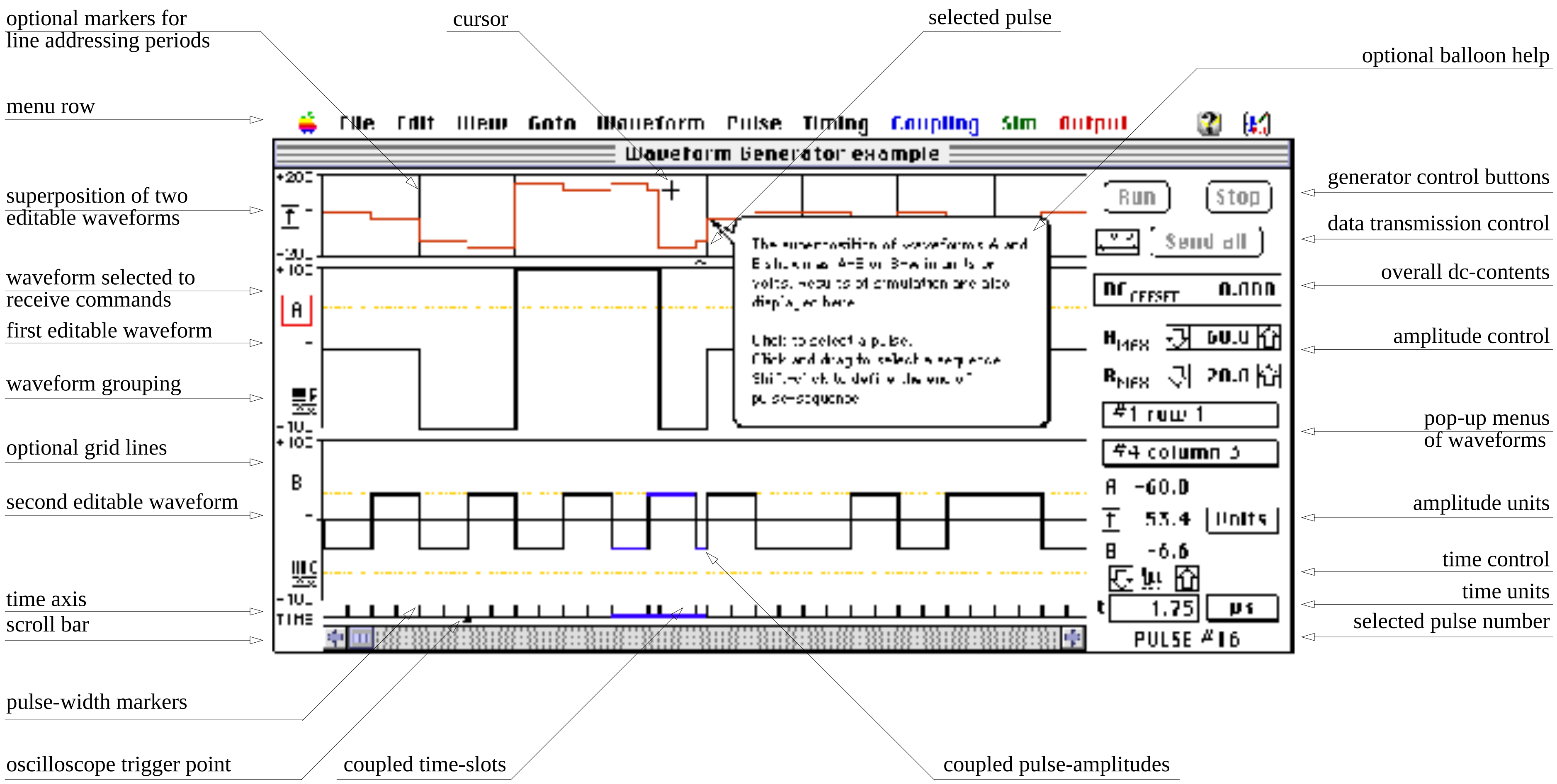


Figure 75. A snapshot of the Macintosh screen showing the Waveform Generator program window. In the center there are two sections where waveforms can be drawn. The waveform superposition, corresponding to the signal seen by a pixel, is shown in the top section which is also used to present the simulation of electro-optic response. In the bottom part of the screen there is a time axis where the width of each pulse can be edited. The control panel is situated on the right-hand side of the screen. A first-time user can be assisted by a help balloon which follows the cursor movements and concisely describes the screen and menu items.

Parameters of the selected waveform-step are displayed in the bottom-right part of the screen. The units are selectable via pop-up menus (volts, respective μs, or ±100 arbitrary units). The maximum-amplitude controls for respective waveform are drawn above the waveform names. ‘Clicking’ with the mouse on an up or down arrow makes an expected change, while clicking on the value allows for the keyboard entry. The timing may be changed in a similar way. The DC-content in the effective driving signal is continuously monitored.

The waveforms may be joined as column, row or arbitrary groups. Adjusting the maximum amplitude of a waveform assigned to a group results in the corresponding adjustment in the remaining members of this group. Thus, it is possible to simultaneously change the amplitude of all column waveforms, for example.

Three buttons for communication with the generator (‘Run’, ‘Stop’ and ‘Send all’) are placed in the upper-right corner of the screen. The ‘auto’ sign means that the changes will immediately be repeated by the generator. If more extensive alternations of the waveforms have to be done, the communication may be switched to a manual mode (then the ‘Send all’-button changes to ‘Update now’). Prior to using these buttons, the communication with the generator must be established and the waveforms must be assigned to physical channels of the generator, using a ‘dialog window’ where only the existing channels are shown.

The pull-down menus, shown in the menu bar at the top of the screen, provide many additional features. The ‘Coupling’ menu requires special attention. It allows for defining the relations between pulses in the waveforms. The coupled pulses are presented differently when waveforms are drawn on the screen, either by a distinct color or a grey shade on a black-and-white display. There are different classes of couplings. A pulse may have a ‘constant area’ attribute - the amplitude of this pulse is then automatically adjusted each time its duration changes. Any number of pulses may have their amplitudes coupled together. This is done by choosing one of them as a ‘master’ (reference) and assigning the coupling parameters (master pulse name, multiplication factor ‘n’ and offset) to a ‘slave’ pulse, such that its amplitude will always follow the relation

$$A_{slave} = n \times A_{master} + \text{offset}$$

When a ‘coupled’ pulse is altered, the software readjusts the amplitude of the master pulse and propagates the change to all related pulses, which may be in different waveforms, even those not shown on the screen. These slave pulses make then corresponding changes in their amplitude values. Finally, the appropriate information is transmitted to the waveform generator. There is no limit on the number of coupling chains nor on the number or placement of pulses within each chain. The time-slots may be coupled together in the same way.

The program has been written in object-oriented C++ programming language. It is compatible with the Macintosh System 7 and uses its ‘help balloons’ to assist a first-time user.

9.8 The Simulation Software

The numerical simulation of the electro-optic response of a surface-stabilized ferroelectric liquid crystal cell is based on the addressing-effective model elaborated by Maltese *et al.*[84]

and discussed in Chapter *Bistable Switching* (page 15). The simulation parameters can be provided in two ways: as a set of physical parameters of the cell or as a set of reduced parameters which were introduced in the model. Both parameter sets can be used interchangeably and Table 1 summarized the required data for respective set. (The actual calculations are performed using the reduced set of parameters, but the conversion from and to the physical set is transparent for the user).

Table 1: Required data for the two sets of simulation parameters.

parameter	symbol	unit	physical set	reduced set
initial azimuthal angle	$\phi_{(t=0)}$	rad	•	•
azimuthal angle of memorized state	ϕ_0	rad	•	•
angle of the ferroelectric cone	θ	rad	•	•
smectic layer inclination	δ	rad	•	•
dielectric biaxiality	$\partial\varepsilon$	–	•	
dielectric anisotropy	$\Delta\varepsilon$	–	•	
rotational viscosity	η	mPa s	•	
spontaneous polarization	P_S	nC/cm^2	•	
relaxation time	t_R	µs	•	
cell thickness	d	µm	•	•
azimuthal angle at infinite voltage	ϕ_V	rad		•
characteristic voltage	V_C	V		•
characteristic time	t_C	µs		•
voltage linearity range	λ	–		•

The effect of an entire addressing scheme or just a chosen pulse sequence can be simulated. The calculated electro-optic response is displayed in the upper part of the program window overlaying or replacing the pixel waveform normally shown in this place. The azimuthal angle ϕ reached at the last simulation step is presented in both parameter-set dialogs to assist adjustment of the initial value of this angle, $\phi_{(t=0)}$. The simulation program can automatically follow all changes made on the waveforms shown on the screen, continuously updating the calculated optical response. The results can be stored in a file (in universal spreadsheet data format which nearly all programs can read). Delay and rise time of the electro-optic response to a chosen pulse can also be directly obtained from the simulation.

9.9 Application Areas

It is nearly impossible to predict all parameters a research instrument should have. The requirements change with the progress of investigations and instruments which cannot be adapted to them is no longer useful. This was recognized in the early, hardware-based addressing generators used and described in Papers I and II. So far, the present Waveform Generator has been able to accommodate new demands simply by improving the software (both for the Macintosh and the internal microprocessor) or by adding functions to the programmable logic devices. Since the Waveform Generator is controlled through a standard serial interface, also different computers and programs can be used to adapt the instrument to specific needs.

The Waveform Generator has been successfully tested in several liquid crystal research laboratories abroad (Italy, Switzerland, Korea, Japan and USA). It has proven particularly simple to use even for persons with no previous experience in electronic addressing of displays. Even first time users could easily draw the waveforms and manipulate them while observing the changing optical response of the experimental cell. Addressing schemes based on time-overlap, that are nearly impossible to implement using existing integrated drivers, can easily be realized and tested by this system. The scope of applications of the Waveform Generator is not limited solely to addressing ferroelectric liquid crystals. It can equally well deal with antiferroelectric and all kinds of nematic devices. Even electroluminescent and vacuum fluorescent displays can be driven and tested by the instrument.

In this work the Waveform Generator has permitted the study, in considerable detail, of the effect of different addressing schemes on a certain material as well as of the effect of small adjustments in the addressing scheme. The versatility can be appreciated from the waveform-response curves presented in Chapters 5, 6 and 7 (Figures 22, 28, 30, 31, 34, 35, 36, 37, 38, 39, 41, 42, 44, 47, 49, 50, 51, 52, 53, 55) which were all obtained by the instrument like many others not reproduced here. It has also permitted a first direct comparison between different schemes, and therefore their relative evaluation, regarding achievable speed / required voltage, an aspect which is commented on below. Many other aspects have to be included, for instance the working temperature interval in which a scheme would work, in order to make a final objective evaluation between schemes. The power consumption should also be included. This will be the object of future work, which the Waveform Generator will greatly facilitate due to its speed of operation.

10

EXPERIMENTAL CELLS AND SETUP

10.1 The Experimental Setup

The experimental setup, as schematically presented in Figure 76, consists of a polarizing microscope, the waveform generator, an opto-detector, a digital oscilloscope and two computers. The measurements were performed by placing a liquid crystal cell in a microscope (Olympus) between crossed polarizers aligned in such a way as to produce a symmetric optical response. As light source a halogen lamp was used. It was powered by a stabilized dc-supply to avoid the normally appearing variations in the light intensity. The cell was driven by the waveform generator, which, in turn, was controlled from a Macintosh computer using the specially developed software. The instrument and its program has been described in detail in Chapter *The Waveform Generator* (page 77). The light transmission through the cell was monitored by an opto-detector, also designed and built at the CTH laboratory.[73] The electro-optic response signal of the cell was amplified and delivered to one of the two channels of a Tektronix TDS320 digital oscilloscope.

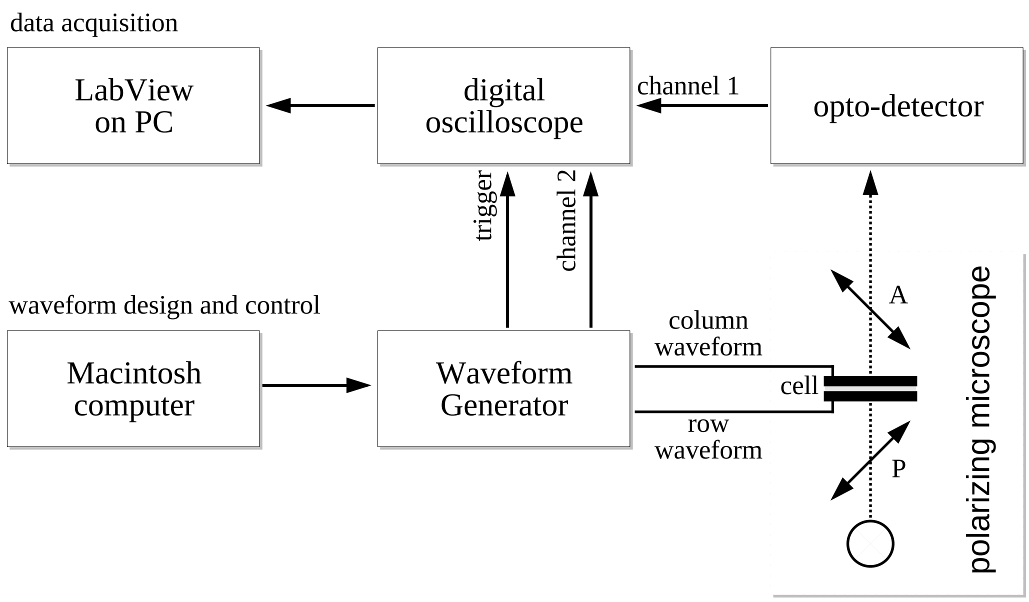


Figure 76. Instrument setup for addressing experiments with SSFLC cells.

The driving voltage, represented by the waveform seen by the studied pixel, was monitored using the second channel of the oscilloscope. This voltage consists of a superposition of waveforms delivered to a corresponding row and column electrodes, and was obtained from the Summation Module of the Waveform Generator. The oscilloscope was triggered externally to facilitate the selection of a desired point of the waveform under observation.

In order to store and further process the measurement results, the data from the oscilloscope had to be transmitted to a computer. This was done by a “virtual instrument” created on a PC using the LabView software. The obtained data were displayed in a higher magnification on the computer screen and stored in a universal spreadsheet-file format. Such data files could directly be read by the KaleidaGraph program on the Macintosh.

It was also important to document the large amount of collected measurement data. Limited file naming capability of the PC (maximum eight characters) was, naturally, an annoying obstacle. To overcome this, experimental notes were filed. Additionally, a log-file of all experiments were kept. This file was then converted to a searchable data base using FileMaker software on the Macintosh.

10.2 The Opto-Detector

The opto-detector has been especially designed[73] for electro-optic characterization of liquid crystals. The light sensitive component is a silicon PIN photo-diode (type BPW 34), which makes a good compromise between sensitivity and speed. As opposed to a photomultiplier, such a diode can easily handle high light-intensity levels used in microscopy. Figure 77 shows the scheme of the opto-detector, while the assembly is presented in Figure 78. The photocurrent from the detector is first processed by a high speed amplifier LH 0032 and then fed to a line driver LH 0033 (both by National Semiconductors) that can handle a standard 50 Ω coaxial cable without degradation of the detector data. The gain of the first amplifier is constant and set to one hundred by means of the feedback resistor network R_1 and R_2. The bias voltage from the pull-up resistor R_B, is necessary to reduce the capacitance C_D of the photodiode. With B ≈ 15 V, the C_D was less then 10 pF. The sensitivity of the opto-detector is only

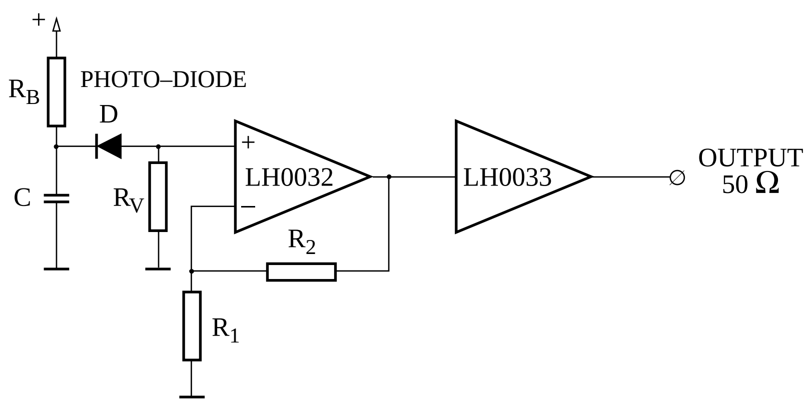


Figure 77. The simplified scheme of the opto-detector. The photocurrent from a biased PIN-diode (D) is amplified and fed into a 50Ω-line driver. The bandwidth of the device is better than 5 MHz.

Figure 78. The opto-detector can be mounted on a microscope using standard components of the Spindler & Hoyer optical bench system. The power supply is shown to the right.

dependent on the resistor R_V used in the form of a BNC-type plug-in adaptor.

The dynamics of the detector system is determined by the capacitance of the photodiode C_D, input capacitance of the amplifier C_A and the resistance R_V. The capacitance C_A, including stray capacitances, was also less than 10 pF. The total response time τ of the system is given by

$$\tau^2 \approx 1.21(\tau_D^2 + \tau_A^2) \tag{31}$$

where τ_D could be obtained from

$$\tau_D \approx 2.2\, R_V(C_D + C_A) \tag{32}$$

and τ_A was measured to be less than 40 ns. With $R_V = 1$ kΩ the response time is equal to 65 ns, which is sufficient for SSFLC measurements.

The output voltage U_{OUT} from the device is given by:

$$U_{OUT} = I\,\Re_D\,R_V\,G \tag{33}$$

where I is the light intensity at the detector diode, $\Re_D$ is the detector responsivity factor ($\Re_D > 300$ mA/W at 600 nm) and G is the gain (G = 100). U_{OUT} was set to swing between zero and 4 volts. As the circuit is dc-coupled, the total optical transmission, including the background light, can be measured.

The device is constructed in a stable metal cabinet which provides the necessary screening. It can be mounted on any microscope with external camera connection using standard Spindler & Hoyer opto-mechanical building blocks.

10.3 Preparation of SSFLC Cells

The SSFLC test cells, used in all of the addressing experiments presented in this work, were fabricated by Marek Matuszczyk using the clean room facilities of the Chalmers liquid crystal group.[85] Substrates were prepared using indium-tin-oxide (ITO) coated glass Baltracon Z20 (commercially available from Baltzers). These substrates have a thin SiO_2 stop-layer (ion diffusion barrier) between the glass and the ITO film. When the ITO is etched away in certain areas during preparation of an electrode pattern, the stop-layer blocks the migration of sodium ions into the liquid crystal. The alignment layer alone is insufficient for this purpose. Ion contamination of both alignment layers and the bulk of liquid crystal deteriorates the switching properties, as it has been discussed in Chapter 4.4 *Ionic Effects and Reverse Electric Field* (page 23).

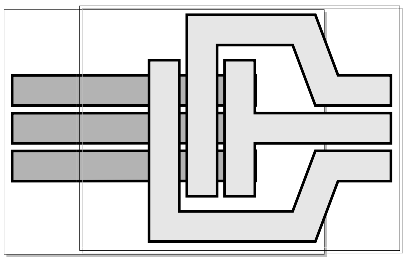


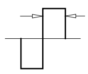
Figure 79. Electrode pattern in the cells investigated in the present work, drawn in 2:1 scale. The real size of a pixel is 2x2 mm.

Figure 79 presents an electrode pattern in the test cells forming a 3x3 matrix. It was prepared using a conventional wet photolitography process. The resistance of the ITO layer was, according to the manufacturer's specifications, less than 200 Ω/square, which is sufficiently low for such small cells with broad electrodes. Carefully cleaned substrates were coated with a variety of polymer aligning materials. The dilute (typically 4-6% by weight) polymer solution was deposited by spinning. After evaporation of the solvent, the polymer films were dried in an oven and then buffed unidirectionally at a constant, weak rubbing strength[43] using a nylon velvet. The cells were assembled with the rubbing direction parallel on both substrates. The glasses were fixed together with UV light sensitive glue NOA 68. The empty cell thickness was defined by 1.5 or 2.0 μm polyball spacers and checked using the wavelength dependence of the light transmission interference pattern. (Beside polymer alignment also oblique evaporation of SiO is normally used for experimental cells in the group but such cells were not utilized in the present work.)

The cells were filled under vacuum with different room temperature FLC mixtures developed for displays. An empty cell was placed on a heating plate inside a dedicated vacuum chamber.[85] The temperature was elevated to, typically, 70°C and the cell gap was evacuated. When the pumping process was completed, the temperature of the heating plate was further raised to the level above the liquid crystal transition to the isotropic phase. After stabilizing the temperature at this level, the liquid crystal was brought in contact with the cell edges and, thus, melted. The liquid was then sucked into the cell by capillary action. Finally, the filled cell was taken out of the vacuum chamber and placed in a temperature-controlled cooling stage, where it was slowly cooled down to room temperature without applying any fields or mechanical stress.

The electrical connections to the cell were prepared by soldering thin wires directly onto the ITO electrodes using an ultrasonic soldering gun (Sunbonder USM-III from Asahi Glass Co. Ltd., Japan).

Table 2: Parameters of materials and experimental cells.

parameter	symbol	unit	SCE8	BDH858	ZLI 4655/ 000
cell thickness	d	μm	2.3	2.3	2.2
phase transition	N*-I	°C	100	87	72
	A*-N*	°C	79	73	69
	C*-A*	°C	59	62	60
birefringence	Δn	–	0.16	0.13	
dielectric biaxiality	∂ε	–	+0.30	>0	+0.064
dielectric anisotropy (at 1kHz)	Δε	–	-1.5	-1.0	
dielectric anisotropy (at 100kHz)	Δε	–	-2.0	-1.4	-0.8 (20 kHz)
spontaneous polarization (at 20°C)	P_S	nC/cm^2	+6.3	+8.4	+7.0
spontaneous polarization (at 30°C)	P_S	nC/cm^2	+5.1	+8.0	+6.0
rotational viscosity	η	mPa s	648		120
tilt angle (at 30°C)	θ	degrees	19.0 (30°C)	18.5 (30°C)	23.5 (22°C)
bipolar pulse response time (20°C, 10V/μm)		μs	255	100	80

10.4 Parameters of the Experimental Cells

In order to compare the efficiency of different addressing schemes three experimental cells filled with different liquid crystal materials were selected. The cells all have Hitachi HL 1110 polymer as the alignment layer. The three material are Merck SCE8, BDH858 and ZLI 4655/000, for which Table 2 summarizes the properties. Most of the material parameters were measured at the Chalmers laboratory by different members of the liquid crystal group. Some parameters, like birefringence, rotational viscosity and phase transition temperatures are stated according to the manufacturer's specifications.

10.5 Test Waveforms

To assess the *general multiplexability* of the material, the test waveform of Paper VIII, shown in Figure 80, was used. It consists of a three-pulse dc-balanced switching sequence followed by a hf square wave and a zero-voltage period, and by an identical waveform of inverted polarity. The amplitudes of the pulses in the switching sequence are all equal and their durations are programmed (cf. Chapter 9.7 *The Waveform Generator Software* (page 87)) so that the width of the central pulse t_3 is equal to the sum of the durations of the first pulse, t_1, and the third pulse, t_3. By changing the ratio between t_1 and t_3, the central pulse can be moved within the sequence without changing the sequence length nor disturbing its dc-balance. In such a way, a complete or partial switching due to the third pulse can be obtained. The hf square wave following the switching sequence is also dc-balanced. It starts and ends with a half-width pulse to minimize the excursion of the optical response (this can be seen in Figure 36 on page 46). Amplitudes and durations of all pulses of the hf sequence can be changed simultaneously. Finally, a zero voltage period of variable length is applied in order to allow observation of the director relaxation. Due to the powerful control software written for the Waveform Generator all adjustments described above could be performed in a very simple and quick way (usually just a single mouse-click).

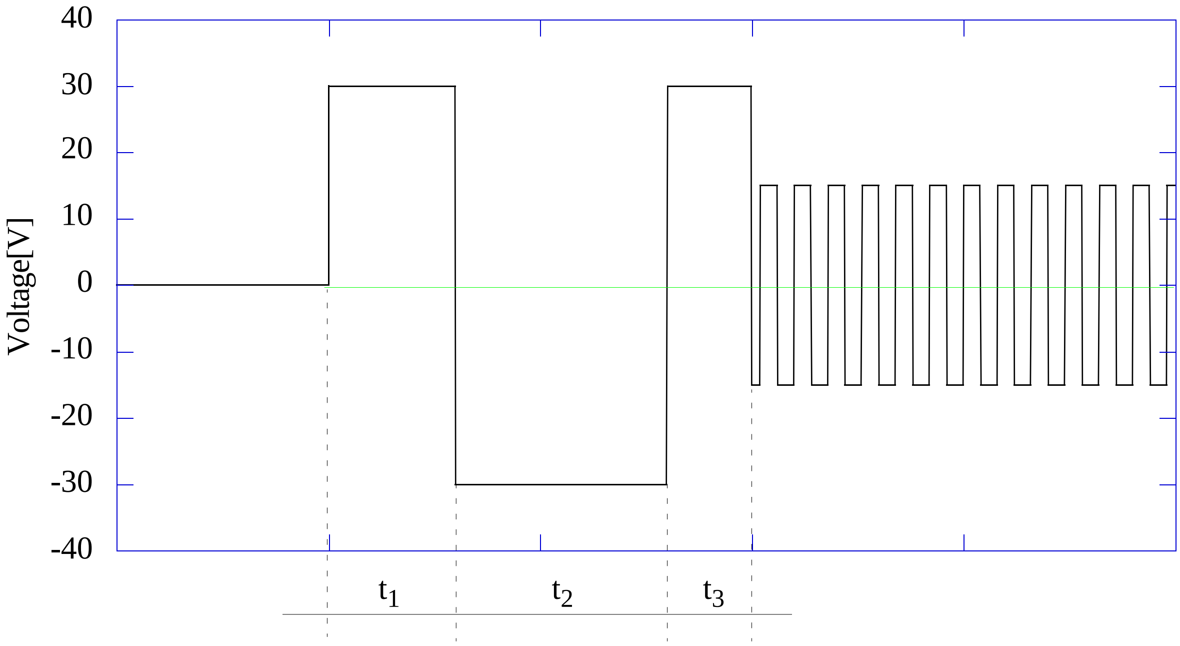


Figure 80. A part of the test waveform used to assess the multiplexability of experimental SSFLC cells in a quick and simple way. The three-pulse switching sequence is dc-balanced, constructed such that $t_2 = t_1 + t_3$. By changing the ratio between t_1 and t_3, the central t_2 pulse can be moved within the sequence. The hf square wave starts and ends with a half-width pulse to make the oscillations in the electro-optic response start at the convenient level (cf. Figure 36). The square wave is followed by a zero-voltage period.

A typical testing procedure was as follows. The operating point of the test waveform, having initially a zero hf voltage, was set to obtain a clean switching on t_2 and t_3, and the cell was rotated for best and symmetric optical response. The amplitude of the switching pulses was initially set to 30 volts, which was assumed safe for all the cells. At this point the switchability of the cell, and also the speed, could be assessed. On this ground a suitable frequency of the hf square wave could be estimated. Then, the amplitude of the hf sequence was raised to (typically) 15 volts and the t_3 was gradually reduced (by moving the t_2 pulse to the right, as described above). It was assumed that if the contrast was enhanced by the hf wave, and also if the partial switching due to the t_3 pulse could be completed by it, the cell should be multiplexable using the fast addressing schemes. In order to gain an indication of possible operating region of such an addressing scheme, two limit values of t_3 were measured – the minimum duration of t_3 which still produces a clean switching (assisted by the hf wave), and the maximum length of t_3 for which the optic response was forced back to the initial state. The cells not showing any hf contrast enhancement, but switchable, bistable and with good optical contrast in relaxed states, might still be multiplexable using the conventional (low voltage) addressing schemes.

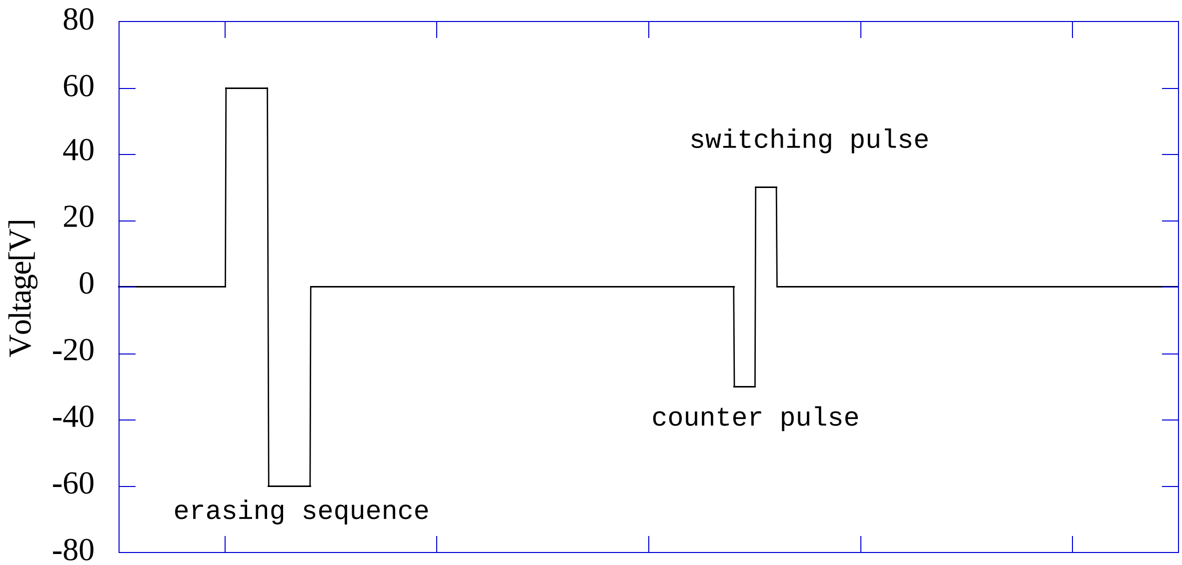


Figure 81. The waveform used for the switching time measurements sequence the cell relaxes to a stable state and is then switched into pulse pair. The size of the switching pulse just enough for latching i counter pulse, monopolar switching behavior can be studied. The pola inverted every frame.

Measurements of the *voltage-time characteristics* were performed using a simple waveform presented in Figure 81. The liquid crystal cell was first erased into one state by a sufficiently large bipolar pulse, and allowed to relax to a field-free stable state. Then either a bipolar or a monopolar switching pulse was applied. For each amplitude of the switching pulse, its width was adjusted to the minimum value necessary to obtain clean latching into the counter state, which was observed during another field-free period. This value was assumed to be the switching time of the cell at the set voltage level. In order to assure the symmetry, the described pulse sequence was repeated with inverted polarity. Even such a simple waveform takes full advantage of the pulse-coupling capability of the Waveform Generator software. It is enough to change the size of one pulse during the measurements: any required adjustments of the remaining pulses are automatically performed before delivering the changed waveform to the liquid crystal cell.

11 Conclusions and Outlook

11.1 Comparison of the Multiplexing Methods

A number of addressing schemes have been presented and discussed in this work. They were also categorized as normal, hold-back and hold-on modes. Each method has its advantages and disadvantages, and comparisons can be made from very different points of view. In the first place one has to judge the achievable speed against the required voltage. The results are presented separately for the three reference cells, in Figure 82. The addressing speed is marked in the diagram by white circles and expressed as the line addressing time, taking into account eventual need for two scanning subframes (as in the Seiko, JOERS/Alvey and original Malvern schemes). The voltage required by each addressing scheme (black squares) is given as a sum of maximum amplitudes of the row and column waveforms. The addressing schemes are presented in the order of increasing voltage.

A low speed of traditional addressing schemes operating in the normal mode (like Seiko) has been significantly improved by introducing blanking and time-overlap of the selection sequences (N21, N4631, CTF, HOE, HOM). Still, in order to achieve a reasonably short switching time, liquid crystals exhibiting high spontaneous polarization would have to be used in these schemes, which has many drawbacks (for instance, the reverse switching effect). Low frequency of the data pulses causes substantial oscillations in the electro-optic response which is detrimental for the achievable contrast.

The hold-back (SW, SDS, ROM, Malvern) and hold-on (F4631, PS) addressing modes utilize dielectric torques, generated by a high frequency crosstalk field, to achieve contrast enhancement and high speed of operation. Hence, the biaxiality of the dielectric tensor plays an important role and liquid crystals with relatively large $\partial\varepsilon$ are preferred. Also, lower values of the spontaneous polarization can be used. In contrast to the cells intended for the normal addressing mode, a weak surface anchoring is of advantage. As can be seen in the diagram, very high voltage levels do not necessarily have to be used for high speed operation.

Operation of these fast addressing schemes (i.e. hold-back and hold-on modes) has not, so far, been demonstrated on large display panels. It is clear, however, that due to the high frequency of the applied waveforms, the impedance of the electrodes is a critical factor. Moreover, these addressing schemes are generally not compatible with currently available integrated display drivers. Display panel prototypes of suitable size cannot be fabricated with facilities available for university research groups and further studies can only be conducted in close cooperation with industrial research laboratories.

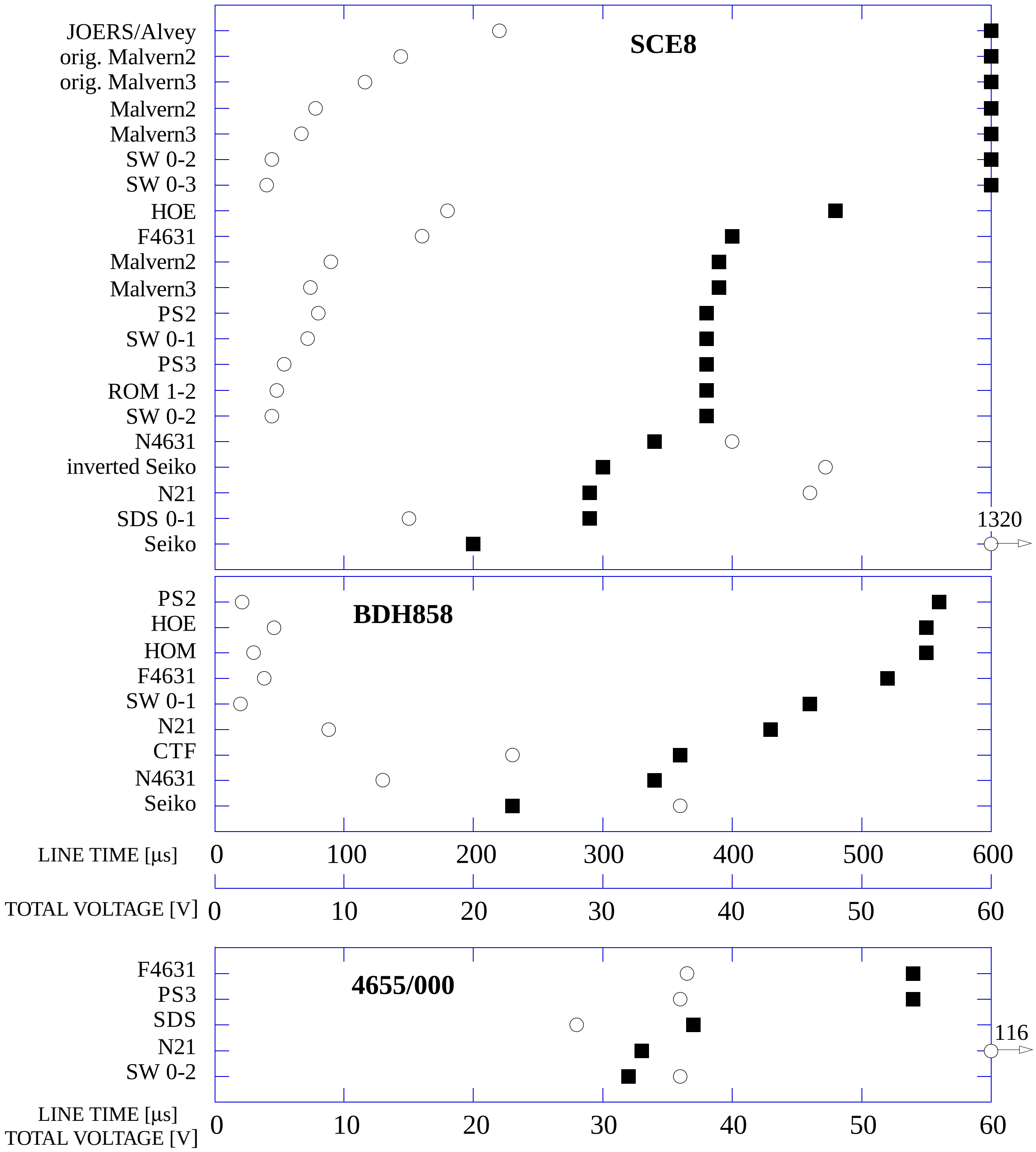


Figure 82. Comparison of the addressing schemes discussed in the present work. For each scheme the effective line addressing time (white circles) and the total voltage (black squares) equal to the sum amplitudes of selection and data waveforms. The cells are presented in separate diagrams because they exhibit different switching speed. The numbers stated after SW and ROM addressing schemes refer to the width of the writing pulse (for example, in the ROM 1-2 scheme the writing pulse is extended over one preceding and two succeeding control windows).

11.2 The Research Progress in the Last Decade

Electronic addressing of SSFLC displays is a very recent field of research. When Clark and Lagerwall disclosed for the first time the concept of surface-stabilized ferroelectric liquid crystals and demonstrated its bistability and microsecond response, at the International Liquid Crystal Conference in Kyoto, 1980, there was much surprise and enthusiasm but also a considerable scepticism. The critics pointed not only to the required extreme condition of 1–2 μm cell gap which they considered unrealistic, but also to the difficulties in aligning smectic C* materials in the required geometry. Moreover, some critics were sceptical about the possibility of multiplexing a non-rms electro-optic response.

Between 1980 and 1984 some possible solutions to the first two problems were demonstrated, which led to a beginning industrial involvement. Some first demonstrations of multiplexing were presented between 1984 and 1988. At that time, the multiplexing philosophy was entirely based on the old schemes used for rms-responding liquid crystals. One might say that those schemes were only slightly adapted to account for the linear interaction with the field and for the peculiar voltage-time area threshold characteristic for this interaction. In addition the polar switching pulses had to be dc-compensated either by a pulse of the same area, giving a useless and disturbing momentaneous switching, or by several sub-threshold pulses distributed in time. Therefore, these early schemes invariably had line writing times larger than (usually at least four times) the characteristic response time of the material.

Gradually, smarter schemes were invented which separated the significant process steps - erasing, switching and dc-compensation – performing them in part simultaneously on different rows. During the same time the importance of the tensorial property of the dielectric permittivity ε came to be gradually recognized as a result of analyzing the optical response in terms of the newly discovered chevron structure. The research in electronic addressing then entered a new phase, based on the understanding of the real local smectic layer structure and the interplay between ferroelectric and dielectric torque. The modern fast addressing schemes are using this interplay in a subtle way with seemingly minute differences in waveforms, for instance in the hold-back and hold-on effects at different phases of the switching process, where the dielectric torque is just momentarily held back or amplified in order to control the final optical state of the pixel.

However, these schemes are the result of academic research, and there is a considerable time lag between demonstrating their power and implementing them in actual large area displays. This time-lag is in part due to the fact that no industrial effort has been made to develop electronic drivers suitable for FLC addressing – because there has been no market so far for them. In part it is also a necessary consequence of the fact that the FLC material together with the polymer precoating define the major properties of the cell structure and that this structure together with specific material parameters determine the cell response to a particular driving scheme. Hence, the development of new addressing schemes is insolubly related to available FLC materials. New materials with optimized values of ε_1, ε_2, ε_3 and P_S therefore have to be developed to take advantage of the new schemes and these materials must, on the other hand, give the desired cell structure. As the relation between the molecular design and the ε tensor is only beginning to be understood (the first measurements of all ε components have only been performed in the last years) we can foresee both a new generation of FLC materials and SSFLC cell structures on which the fast addressing modes can be used in future displays. From the Figure 82 we can get an appreciation of what may be achieved. If, for instance, the Split-writing mode SW 0-2 could be implemented on SCE8 – a material with a P_S value of only 5 nC/cm^2 and not at all yet optimized in ε_1, ε_2, ε_3 values – in a present day display, it would enable video rate of HDTV. As the development of the materials is far from completed, future displays may well go beyond this limit, even when other desirable features, like analog grey scale, are included.

12 Acknowledgments

There is a long list of persons to whom I would like to express my deepest gratitude for their unconditional help, interesting discussions and fruitful collaboration. But I will only name a few.

I am very grateful to my supervisors, Professors Torbjörn Lagerwall and Bengt Stebler, for giving me the opportunity to become a member of the Chalmers liquid crystal group, introducing me to the fascinating world of liquid crystals, guiding through the difficult world of Physics and being there when I needed them.

I owe special thanks to professor Paolo Maltese for fruitful and stimulating collaboration and for teaching me his addressing tricks.

I cannot stress enough how I appreciate the friendly support from my colleagues at the department – Gunnar Andersson, Marius Buivydas, Fathi Gouda, Johan Persson and all others. This work would not have been accomplished without their help. I would also like to gratefully acknowledge my international collaborators – Monique Brunet, Fabrizio Bernardini, Vincenzo Ferrara, Erwin De Ley, Kim Yong Bai, Karl-Franz Reinhart, Jürgen Wahl. I owe a lot to Wojciech Kuczynski.

My particular thanks to my brother, Marek Matuszczyk, for his daily support and for all liquid crystal cells he prepared for me.

I am grateful to my parents for rising me up and for encouraging my interest in science.

I dedicate this work and all my life to my wife, Pepi, and our son, Gabriel, with my warmest thanks for their love, support and patience.

I acknowledge the support from the Swedish National Board of Technical Development NUTEK, the ESPRIT 2360 research program, the Swedish Work Environment Fond and the Human Capital and Mobility project “Ferroelectric Liquid Crystals for Displays and Optical Devices” CHRX-CT930-0206

13 References

[1] F.Reinitzer, *Monatshefte für Chemie*, Vol. 9, p. 421 (1888)

[2] J.L.Fergasson, “Liquid Crystals”, *Scientific American*, Vol. 211, p. 77-85 (1964)

[3] G.H.Heilmeier, L.A.Zanoni and L.A.Barton,”Dynamic scattering: a new electrooptic effect in certain classes of nematic liquid crystals”, *Proc. IEEE*, Vol. 56, p. 1162-1171 (1968)

[4] M.Schadt and W.Helfrich,”Voltage-dependent optical activity of a twisted nematic liquid crystal”, *Appl. Phys. Lett.*, Vol. 18, p. 127-128 (1971)

[5] A.Sobel, “Some constraints on the operation of matrix displays”, *IEEE Trans. ED*, Vol. 18, pp. 797-798 (1971)

[6] R.B.Meyer, L.Liébert, L.Strzelecki and P.Keller, “Ferroelectric liquid crystals”, *J. Physique (Lett.)*, Vol. 36, L69-L71 (1975)

[7] N.A.Clark and S.T.Lagerwall, “Submicrosecond bistable electro-optic switching in liquid crystals”, *Appl. Phys. Lett.*, Vol. 36, pp. 899-901 (1980)

[8] K.Kondo, F.Kobayashi, A.Fukuda and E.Kuze, “Preparation of monodomain cells of ferroelectric liquid crystals and their evaluation with an optical microscope”, *Jpn. J. Appl. Phys.*, Vol. 20, pp. 1773-1777 (1981)

[9] N.A.Clark, M.A.Handschy and S.T.Lagerwall, “Ferroelectric liquid crystal electrooptics using the surface stabilized structure” *Mol. Cryst. Liq. Cryst.*, Vol. 94, p. 213-234 (1983)

[10] K.Kondo, H.Takezoe, A.Fukuda and E.Kuze, “A practical method of preparing thin homogeneous ferroelectric smectic cells for electro-optical microsecond switches: alignment control of liquid crystal molecules by utilizing spacer edges”, *Jpn. J. Appl. Phys.*, Vol. 22, No. 2, pp. L85-L87 (1983)

[11] K.Ishihawa, K.Hashimoto, H.Takezoe, A.Fukuda and E.Kuze, “A practical method of preparing thin homogeneous ferroelectric smectic cells for electro-optical microsecond switches (II): Sm A liquid crystal growth under a temperature gradient”, *Jpn. J. Appl. Phys.*, Vol. 23, No. 4, pp. L211-L213 (1984)

[12] T.J.Scheffer and J.Nehring, “A new, highly multiplexable liquid crystal display”, *Appl. Phys. Lett.*, Vol. 45, No. 10, pp. 1021-1023 (1984)

[13] J.M.Geary, “A multiplexed ferroelectric LCD using ac field-stabilized states”, *SID 1985 Digest*, pp. 128-130 (1985)

[14] T.Harada, M.Taguchi, K.Iwasa and M.Kai, “An application of chiral smectic C liquid crystal to a multiplexed large-area display,” *SID Digest*, *Playa del Rey*, 16, pp. 131-134 (May 1985)

[15] K.Ishihawa, Y.Ouchi, T.Uemura, T.Tsuchiya, H.Takezoe and A.Fukuda, “Methods for preparing SSFLC cells and their electro-optical properties”, *Mol. Cryst. Liq. Cryst.*, Vol. 122, pp. 175-190 (1985)

[16] S.T.Lagerwall, J.Wahl and N.A.Clark, “Ferroelectric liquid crystals for displays,” *Proc. IDRC*, pp. 213-221 (1985)

[17] H.Orihara, K.Nakamura, Y.Ishibashi, Y.Yamada, N.Yamamoto and M.Yamawaki, “Anomalous switching behavior of a ferroelectric liquid crystal with negative dielectric anisotropy”, *Jap. J. Appl. Phys.*, Vol. 25, No. 10, pp. L839-L840 (1986)

[18] C.Bowry, A.Mosley and B.M.Nicholas, “Four slot and two slot multiplexing schemes for ferroelectric liquid crystal displays,” *Conf. Record of the IDRC, London*, pp. 152-155 (Oct. 1987)

[19] J.Dijon, P.Maltese and C.Ebel “A 6” diagonal black and white ferroelectric panel: switchability for TV rate grey levels,” *Conf. Record of the IDRC, London*, pp. 40-43 (Oct. 1987)

[20] S.T.Lagerwall, B.Otterholm and K.Skarp, “Material properties of ferroelectric liquid crystals and their relevance for applications and devices”, *Mol. Cryst. Liq. Cryst.*, Vol. 152, pp. 503-587 (1987)

[21] S.Okada, J.Kanbe, A.Tsuboyama and Y.Inaba, “Ferroelectric display panel of varying thickness and driving method therefor”, Canon Inc., US Patent 4712877 (1987)

[22] T.Rieker, N.A.Clark, G.S.Smith, D.S.Parmar, E.B.Sirota and C.R.Safinya, “Chevron local layer structure in surface-stabilized ferroelectric smectic C cells”, *Phys. Rev. Lett.*, Vol. 59, No. 23, pp. 2658-2661 (1987)

[23] Xue Jiu-Zhi, M.A.Handschy and N.A.Clark, “Electrooptic response during switching of a ferroelectric liquid crystal cell with uniform director orientation”, *Ferroelectrics*, Vol. 73, pp. 305-314 (1987)

[24] Xue Jiu-Zhi, M.A.Handschy and N.A.Clark, “Electrooptical switching properties of uniform layer tilted surface stabilized ferroelectric liquid crystal devices”, Liq. Cryst., Vol. 2, No. 5, pp. 707-716 (1987)

[25] J.Dijon, C.Ebel. C.Vauchier, F.Baume, J.-F.Clerc, M.Estor, T.Leroux, P.Maltese and L.Mulatier, “High speed Sc* mixtures: an evaluation of their performances”, SID 88 Digest, pp. 246-249 (May 1988)

[26] C.Escher, T.Gelhaar and E.Böhm, “Measurement of the rotational viscosity of ferrroelectric liquid crystals based on a simple dynamical model”, *Liq. Cryst.*, Vol. 3, No. 3, pp. 469-484 (1988)

[27] W.J.A.M.Hartmann, “Uniform SSFLC director pattern switching”, *Ferroelectrics*, Vol. 85, pp. 67-77 (1988)

[28] W.J.A.M.Hartmann, “Ferroelectric liquid crystal video display”, *Proc. Int. Disp. Res. Conf.*, San Diego, pp. 191-194 (1988)

[29] J.R.Hughes and F.C.Saunders, “Inversion of contrast in ferroelectric smectic C liquid crystal displays”, *Liq. Cryst.*, Vol. 3, No. 10, pp. 1401-1410 (1988)

[30] Y.Inaba, K.Katagiri, H.Inoue, J.Kanbe, S.Yoshihara and S.Iijima, “Essential factors in high-duty FLC matrix display,” *Ferroelectrics*, Vol. 85, pp. 255-264 (1988)

[31] T.Leroux, F.Baume, J.F.Clerc, J.Dijon, C.Ebel, L.Mulatier and C.Vauchier, “Black and white FLC TV panel with grey levels,” *Proc. IDRC, San Diego*, pp. 111-113 (1988)

[32] P.Maltese, J.Dijon and T.Leroux, “Fast addressing modes for ferroelectric LC display panels,” *Proc. IDRC, San Diego*, 98-101, (1988)

[33] P.Maltese, J.Dijon, T.Leroux and D.Sarrasin, “Addressing cycles for fast settling grey shades in ferroelectric liquid crystal matrices,” *Ferroelectrics*, Vol. 85, pp. 265-276 (1988)

[34] T.Nagata, T.Umeda, T.Igawa, A.Mukoh and Y.Hori, “Effect of spontaneous polarization and viscosity of ferroelectric liquid crystals on ac field-stabilization phenomena”, *Proc. Int. Disp. Res. Conf.*, San Diego, pp. 185-190 (1988)

[35] P.W.Ross, “720x400 matrix ferroelectric display operating at video frame rate”, *Proc. Int. Disp. Res. Conf.*, San Diego, pp. 94-97 (1988)

[36] J.Wahl “Electronic addressing of FLC devices”, *Ferroelectrics*, Vol. 85, pp. 207-233 (1988)

[37] J.J.Wysocki, S.K.Hark and J.Hull, “Response time and contrast ratio of ferroelectric liquid crystal cells”, *Proc. Int. Disp. Res. Conf.*, San Diego, pp. 102-106 (1988)

[38] C.Escher, H.-R.Dubal, T.Harada, G.Illian, M.Murakami and D.Ohlendorf, “Impact of ionic impurities on the performance of SSFLC displays – a quantitative analysis”, *Proc. of Japan Display*, SID, pp. 348-351 (Oct. 1989)

[39] W.J.A.M.Hartmann, “Charge-controlled phenomena in the surface-stabilized ferroelectric liquid crystal structure”, *J. Appl. Phys.*, Vol. 66, pp.1132-1132 (1989)

[40] S.T.Lagerwall, N.A.Clark, J.Dijon and J.F.Clerc, “Ferroelectric liquid crystals: the development of devices”, *Ferroelectrics*, Vol. 94, pp. 3-62 (1989)

[41] F.C.Saunders, J.R.Hughes, H.A.Pedlingham and M.J.Towler, “Electro-optic pulse response of ferroelectric liquid crystals”, *Liq. Cryst.*, Vol. 6, No. 3, pp. 341-347 (1989)

[42] Y.Sato, T.Tanaka, H.Kobayashi, K.Aoki, H.Watanabe, H.Takeshita, Y.Ouchi, H.Takezoe and A.Fukuda, “High quality ferroelectric liquid crystal display with quasi-bookshelf layer structure”, *Jpn. J. Appl. Phys.*, Vol. 28, No. 3, pp. L483-L486 (1989)

[43] T.Uchida, M.Hirano and H.Sakai, “Director orientation of a ferroelectric liquid crystal on substrates with rubbing treatment: the effect of surface anchoring strength,” *Liquid Crystals*, Vol. 5, No. 4, pp. 1127-1137 (1989)

[44] N.Yamamoto, Y.Yamada, K.Mori, H.Orihara and Y.Ishibashi, “Ferroelectric liquid crystal display with high contrast ratio”, *Jpn. J. Appl. Phys.*, Vol. 28, No. 3, pp. 524-529 (1989)

[45] K.H.Yang. T.C.Chieu and S.Osofsky, “Depolarization field and ionic effects on the bistability of surface-stabilized ferroelectric liquid-crystal devices”, *Appl. Phys. Lett.*, Vol 55, no. 2, pp.125-127 (1989)

[46] J.Dijon, “Ferroelectric LCDs”, Chapter 13 in B.Bahadur (ed.) *Liquid Crystals, Applications and Uses*, Vol.1, World Scientific (1990)

[47] W.J.A.M.Hartmann and A.M.M.Luyckx-Smolders, “The bistability of the SSFLC effect in electrically-reoriented chevron structures”, *J. Appl. Phys.*, Vol. 67, pp. 1253-1261 (1990)

[48] K.Nakao, N.Wakita and T.Uemura, “The gray scale feasibility of ferroelectric liquid crystal cell”, *16th Natl. (Japan) Liq. Cryst. Conf.*, Univ. of Hiroshima, pp. 272-273 (Oct. 1990)

[49] T.Uwano, Y.Idoo, M.Oyama, M.Kuwahara, H.Onnagawa and K.Miyashita, “Feasibility of gray scale in ferroelectric liquid crystal cells”, *16th Natl. (Japan) Liq. Cryst. Conf.*, Univ. of Hiroshima, pp. 274-275 (Oct. 1990)

[50] A.G.H.Verhulst, W.J.A.M.Hartmann, F.J.Stommels and A.M.M.Luyckx-Smolders, “The Texture Method, an analogue grey-scale technique for SSFLC displays based on local reorientation of the smectic layers”, *Proc. 10th Intl. Display Research Conf.*, pp. 150-153 (1990); *Proc. SID*, Vol. 32/4, pp. 379-386 (1991)

[51] J.Dijon, T.Leroux and P.Maltese, “Design of addressing schemes for FLC displays”, *Ferroelectrics*, Vol. 113, pp. 371-386 (1991)

[52] C.Escher, H.R.Dübal, T.Harada, G.Illian, M.Murakami and D.Ohlendorf, “The SSFLC switching behaviour in view of chevron layer geometry and ionic charges”, *Ferroelectrics*, Vol. 113, pp. 269-303 (1991)

[53] W.J.A.M.Hartmann, “Ferroelectric liquid crystal displays for television application”, *Ferroelectrics*, Vol. 122, pp. 1-26 (1991)

[54] W.J.A.M.Hartmann, “A passive matrix addressed ferroelectric liquid-crystal video display”, *Proc. SID*, Vol. 32/2, pp. 115-120 and Vol. 32/3, pp. 256 (1991)

[55] J.C.Jones, E.P.Raynes, M.J.Towler and J.R.Sambles, “Dielectric biaxiality in S_c host systems”, *Mol. Cryst. Liq. Cryst.*, Vol. 199, pp. 277-285 (1991)

[56] J.C.Jones, M.J.Towler and E.P.Raynes, “The importance of dielectric biaxiality for ferroelectric liquid crystal devices”, *Ferroelectrics*, Vol. 121, pp. 91-102 (1991)

[57] J.Kanbe, H.Inoue, A.Mizutome, Y.Hanyuu, K.Katagiri and S.Yoshihara, “High resolution, large area display with graphic performance”, *Ferroelectrics*, Vol. 114, pp. 3-26 (1991)

[58] B.Maximus, E.DeLey, A.DeMeyere and H.Pauwels, “Ion transport in SSFLCDs”, *Ferroelectrics*, Vol. 121, pp. 103-112 (1991)

[59] C.Reynaerts, J.van Campenhout and F.Cuypers, “Time integration grey scales for ferroelectric LCD’s”, *Ferroelectrics*, Vol. 113, pp. 419-437 (1991)

[60] P.W.H.Surguy, P.J.Ayliffe, M.J.Birch, M.F.Bone, I.Coulson, W.A.Crossland, J.R.Hughes, P.W.Ross, F.C.Saunders and M.J.Towler, “The ‘JOERS/Alvey’ ferroelectric multiplexing scheme,” *Ferroelectrics*, Vol. 122, pp. 63-79 (1991)

[61] K.Nakao, N.Wakita, T.Uemura and H.Yamazoe, “A novel gray scale display method in ferroelectric liquid crystal display”, *IEEE Tokyo Section*, No. 30 (1991)

[62] N.Wakita, Y.Iwai, T.Uemura, S.Fujiwara, Y.Gohara, I.Ota, Y.Masumoto, Y.Miyatake, T.Tsuda and Y.Horio, “Multi-color projection display using 3 FLC LVs with 4 million pixels”, *Ferroelectrics*, Vol. 114, pp. 27-41 (1991)

[63] C.Escher, G.Illian, A.Kaltbeitzel, J.Manero, D.Ohlendorf, H.Rieger, N.Reusch, H.Schlosser, P.Wegener and R.Wingen, “Surface stabilized ferroelectric liquid crystals (SSFLC) - a promising technology for high resolution displays,” *SPIE IS&T Symposium, San Jose* (Feb. 1992)

[64] F.M.Gouda, “Dielectric relaxation spectroscopy of chiral smectic liquid crystals”, Ph.D. thesis, Chalmers University of Technology (1992)

[65] J.C.Jones and E.P.Raynes, “Measurement of the biaxial permittivities for several smectic-C host materials used in ferroelectric liquid crystal devices”, *Liq. Cryst.*, Vol. 11, No. 2, pp. 199-217 (1992)

[66] M.Koden, H.Katsuse, A.Tagawa, K.Tamai, N.Itoh, S.Miyoshi and T.Wada, “Four states of surface-stabilized ferroelectric liquid crystal with parallel rubbing“, Jpn. J. Appl. Phys., vol. 31, pp. 3632-3635 (1992)

[67] E.DeLey, A.DeMeyere, B.Maximus, P.Vetter and H.Pauwels “Ionic effects in LCD’s”, *Liquid Crystals and Solid State Crystals*, SPIE Vol. 1845, pp.391-399 (1992)

[68] P.Maltese, “Advances and problems in the development of ferroelectric liquid crystal displays,” *Mol. Cryst. Liq. Cryst.*, Vol. 215, pp. 57-72 (1992)

[69] S.Okada, Y.Inaba and K.Katakura, “Liquid crystal display apparatus”, European Patent Appl. 0 545 400 A2, Canon Inc. (1992)

[70] M.J.Towler, J.C.Jones and E.P.Raynes, “The effect of the biaxial permittivity tensor and tilted layer geometries on the switching of ferroelectric liquid crystals”, *Liq. Cryst.*, Vol. 11, pp. 365-371 (1992)

[71] A.Tsuboyama, Y.Hanyu, S.Yoshihara and J.Kanbe, “Characteristics of the large size, high resolution FLCD,” *Proc. of Japan Display*, pp. 53-56 (1992)

[72] N.Wakita, Y.Kobbayashi, S.Fujiwara, K.Nakao, T.Uemura and H.Yamazoe, “Grey scales on ferroelectric liquid crystals by weighted subfield”, National Tech. Report, Vol. 38, No. 3, pp. 313-317 (1992)

[73] G.Andersson, “Electro-optic effects in chiral smectic liquid crystals”, Ph.D. thesis, Chalmers University of Technology (1992)

[74] W.A.Crossland and A.B.Davey, “Addressing requirements for chiral smectic liquid crystal active backplane spatial light modulators”, *Ferroelectrics*, Vol. 149, pp. 361-374 (1993)

[75] D.G.McDonnel, R.W.Bannister, A.Graham, J.R.Hughes, H.A.Pedlingham, D.C.Scattergood and C.J.T.Smith, “An ultra high resolution ferroelectric liquid crystal video display,” *Digest of Tech. Papers of the 1993 SID Symposium, Seattle*, pp. 654-657 (May 1993)

[76] Y.Hanyu, K.Nakamura, Y.Hotta, S.Yoshihara and J.Kanbe, “Molecular alignment of a very large size FLCD”, SID 93 Digest, pp. 364-367 (1993)

[77] W.J.A.M.Hartmann, A.G.H.Verhulst, J.A.M.M.van Haaren and F.J.J.Blommaert, “The possibilities of ferroelectric liquid crystals for video displays”, *Journal of SID*, Vol. 13, (1993)

[78] J.R.Hughes and E.P.Raynes, “A new set of high speed matrix addressing schemes for ferroelectric liquid crystal displays,” *Liq. Cryst.*, Vol. 13, pp. 597-601 (1993), errata corrige Vol. 15, pp. 281-282 (1993)

[79] N.Itoh, M.Koden, S.Miyoshi and T.Wada, “Study of molecular orientational states of ferroelectric liquid crystals in a surface stabilized geometry“, *Liq. Cryst.*, Vol. 15, No. 15, pp. 669-687 (1993)

[80] J.C.Jones, M.J.Towler and J.R.Hughes, “Fast, high-contrast ferroelectric liquid crystal displays and the role of dielectric biaxiality”, *Displays*, Vol. 14, No 2, pp. 86-93 (1993)

[81] M.Koden, H.Katsuse, N.Itoh, T.Kaneko, K.Tamai, H.Takeda, M.Kido, M.Matsuki, S.Miyoshi and T.Wada, “Ferroelectric liquid crystal device using the τ–V_{MIN} mode”, *Ferroelectrics*, Vol. 149, pp. 183-192 (1993)

[82] P.Maltese, “Wide high-voltage addressing modes for SSFLC matrix displays, ”*Conf. Record of the 1993 IDRC Strasbourg*, pp. 371-375 (1993)

[83] P.Maltese and R.Piccolo, “Superfast addressing modes for SSFLC matrix displays”, *Digest of Technical Papers of the 1993 SID Symposium, Seattle*, pp. 642-645 (May 1993)

[84] P.Maltese, R.Piccolo and V.Ferrara, “An addressing effective computer model for surface stabilized ferroelectric liquid crystal cells,” *Liquid Crystals*, Vol. 15, No. 6, pp. 819-834 (1993)

[85] M.Matuszczyk, “Development of fast-switching chiral smectic electro-optic devices”, Lic. Eng. Thesis, Chalmers University of Technology (1993)

[86] S.Okada, Y.Inaba, T.Kato and K.Katakura, “Display apparatus”, European Patent Appl. 0 564 263 A2, Canon Inc. (1993)

[87] S.Okada, Y.Inaba and K.Katakura, “Method and apparatus for liquid crystal display”, European Patent Appl. 0 605 865 A1, Canon Inc. (1993)

[88] M.Terada, S.Yamada, K.Katagiri, S.Yoshihara and J.Kanbe, “Static and dynamic properties of chevron uniform FLC”, *Ferroelectrics*, Vol. 149, pp. 283-294 (1993)

[89] A.Yasuda, Y.B.Yang, K.Nito and H.Takanashi, “Gray-scale method utilizing FLCs containing ultra-fine particles”, *Eurodisplay*, pp. 59-62 (1993)

[90] F.Gouda, M.Buivydas, T.Carlsson, S.T.Lagerwall and B.Stebler, “Frequency dependence of the dielectric biaxiality in the chiral smectic C* phase and the observation of a compound with negative dielectric biaxiality”, *Physics Lett. A*, Vol. 190, pp. 345-348 (1994)

[91] J.A.M.M.van Haaren, W.J.A.M.Hartmann and A.G.H.Verhulst, “Switching on stray electric fields in ferroelectric liquid crystal cells”, *Liq. Cryst.*, Vol. 16, No. 5, pp. 735-748 (1994)

[92] E.DeLey, “Schakelen in ferroëlektrische vloeibaar-kristalbeeldschermen”, Ph.D. Thesis, University of Gent (1994)

[93] P.Maltese and V.Ferrara, “Improved addressing modes for SSFLC matrix displays”, *Proc. IDRC, Monterey*, (Oct. 1994)

[94] E.DeLey, H.Pauwels and V.Ferrara, “The influence of an inhomogeneous electric field on SSFLC-addressing”, *Proc. IDRC, Monterey*, pp.499-502 (Oct. 1994)

[95] P.Maltese, V.Ferrara and R.Piccolo, “Automated tracing of operating regions of high speed addressing modes for FLC matrix displays,” *Proc. SID*, San Jose, pp. 151-154 (June1994)

[96] K.Myojin, H.Moritake, M.Ozaki, K.Yoshino, T.Tani and K.Fujisawa, “Unidirectional layer alignment in ferroelectric liquid crystal with N*-C* phase sequence”, *Jpn. J. Appl. Phys.*, Vol. 33, No. 9B, pp. 5491-5493 (1994)

[97] P.Maltese, V.Ferrara and A.Coccettini, “Studies on addressing techniques for bistable ferroelectric liquid crystal cells,” *presented to the 1st SICL Conf., Amalfi, June 1994, accepted for publication in Mol. Cryst. Liq. Cryst.*

[98] S.T.Lagerwall and B.Stebler, “The linear electro-optic effects in liquid crystals,” presented to 11th Conference on Solid and Liquid Crystals, Zakopane, October 1994, *Proc. SPIE*, in press (1995)

14 LIST OF PAPERS

PAPER I

A dynamic picture of a ferroelectric liquid crystal screen in multiplex drive
J. Wahl, T. Matuszczyk and S. T. Lagerwall
Molecular Crystals Liquid Crystals, Vol. 146, pp. 143-150 (1987)

PAPER II

Experimental driver and addressing techniques for ferroelectric liquid crystal devices
J. Wahl and T. Matuszczyk
Journal of Physics E: Scientific Instruments, Vol. 21, pp. 460-466 (1988)

PAPER III

A 1" x 0.5" FLC bar-graph display with short-term memory
K. Skarp, M. Matuszczyk, T. Matuszczyk, B. Bijlenga, Å. Hörnell, B. Stebler and S. T. Lagerwall
Ferroelectrics, Vol. 85, pp. 313-325 (1988)

PAPER IV

Dielectric anisotropy and dielectric torque in ferroelectric liquid crystals and their importance for electro-optic device performance
F. Gouda, G. Andersson, M. Matuszczyk, T. Matuszczyk, K. Skarp and S. T. Lagerwall
Journal of Applied Physics, Vol. 67, No. 1, pp. 180-186 (1990)

PAPER V

Addressing of ferroelectric liquid crystal matrices and electrooptical characterization
K-F. Reinhart, L. Dorfmüller, K. Marx and T. Matuszczyk
Ferroelectrics, Vol. 113, pp. 405-417 (1991)

Paper VI

Determination of the dielectric biaxiality in a chiral smectic-C phase

F.M. Gouda, W. Kuczynski, S.T. Lagerwall, M. Matuszczyk, T. Matuszczyk and K. Skarp

Physical Review A, Vol. 46, No. 2, pp. 951-958 (1992)

Paper VII

Waveform generator for ferroelectric liquid crystal devices

T. Matuszczyk and S. T. Lagerwall

Ferroelectrics, in press (1994)

Paper VIII

Investigations on restoring torques in bistable SSFLC cells

T. Matuszczyk, P. Maltese and F. Bernardini

presented to the I Congresso della Società Italiana Cristalli Liquidi (SICL), Amalfi, June 1994

Molecular Crystals Liquid Crystals, in press (1994)

Paper IX

Studies on bistability phenomena in SSFLC cells

T. Matuszczyk, M. Buivydas, S. T. Lagerwall, F. Bernardini and P. Maltese

Proc. International Display Research Conference, Monterey, pp. 221-224 (October 1994)

Paper X

Addressing modes of ferroelectric liquid crystal displays

T. Matuszczyk and P. Maltese

presented to 11th Conference on Solid and Liquid Crystals, Zakopane, October 1994

Proc. SPIE, Vol. 2372, pp. 296-309 (1995)

15 Summary of Papers

Paper I demonstrates the possibility of multiplexing the surface stabilized ferroelectric liquid crystal devices (which had been questioned since 1980) in dynamic mode. A moving SSFLC pattern is demonstrated for the first time, on a 16 by 16 element matrix. Photographs of the experimental set-up and displayed pattern are presented along with the 5-slot addressing scheme and the block diagram of the electronic circuitry.

Paper II discusses the switching properties of ferroelectric liquid crystals, addressing techniques and driving waveforms. An improved, 4-slot multiplexing scheme with enhanced dielectric stabilization, is presented. A possibility of selective addressing is pointed out and suitable addressing waveforms, both for a linear array and a matrix display, are proposed. The construction of a nearly universal, experimental SSFLCD driver is described. The internal structure of commercial TN-LCD integrated drivers is presented and their suitability for addressing SSFLC devices discussed.

Paper III describes the construction and performance of a bar-graph display composed of 96 stripe electrodes of 200 µm width. This linear array was used to demonstrate a grey scale for the first time. A dynamic pattern, displaying eight shades, was generated by pure temporal dither.

Paper IV deals with the dielectric properties of ferroelectric liquid crystals of relevance for electronic addressing. Measurements of the dielectric anisotropy are presented and the dielectric torque calculated. The interplay between dielectric and ferroelectric torques, of importance for the stabilization of liquid crystal molecules during multiplexing, is discussed and conclusions for addressing techniques are drawn.

Paper V presents the addressing experiments made on ferroelectric liquid crystal prototype matrices. The temperature dependence of the critical pulse area is investigated. A time-overlap addressing scheme is evaluated along with a conventional one. Experiments with generation of grey scale based on digital and analogue techniques are described. The method of achieving a grey scale based on analogue addressing of pixels having discrete threshold steps, obtained by evaporating additional dielectric layers, is proposed.

Paper VI deals with the biaxiality of the dielectric tensor. A method of experimental determination of its three principal values for C* liquid crystal is proposed. The measurements have been performed on an ester compound exhibiting A* and C* phases. The dielectric tensor components are presented as functions of temperature and frequency of the applied electric field. The implications for addressing methods are discussed.

Paper VII describes the construction of the waveform generator dedicated primarily to electronic addressing of liquid crystals. The design assumptions are unique and could not, so far, be found in any commercial instrument. Each generated pulse has an individual width and the use of two memory banks allows undisturbed editing of the waveforms *during operation*. The waveform generator has eight synchronized channels capable of pulse amplitudes up to ±100 V. Extensive software has been developed for the Macintosh computer to design and test the addressing schemes. Recently the program has been complemented by a simulation of the electro-optic response of SSFLC cells.

Paper VIII reports the investigations on the equilibrium restoring torques in bistable SSFLC cells. It presents measurements of the optical response of the cells driven by specially designed test waveforms. Switching slopes are also measured under different conditions. The balance of elastic, dielectric and ferroelectric torques is experimentally studied.

Paper IX continues the work of the previous paper. Delay and rise time of the electro-optic response is studied in detail. Simulation parameters for two cells are established through three different kinds of experiment. The simulated electro-optic response is compared with the measured one.

Paper X gives a general discussion on the construction of multiplexing waveforms for ferroelectric liquid crystal devices. Conventional addressing methods are opposed to more recent ones, where time-overlap of the selection waveforms and dynamic contrast enhancement due to dielectric effects induced by high frequency of data waveforms is extensively utilized. A general classification of addressing modes is suggested and representative addressing schemes are discussed in detail. A new “Split Writing” addressing scheme is proposed.